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Research Article

Low Power methodology for SRAM Memory using Dynamic Threshold MOS Transistor

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Abstract

Memory is a physical device capable of storing information temporarily or permanently. It is the most important part in complementary metal oxide semiconductor (CMOS) integrated circuit applications. It has been broadly used in VLSI (Very Large Scale Integration) circuits. SRAM is volatile in the conventional sense that data is eventually lost when the memory is not powered. Most important factor is that by applying various techniques its performance should not be changed and other factors such as area and speed should be taken into account. Thus in the design of SRAM cell using DTMOS (Dynamic Threshold Metal Oxide Semiconductor), body terminal is connected to the gate terminal is a promising method for achieving enhanced performance without even modifying the existing structure of MOSFET. This is the major advantage of DTMOS as it is fully compatible with the conventional CMOS process. Hence SRAM (Static Random Access Memory) memory cell by using DTMOS technique were designed and parameters like power, delay and power delay product has been analyzed and it is compared with the existing techniques. It can be used in personal computers, work stations, routers and peripheral equipment. On an average 33% of power has been reduced using DTMOS technique compared to conventional CMOS circuit. Thus the Proposed SRAM cell be used for used low power VLSI application. All the circuits were designed using TANNER EDA tool.

Keywords: Memory; Static Random Access Memory; Low power; Dynamic Threshold Logic.

Introduction

VLSI is the process of creating an IC (Integrated Circuit) by combining thousands of transistors into a single chip. VLSI began when complex semiconductor and communication technologies were being developed. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU (Central Processing Unit), Read Only Memory (ROM), Random Access Memory (RAM) and other glue logic. VLSI lets IC designers add all of these into one chip. VLSI has been around for a long time, there is nothing new about it but as a side effect of advances in the world of computers, there has been a dramatic proliferation of tools that can be used to design VLSI circuits. Alongside, obeying Moore's Law, the capability of an IC has increased exponentially over the years, in terms of computation power, utilization of available area, yield. The combined effect of these two advances is that people can now could diverse functionality into the IC's, opening up new frontiers [1].

The power dissipation in VLSI circuit is due to three major sources i.e. power required to charge or discharge a node, power dissipation [2] due to output transition and power dissipation due to leakage current. Static power dissipation becomes an issue when circuits inactive or in a power down mode. It becomes more important when there is no activity doing circuit and they all biased to a specific state. The static power dissipation includes sub threshold and reverse biased diode leakage current. Dynamic power dissipation is due to the repeated charging and discharging of the output capacitance is necessary to transmit information in CMOS circuit [3]. Real circuit signals have non zero rise and fall times which causes both P_{net} and the N_{net} of the CMOS gate to conduct current simultaneously. This leads to flow of a short circuit current for a short period of time. All the above power dissipation depends on activity,

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timing, output capacitance and supply voltage of the circuit.

Memory plays an essential role in the design of electronic system [4] where storage of data is required. The amount of memory required depends on the type of application. On chip memory has been widely used in VLSI circuits. Random Access memory is a form of computer data items to be read and written in approximately the same amount of time regardless of order in which data items are accessed. RAM is volatile in nature it means that the information can be accessed only when the power is ON. It can be classified into the two types. SRAM is a type of semiconductor memory that uses bistable launching circuit to store each bit [5]. SRAM is static in nature and data stored in SRAM need not to be refreshed periodically so it consumes less power. SRAM is more preferable compared to DRAM (Dynamic Random Access Memory) because of its high speed operation, large noise margin and logic compatibility. SRAM is mostly used in cache memories in main frame, micro processer. DRAM is a type of volatile memory. DRAM can hold more data than SRAM of same size chip but capacitor needs to be refreshed periodically [6]. The DRAM cell consist of capacitor to store binary information and a transistor to access the capacitor.

The integrated circuit performance mostly depends on the basic devices [7] and its scaling methods, but in conventional CMOS devices in ultra deep submicron technology, leakage power becomes the major portion apart of dynamic power. The demerits of the conventional CMOS is less speed and, more leakage, for any digital design PDP (Power Delay Product) is the figure of merit which can be used to determine energy consumed per switching event, hence we designed a NOVEL NMOS and PMOS which has superior performance than conventional PMOS and NMOS. This has superior performance than conventional PMOS and NMOS [8].

A dual threshold voltage and sleep switch dual threshold voltage for leakage reduction [9] in domino logic circuits by DOIND (Domino logic with clock and input dependent transistors) approach. This technique is used for reducing the sub threshold leakage power consumption in domino logic circuit. Dual threshold voltage DOIND and NMOS sleep switch dual threshold voltage DOIND circuits for low leakage domino logic circuits are presented. High threshold voltage transistors are utilized to reduce the leakage current and a sleep transistor is added to the dynamic node that strongly turnoff all the high threshold voltage transistor and significantly reduce the sub threshold leakage power. DTMOS technique meets the requirement [10] for the low voltage and low power for the design of analog circuits. Due to larger current driving capacity and low leakage current, DTMOS is attractive for low power applications. In this work high performance super cascode CMOS is analyzed using DTMOS technique. Modified circuit has high accuracy with very less current copying error.

Existing Design Methodologies

6T SRAM Cell

The 6T SRAM cell consists of 6 transistor, two pull up transistor (PMOS_1, PMOS_2), two pull down transistor (NMOS_2, NMOS_3) and two pass transistors (NMOS_1, NMOS_2). The gate of pass transistor is controlled by the word line input (WL). Whenever the word line is high the BL and BLB are connected to the cell hence the cell can be read out or write in from the bit lines. When the WL is off there is no reading or writing is performed by the cell, hence the cell will be in the hold state [11].

For success writing to be done in the cell there must be a write driver which monitor the presence of data and allows the data to be written into the cell. This write driver is simple a AND gate whose input are write enable and data. The schematic diagram of conventional 6T SRAM cell is shown in Fig. 1. When reading is to be done the write enable of the write driver is switch off so that writing is not performed. Reading is carried out with the help of sense amplifier. There is a column transistor which is ON by the read enable input when the reading is carried out by the sense amplifier. Sense amplifier is a differential amplifier which senses the difference between the voltages in BL and BLB.

It is also very important to mention here that before reading is to begin the BL and BLB are to be pre charge to the certain level of voltage so that both the lines would have same voltage. This pre charge is done by the pre charge circuit.

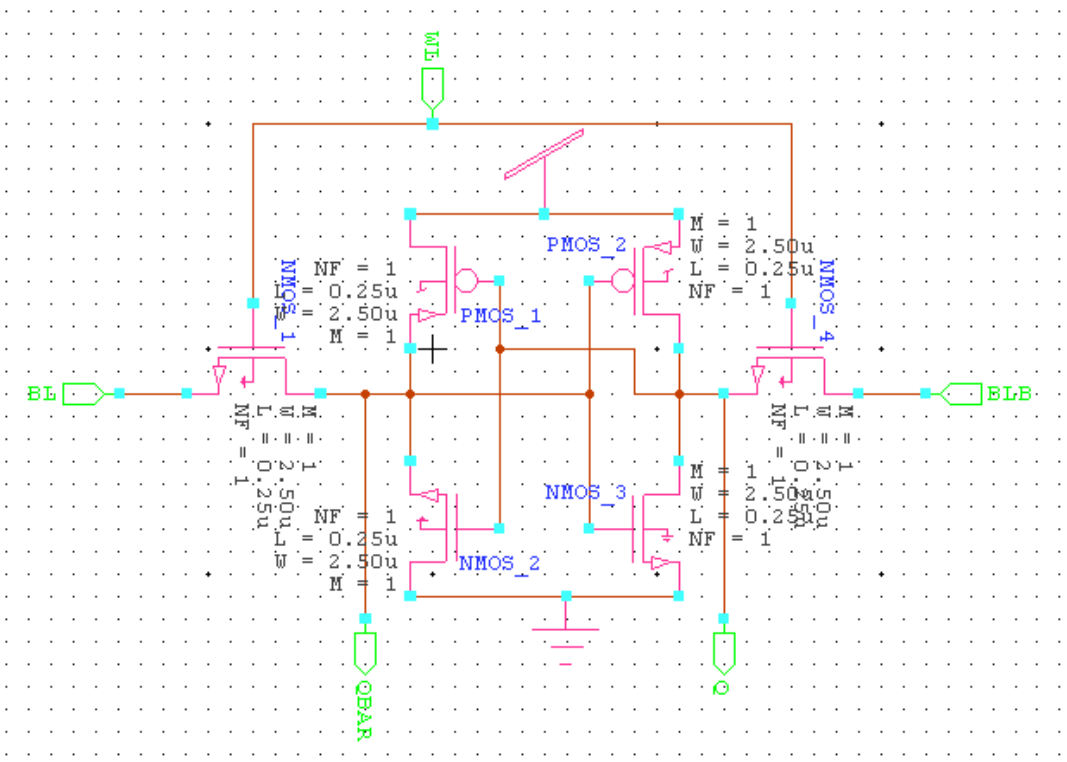

Fig. 1. Schematic diagram of SRAM cell

Multi Threshold Logic

Multi-threshold CMOS (MTCMOS) is a popular power gating approach that uses high V_t devices for power gating in order to achieve low power [12]. High threshold transistors which are normally slow, but have a low sub threshold leakage current are used as sleep transistors (S and S).The techniques of MTCMOS consist of inserting an additional PMOS sleep transistor (S) with high V_t in series between PUN and power supply. Similarly, a high V_t NMOS sleep transistor (S) is also inserted between PDN and ground. During active mode, both the high V_t transistors are turned ON, so the low V_t transistors in PUN (Pull up Network) and PDN (Pull down Network) operate as per the logic. The schematic diagram of MTCMOS is shown in Fig. 2.

The sleep transistors are turned OFF when the sleep signal goes high and the circuit becomes idle. This way, it reduces the sub threshold leakage current by cutting OFF the power supply from V_{dd} to ground through these high V_t sleep transistors. This technique has, however, few drawbacks. First, the circuit will lose data when sleep transistors are turned OFF. Secondly, timing is critical to generate sleep signal and lastly, in large circuit, transistor sizing is a difficult task.

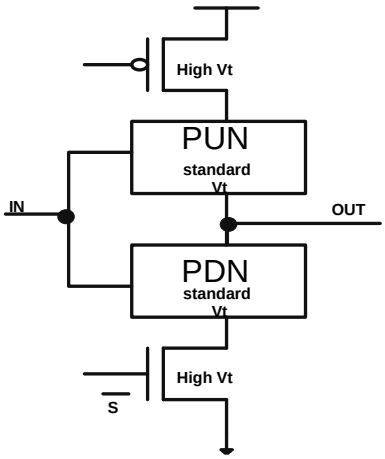

Fig. 2. Schematic diagram of Multi Threshold Logic

Leakage Reduction Scheme

Leakage Reduction Scheme uses two extra transistors called Leakage Control Transistors (LCT). These two transistors are inserted in between PUN and PDN, within the logic circuit. LCTs are connected in such a manner that transistors are always near the cutoff voltage. LCTs cause increase in path resistance from supply to ground, leading to significant leakage reduction. The schematic diagram of leakage reduction scheme is shown in Fig. 3.
However, it faces signal quality problems. It falls under the self-controlled leakage technique

because LCTs are internally biased, not externally [13].

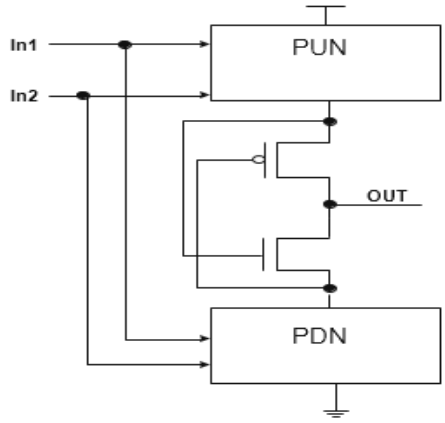

Fig. 3. Schematic diagram of Leakage Reduction Scheme

Power Reduction Technique

A PMOS LCT is located between PDN and output terminal, whereas an NMOS LCT is located between PUN and output terminal. Although provides the best leakage minimization, however, it faces a serious problem of output signal levels. The low logic signal level than 0V, and high logic signal level is very much lower than V_{dd}. It also comes under self-controlled leakage technique [14]. The schematic diagram of power reduction scheme is shown in Fig. 4.

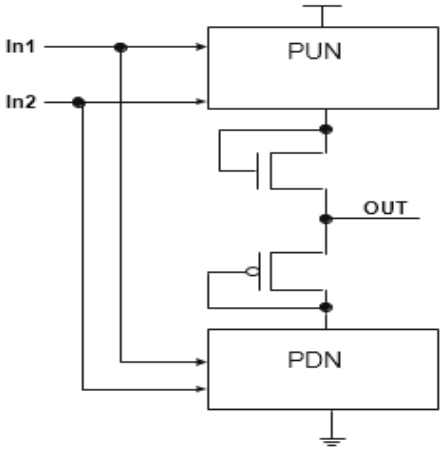

Fig. 4. Schematic diagram of Power Reduction Scheme

Leakage Current Reduction

It is based on introducing two sleep transistors (S and S) and two other helper transistors (H1 and H2) both in PUN and PDN. The sleep transistors act like header and footer, whereas the helper transistors are used to maintain logic state during sleep mode and are driven by the output of an inverter utilizing leakage feedback [14]. The schematic diagram of leakage current reduction scheme is shown in Fig. 5. During sleep mode, sleep transistors are turned OFF and one of the helper transistors in parallel to the sleep transistors keeps connection with appropriate power rail and thus retains the previous data. This approach solves the data retention problem. However, it is achieved at the cost of increase in area and propagation delay.

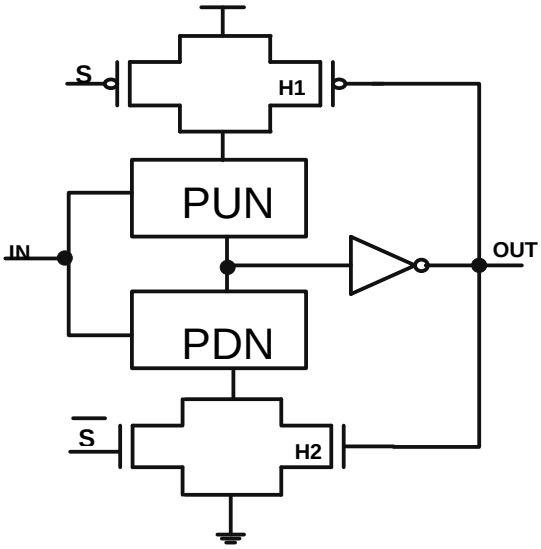

Fig. 5. Schematic diagram of Leakage Current Reduction

Drain Balance

In drain balance, leakage current can be reduced by inserting extra sleep transistors between PUN and PDN. The PMOS sleep transistor (S) is connected between PUN and output, whereas the NMOS sleep transistor ($\bar{S}$) is connected between PDN and output. During standby mode, both the sleep transistors are turned OFF thereby causing the stack effect and hence reduce the leakage current. The schematic diagram of Drain Balancing scheme is shown in Fig. 6.

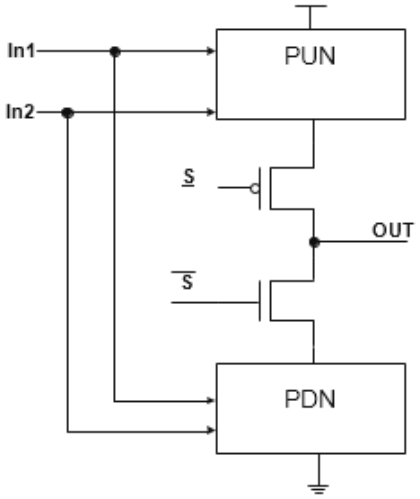

Fig. 6. Schematic diagram of Drain Balance

In active mode, both the sleep transistors are turned ON to provide the exact logic state. The disadvantage of this technique is that a separate control signal is needed to control the sleep transistors. Thus, DG comes under the scheme of externally leakage control technique [15].

Proposed Low power Design

Dynamic Threshold MOS Transistor technique is applied to the SRAM memory cell. On the analysis it is seen that this technique applied dissipates less power compared to all other SRAM cell. In the design of DTMOS, body terminal is connected to the gate terminal is a promising method for achieving enhanced performance without even modifying the existing structure of MOSFET. This is the major advantage of DTMOS as it is fully compatible with the conventional CMOS process. The technique behind the dynamic threshold MOS is that the input voltage V_{bs} is greater than Zero for NMOS and for PMOS it is negative and hence the threshold voltage can be reduced accordingly.

The DTMOS structure uses both the DTMOS gate and the body terminal are shorted V_{bs} become the function of the input signal which is applied to the gate terminal thus $V_{bs}=V_{gs}$ is maintained. Due to dynamic body bias, potential in the channel region is strongly controlled by the gate and body terminals, leading to high trans conductance owing to faster current transport. The schematic diagram of DTMOS transistor is shown in Fig. 7.

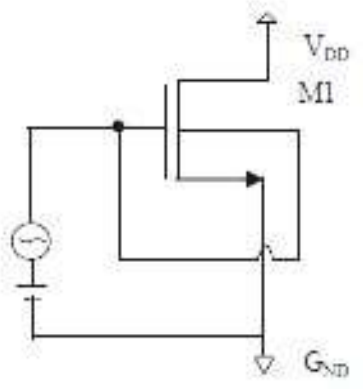

Fig. 7. Schematic diagram of DTMOS Transistor

Design of DTMOS Inverter

A dynamic threshold MOS inverter which consists of a NMOS and a PMOS transistor whose body and gate terminals are tied together. In DTMOS, body voltage varies with the gate voltage. The ability of DTMOS is that it can dynamically tune the threshold voltage (V_t) of the MOSFET for high ON current during active mode (due to low V_t caused by forward body bias) and low OFF current during standby mode (due to high V_t). Thus, it helps the designer to achieve high system performance with low power dissipation. The schematic diagram of DTMOS inverter is shown in Fig. 8.

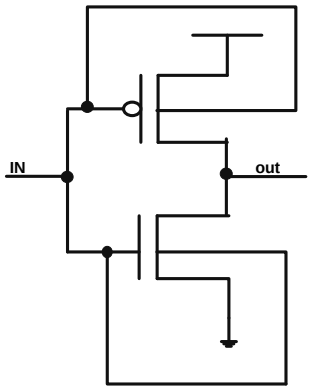

Fig. 8. Schematic diagram of DTMOS Inverter

In active mode, body–source junction is forward biased, and in standby mode, body–source junction is reverse biased. DTMOS is a popular technique to change V_t dynamically in bulk CMOS. As the DTMOS transistor turns ON, the body voltage must track the gate voltage. However, as we scale down the devices, both the body resistance and body capacitance increase which results in increase in RC time constant. This prevents the body condition favorable for fast switching which is the main drawback of the DTMOS.

Design of Proposed SRAM Memory Cell

The proposed SRAM cell consists of two inverters in which both the inverters are cross coupled. The power supply to the inverters is given in such a way that the output of the right inverter is given as an input to the left and output of the left inverter is given as an input to the right instead of V_{dd}. The schematic diagram of proposed SRAM cell is shown n Fig. 9. The power supply is given to two inverters. The word line (wl) is set as one during write operation. During standby mode, the sleep transistor is set to high, due to reverse biased condition, threshold voltage increases which leads to less power dissipation. During active mode, the sleep transistor is set to low, OFF and one of the helper transistors in parallel to the sleep transistors keeps connection with appropriate power rail and thus retains the previous data.

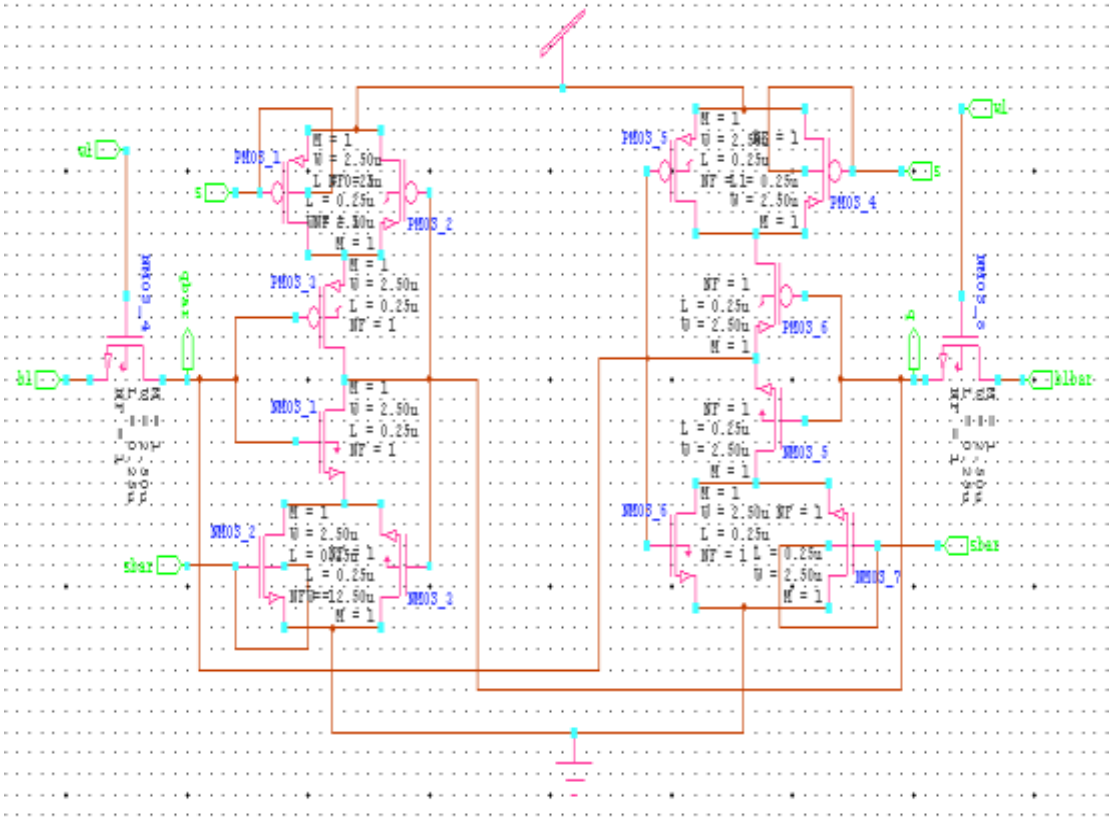

Fig. 9. Schematic diagram of proposed memory SRAM cell

Results and discussion

The tool used to design the SRAM cell is TANNER EDA tool. All the cells are simulated in 250nm technology using TSPICE library. Tool used for circuit design is S-EDIT and for simulation is W-EDIT.

Simulation Result of Proposed SRAM Memory Cell

There are five inputs namely bl, blbar, wl, s, sbar and outputs are q and qbar. For different supply voltages and input values the power dissipation value changes. The simulation results of proposed SRAM cell is shown in Fig. 10. The time period is specified in X-axis and voltage is represented in Y-axis. The word line (wl) is always given as one to perform write and read operation. The bl is given as 10 and blbar is given as 10 and the output q is same as qbar.

Power Analysis with Conventional Inverter Designs

The power dissipation of different existing technique is calculated using TANER EDA tool in 250 nm technology.

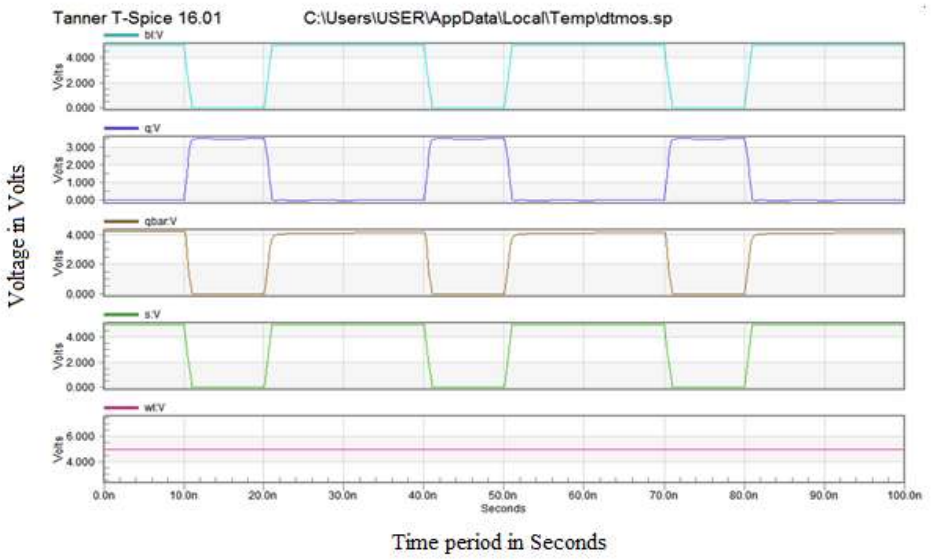

Fig. 10. Simulation result of proposed memory SRAM cell

Table 1 gives the average power dissipation of different techniques. Table 1 shows the average power dissipation of existing techniques in 250 nm technology. It is observed that the proposed technique has less power dissipation compared to the existing techniques.

Table 1. Power analysis of proposed and existing techniques for inverter designs

Different Techniques	Power dissipation in micro watts				
	1.5V	1.7V	2.1V	2.3V	2.5V
MTCMOS	1.42	1.69	2.95	3.91	5.05
Leakage Reduction	2.36	3.19	4.69	6.05	7.79
Power Reduction	1.62	2.08	3.14	3.68	5.51
Leakage Current Reduction	2.25	13.53	111	198	275
Drain Balance	0.67	2.22	2.75	4.31	7.02
Proposed SRAM	2.16	2.75	4.75	5.81	4.77

Power, Delay and PDP Analysis

The average power dissipation of 6T SRAM, Novel SRAM and proposed SRAM cell using DTMOS technique and power delay product of 6T SRAM, Novel SRAM and proposed SRAM cell using DTMOS technique are calculated using TANNER EDA TOOL in 250 nm technology. Table 2 shows the average power dissipation of proposed and existing techniques of SRAM cell. It is observed that the proposed technique reduce 33.17% of power compared to the existing technique.

Table 2. Power comparison of proposed technique with existing technique

Different Techniques	Power dissipation in micro watts				
	1.5V	1.7V	2.0V	2.3V	2.5V
6T SRAM	872	935	992	976	935
Power Reduction	416	435	444	410	374
Leakage Current Reduction	247	264	275	272	262
Drain Balance	246	263	277	271	264
Proposed SRAM	245	262	278	274	260

Table 3 shows the delay analysis of proposed and existing techniques of SRAM cell. It is observed that the proposed technique reduce 78.18% of delay compared to the conventional technique. Table 4 shows the power delay product analysis of proposed and existing techniques of SRAM cell. It is observed that the proposed technique reduce 85.55% of power delay product compared to the conventional technique. Table 2, 3 and 4 shows the average power dissipation, delay and power delay product of SRAM cell for different voltages and for different techniques in 250nm technology. The power dissipation of SRAM memory cell gets reduced due to the use of DTMOS technique. This shows greater reduction of power without performance degradation of SRAM memory cell.

Table 3. Delay comparison of proposed technique with existing technique

Different Techniques	Delay in nanoseconds				
	1.5V	1.7V	2.0V	2.3V	2.5V
6T SRAM	5.05	0.115	4.99	0.167	0.175
Power Reduction	0.093	0.136	0.137	0.110	30.11
Leakage Current Reduction	0.026	0.028	0.027	0.029	0.028
Drain Balance	0.014	0.014	0.019	0.014	0.018
Proposed SRAM	0.023	0.022	0.022	0.024	0.022

Table 4. PDP comparison of proposed technique with existing circuit

Different Techniques	Power delay product in 10^-12 J				
	1.5V	1.7V	2.0V	2.3V	2.5V
6T SRAM	4.40	0.107	4.95	0.162	0.163
Power Reduction	0.038	0.059	0.060	0.045	11.26
Leakage Current Reduction	0.0064	0.0073	0.0074	0.0078	0.0073
Drain Balance	0.0034	0.0036	0.0052	0.0037	0.0047
Proposed SRAM	0.0056	0.0057	0.0061	0.0065	0.0057

Graphical Representation

Fig. 11 shows the average power dissipation of proposed and existing techniques of SRAM cell. From the graph, it is observed that the proposed technique has minimum power than conventional SRAM cell. Fig. 12 shows the delay analysis of proposed and existing techniques of SRAM cell. From the graph, it is observed that the proposed technique has minimum delay than conventional SRAM cell. Fig. 13 shows the power delay product analysis of proposed and existing techniques of SRAM cell. From the graph, it is observed that the proposed technique has minimum power delay product than conventional SRAM cell.

Fig. 11, 12 and 13 shows the average power dissipation, delay and power delay product of SRAM memory cell for different voltage levels in 250nm technology. The graph clearly shows the power dissipation, delay and PDP of different SRAM memory cell. This shows greater reduction of power without performance degradation of SRAM memory cell.

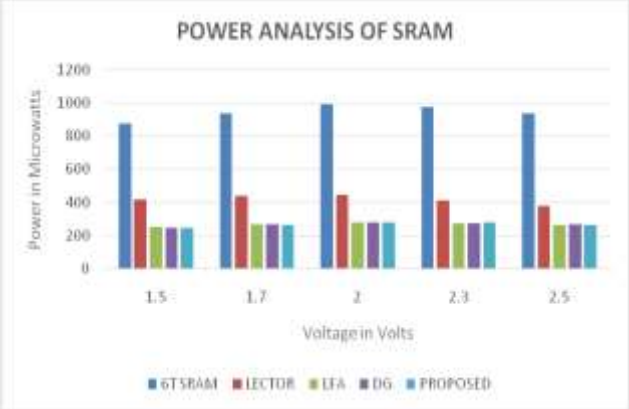

Fig. 11. Power comparison between DTMOS and existing techniques

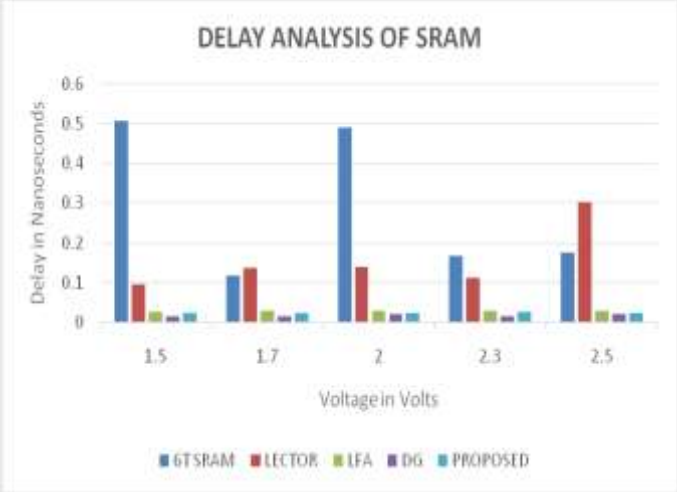

Fig. 12. Delay comparison between DTMOS and existing techniques

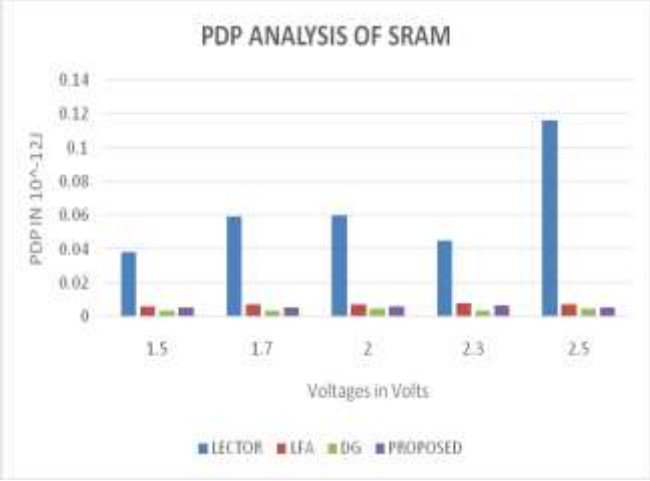

Fig. 13. PDP comparison between DTMOS and existing techniques

Conclusions

Power, area, and delay are the major aspects of VLSI industry. Thus the power optimized SRAM cell were designed using DTMOS technique. In this paper, the proposed SRAM cell reduce leakage power, delay and power delay product. Simulation results explores that the proposed technique has achieved leakage reduction up to 33.17% on average, delay improvement of 78.18% and power delay product of 85.55% compared to the conventional techniques. Thus SRAM cell by dynamic threshold MOS transistor was designed using TANNER EDA tool in 250nm technology. In modern day processor power dissipation plays a major role because of the miniaturization of chip design. So this DTMOS technique can be used in future for reducing the power dissipation in memory cell. Since cost and size of DRAM cells are less compared to SRAM cells but power is only disadvantage of DRAM so these power can be optimized by using SRAM cell. The power optimized SRAM cell can be used to replace a conventional structure for low power VLSI application. It can be used in personal computers, work stations, routers and peripheral equipments like CPU register files, hard disk buffers, router buffers, etc. In future, the proposed method can be experimented with the latest technologies.

Conflicts of Interest

Authors declare no conflict of interest.

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