Analysis and Characterization of HighSpeed CMOS Voltage Comparator

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Abstract- This paper presents detail analysis and characterization of High Speed CMOS Comparator for High Performance Applications like ADCs. In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high speed applications. In this high speed low power, low voltage era there is an increasing demand of a High Speed Comparator for ADC, DAC and various applications in analog and digital domain. Comparator is the main building block in ADC architecture. Various types of Dynamic Latch Comparators which includes Resistive DividingComparator, Current Sensing Comparator, Charge Sharing Comparator and ModifiedHigh Speed CMOS Voltage Comparators simulated for the differentcharacteristics in different CMOS Technologies. In the new design two pMOS transistors were added in the differential current sensing comparator architecture to resolve the problem associated with previous code dependent biased decision which occurs due to the charge imbalance left from previous decision at one of the nodes of the comparator which affects next decision is thus removed. This new architecture showed low power dissipation and high speed as compared to other architectures.

Keywords- Analog to Digital Converters (ADCs), Propagation delay, Offset Voltage, Power Dissipation, CMOS Comparator

I. INTRODUCTION

The schematic symbol and basic operation of a voltage comparator are shown in figure 1, this comparator can be thought of as a decision making circuit.

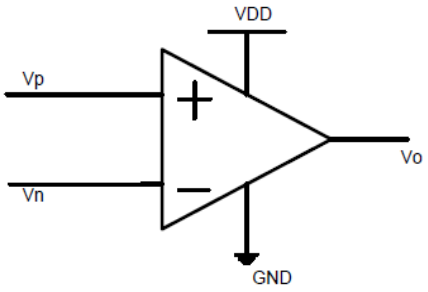


Fig.1: Circuit Symbol for a Comparator

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. VP is the input voltage applied to the positive input terminal of comparator and VN is the reference voltage applied to the negative terminal of the comparator. If the VP, the input of the comparator is at a greater potential than the VN, input, the output of the comparator is at logic '1' where as if VP is at potential less than VN the output of the comparator is at logic '0'

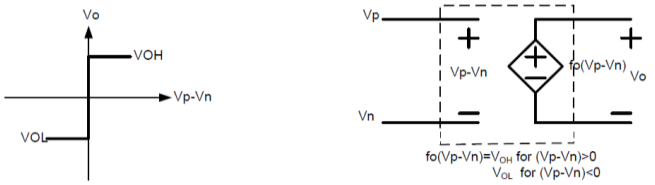
If $V_P \geq V_N$, then V_o = logic '1'.
If $V_P < V_N$, then V_o = logic '0'.

An analog signal is one that can have any of a continuous of amplitude values at a given point in time. In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region. The comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, like sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast [1].

In recent years, the demand for portable devices with high speed and low power is increasing. In this high speed, low power era there is increasing demand of high speed comparators for ADC, DAC, zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission etc. High speed applications and technology is becoming an increasingly important and growing area of electronics. Comparator is the main building block in ADC architecture. Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. Due to low-offset, fast speed, low power consumption, high input impedance, CMOS dynamic latched comparator are very attractive for many applications such as high speed analog-

to-digital convertors (ADCs), memory sense amplifiers (SAs) and data receivers.

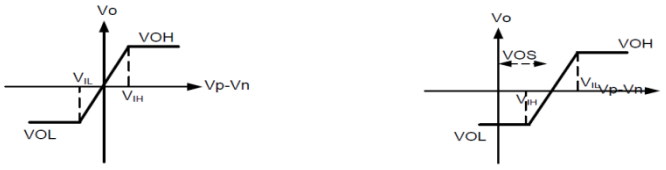
A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Figure 3.1. The output of the comparator is high (VOH) when the difference between the non-inverting and inverting inputs is positive, and low (VOL) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modelled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Figure3.2 comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the Figure 2.



(a) (b)

Fig.2: (a) Ideal Transfer curve of a Comparator (b) Model for an ideal Comparator

The gain of the comparator is the derivative of the dc transfer curve at VI ~VR. The transfer curve of an ideal comparator with infinite gain is as shown in Figure 2. The second non ideal effect seen in comparator circuits is input-offset voltage, Vos. In Figure 2 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value +Vos, then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit [16] for a given design.

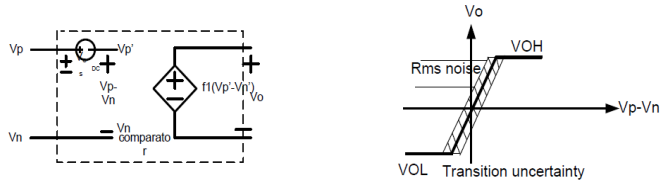


(a) (b)

Fig.3: (a) Transfer curve of a comparator with infinite gain (b) Transfer curve of a comparator including input - offset voltage

Figure 3 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Figure 3. The sign of the offset voltage accounts for the fact that Vos is unknown in polarity.

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. All these aspects can be modelled in the same manner as was done for the Op-amp. Because the input to the comparator is usually differential, the input common-mode range is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation. Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modelled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Figure 4. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.



(a) (b)

Fig.4: (a) Model for a comparator including Input-offset voltage. (b) Influence of noise on a Comparator

The dynamic characteristics of the comparator include both small-signal and large-signal behaviour. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 5 illustrates the response of a comparator to an input as a function of time. Note that there is a delay between the input excitation and the output response. This time difference is called the propagation delay time of the comparator. It is a very important parameter since it is often the speed limitation in the conversion rate of an A/D Converter. The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which further increase in the input voltage will no longer affect the delay. This mode of operation is called slewing or slew rate [1] [2]. The small-signal dynamics are characterized by the frequency response of the comparator. A simple model of this behavior assumes that the differential voltage gain, Av, is given as

$$Av(S) = \frac{Av(0)}{\frac{S}{Wc} + 1} = \frac{Av(0)}{S\tau c + 1} ----(1)$$

Where Av(0) is dc gain of the comparator and Wc = 1/τc is the -3 dB frequency of the single (dominant) pole approximation to the comparator frequency response. Normally, the Av(0) and WC of the comparator are smaller and larger, respectively, than for an op-amp

Let us assume that the minimum change of voltage at the input of the comparator the resolution of the comparator. We will define this minimum input voltage to the comparator as

$V_{in(min)} = V_{OH} - V_{OL}/ Av(0)$ -----(2)

For a step input voltage, the output of the comparator modelled by Equation 1 rises (or falls) with a _rst-order exponential time response from VOL to VOH (or VOH to VOL). If Vin is larger than Vin(min), the output rise or fall time is faster. When Vin(min) is applied to the comparator, we can write the following equation

$\frac{VOH-VOL}{2}$ = Av(0)[1 - $e^{\frac{Tp}{Tc}}$] $Vin(min)$ = Av(0)[1 - $e^{\frac{Tp}{Tc}}$](V_{OH} – V_{OL}/ Av(0)) -------(3)

Therefore, the propagation delay time for an input step of Vin(min) can be expressed as
tp(max) = τcln2 = 0:693τc ----(4)

This propagation delay time will be valid for either positive-going or negative-going comparator outputs. The propagation delay time is given as
tp =τc ln 2k/(2k-1) --------(5)
where k = (V_{in}/$V_{in(min)}$) Vin
Obviously, the more overdrive applied to the input of this comparator, the smaller the propagation delay time. As the overdrive increases to the comparator eventually the comparator enters a large signal mode of operation. Under large-signal operation, a slew-rate limit will occur due to limited current to charge or discharge capacitors.

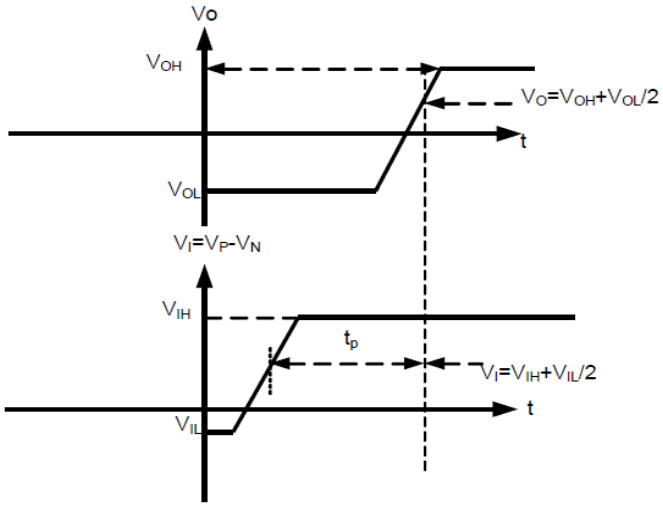
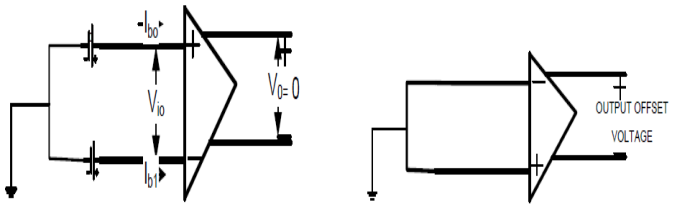


Fig.5: Propagation Delay time of a Non-inverting Comparator

The input offset can be minimized or ignored by proper layout. If the input step is sufficiently small the output should not slew, and the transient response will be a linear response. The settling time is the time needed for the output to reach a finalvalue within a predetermined tolerance, when excited by a small signal. Small-signal settling time is determined by the gain bandwidth product of the amplifier; this will be shown in the op-amp circuit section later. If the input step magnitude is sufficiently large, the comparator will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. Slew rate is limited by the current-sourcing/sinking capability in charging the output capacitor. Settling time is important in analog signal processing. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.
The ideal operational amplifier shown in Figure 6 is perfectly balanced, that is, Vo = 0 when V1 = V2. A real operational amplifier exhibits an unbalance caused by a mismatch [3] of the input transistors. This mismatch results in unequal bias currents owing through the input terminals, and also requires that an input offset voltage be applied between the two input terminals to balance the amplifier output. In this section the dc error voltages and currents that can be measured at the input and output terminals are discussed.



(a) (b)

Fig.6: (a) Input Offset Voltage (b) Output Offset Voltage

Input Bias Current: The input bias current is one-half the sum of the separate currents entering the two input terminals of a balanced amplifier as shown in Figure 6 the input bias current is IB = (IBl + IB2) /2 when Vo = 0.
Input Offset Current: The input offset current is the difference between the separate currents entering the input terminals of a balanced amplifier. As shown in Figure 6, we have Iio = IB1 - IB2 when Va = 0.
Input Offset Current Drift: The input offset current drift ΔIio/ΔT is the ratio of the change of input offset current to the change of temperature.
Input Offset Voltage: The input offset voltage Via is that voltage which must be applied between the input terminals to balance the amplifier, as shown in Figure 6.
Input Offset Voltage Drift: The input offset voltage drift ΔVi/ΔT is the ratio of the change of input offset voltage to the change in temperature.
Output Offset Voltage: The output offset voltage is the difference between the dc voltages present at the two output terminals (or at the output terminal and ground for an amplifier with one output) when the two input terminals are grounded
Power Supply Rejection Ratio: The power supply rejection ratio (PSRR is the ratio of the change in input offset voltage to the

corresponding channel in one power supply voltage, with all remaining power supply voltage constant.
Slew Rate: The slew rate is the time rate of change of the closed loop amplifier output voltage under large-signal conditions.

II. Existing Architectures of Differential Dynamic Comparator

The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. The output buffer is also known as post amplifier which accepts differential input signals. For a simple design for the output buffer, we can use the self biased differential amplifier.

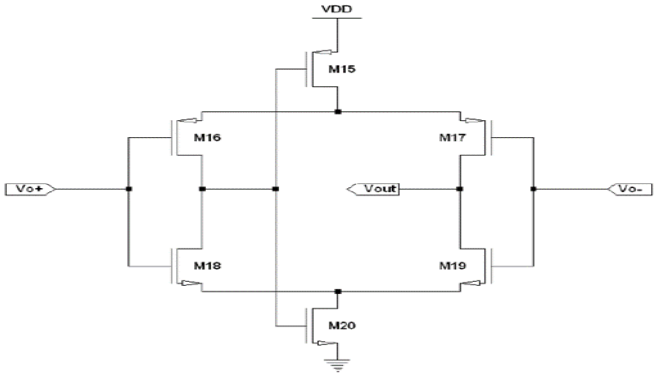


Fig.7: Self Biased Differential Amplifier

The circuit configuration of this amplifier differs from those of conventional CMOS differential configurations in two ways:

1. The amplifiers are completely complementary, i.e. each nMOS device operates in push pull fashion with a corresponding pMOS
2. The amplifiers are self biased through negative feedback.

These two differences in the amplifier configurations results in several performance enhancement:
1. Less sensitivity of active region biasing to variations in processing, temperature and supply.
2. Capability of supplying switching currents that is significantly greater than the quiescent bias current.

These performance enhancements are desirable in comparator applications where precision, high speed, ease of interfacing to logic gates and high production yields are required. This amplifier consists of two differential amplifiers each serving as the load for the other**.** The tail current of the amplifier becomes adaptive by connecting thegates of M19 and M20 to the drains of M16 and M17. This self biasing of the amplifier creates a negative feedback loop that stabilizes the bias voltages. The transistors M19 and M20 operates in linear region, so the voltages at the drain of both the transistors may be set very close to the supply voltages. Since these two voltages determine the output swing of the amplifier, the output swing can be very close to the difference between the two supply rails.

a. Resistive Dividing Comparator

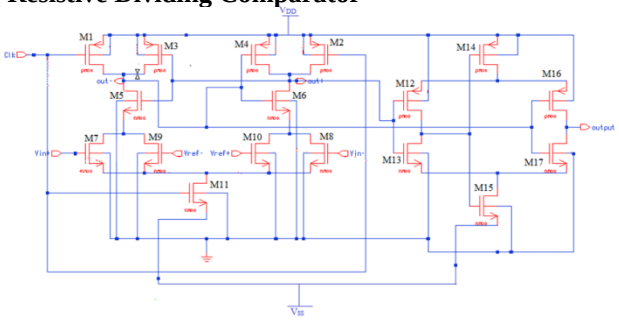


Fig.8: Schematic of Resistive Dividing Comparator

The Resistive Dividing Comparator was introduced in [5]. shows the circuit diagram of comparator consisting of resistive dividing network and output buffer stage. The two ended output of the resistive dividing comparator are Vout+ & Vout-. Both the outputs of the comparator are inputs to the buffer. Thus, the two ended output of resistive dividing comparator is being converted into single ended output for different types of analysis. The input transistors M7, M9, M10 and M8 operate in triode region and acts like voltage controlled resistors, R1 and R2, this comparator is called "Resistive Dividing Comparator". The advantage of this comparator is its low power consumption (No DC power consumption) and adjustable threshold voltage (decision level) which is defined as

$$V_{in}(\text{threshold}) = (W_B/ W_A)\ Vref$$

Where $W_A = W_7 = W_8$ and $W_B = W_9 = W_{10}$

$$V_{in} = V_{in+} - V_{in-} \text{ and } V_{ref} = V_{ref+} - V_{ref-}$$

The circuit works in regenerative mode when the Clk signal goes high. As the Clk is high the nMOS transistor M9 are on and the pMOS transistors M6 and M13 will be off. In regenerative mode the circuit compares the input voltages with the help of transistors which will be operated in triode region. The circuit is in reset mode when the Clk signal goes low. As the Clk is low nMOS transistor M9 is off and hence circuit will get disconnected from the VSS. At the same time, pMOS transistors M13 and M6 are on and hence the outputs will be pre-charged up to VDD. The advantage of using a differential input pair is the ease in the adjustment of the threshold voltage by changing the transistor widths instead of changing reference voltages.

b. Differential Current Sensing Comparator

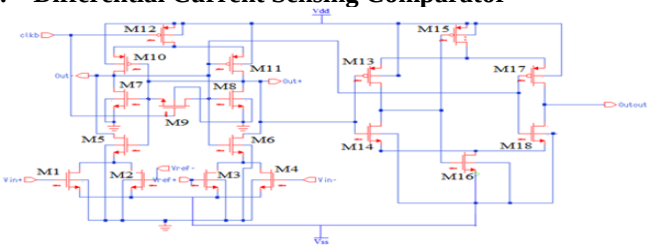


Fig.9: Schematic of Differential Current Sensing Comparator

The Differential Current Sensing Comparator was introduced in [5]. Whenever the Clk signal goes low the circuit enters in regenerative mode. Transistor M12 is on and M7 is off. When values of both the outputs Out+ and Out- increases above threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side. It consumes more power because unless and until final state is reached both the outputs have to drive common mode currents.The comparing circuit used at the input side consisting of transistors M1, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M7 is used to connect both the outputs together. The two outputs Out+ and Out- of differential current sensing comparator are being converted into single output with the output buffer circuit so that various analysis can be carried out

c. Charge Sharing Dynamic Latch Comparator

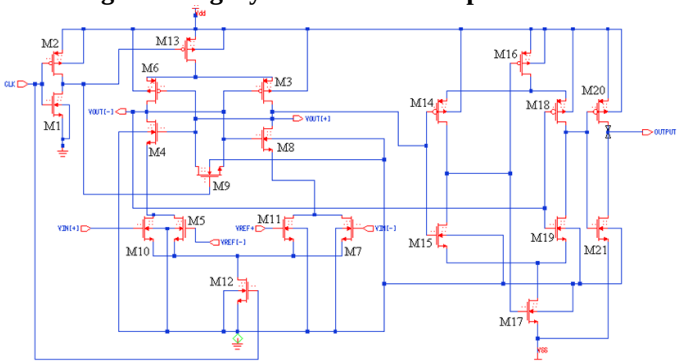


Fig.10: Schematic of Charge Sharing Dynamic Latch Comparator

This topology combines the good features of the other two of dynamic latch comparator that suitable with pipeline A/D converters which is resistive dividing comparator and differential current sensing comparator [2]. The nMOS transistor M12 is used in series with resistive comparing circuit for regenerative mode in order to achieve low power. For reset mode pMOS pre charging circuit is absent and nMOS transistor M9 for output pass transistor for the equalization of both the voltages nearly to Vdd/2. Now, when the clock goes low, Vdd and ground both will be disconnected from the latch with the help of transistors M12 & M3. The two ended output of the dynamic charge sharing comparator are Vout+ & Vout-. Both the outputs of the comparator are inputs to the buffer. Thus, the two ended output of dynamic charge sharing comparator is being converted into single ended output for different types of analysis.

III. Modified High Speed CMOS Voltage Comparator

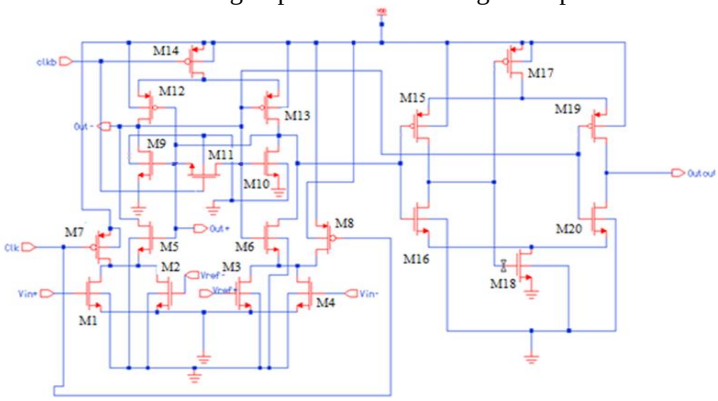


Fig.11: Schematic of Modified High Speed CMOS Voltage Comparator

Whenever the Clk signal goes high, the circuit enters in regenerative mode. Transistor M11 and M7 are off and M14 is on. When values of both the outputs Out+ and Out- increases above threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side.

The comparing circuit used at the input side consisting of transistors M1, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M11 is used to connect both the outputs together. Whenever the Clk signal goes low, transistor M7 and M8 are on. The two nodes which relate to the drains of M7 and M8 will get reset to Vdd. These internal nodes are reset to Vdd during the phase when the comparator is not deciding. This will ensure that all the internal nodes are reset before the comparator goes into decision mode. So, the problem associated with previous code dependent biased decision which occurs due to the charge imbalance left from previous decision at one of the nodes of the comparator which affects next decision is thus removed. The two outputs Out+ and Out- of the comparator are being converted into single output with the output buffer circuit so that various analysis can be carried out.

IV. SIMULATION RESULT

a. Simulation Results of Resistive Dividing Comparator

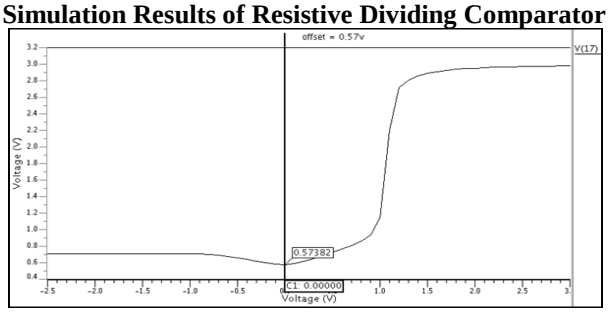


Fig.12: Offset Voltage in TSMC 0.35µm Technology

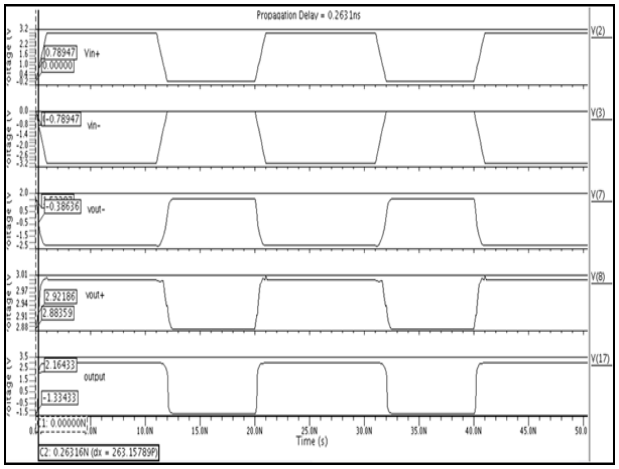


Fig.13: Transient Response in TSMC 0.35µm Technology

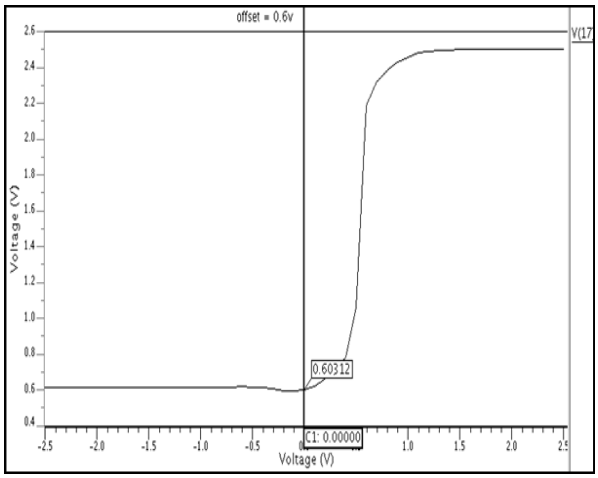


Fig.14: Offset Voltage in TSMC 0.25µm Technology

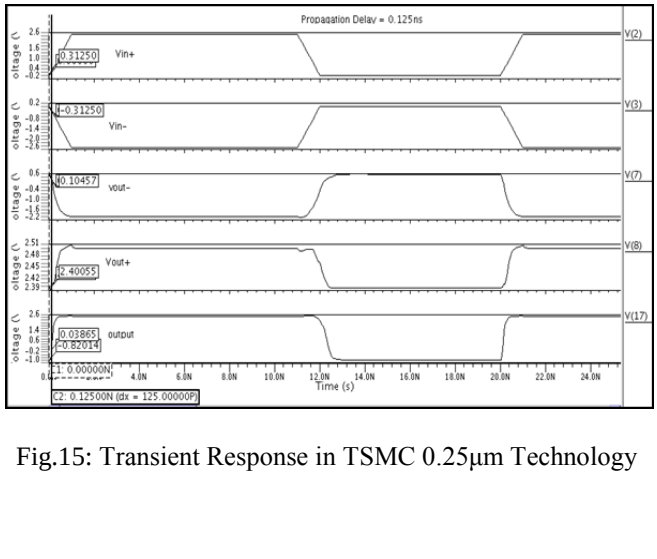


Fig.15: Transient Response in TSMC 0.25µm Technology

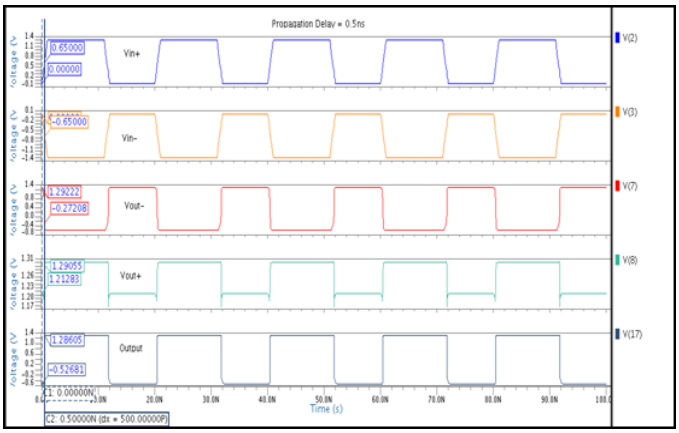


Fig.16: Transient Response in Generic 130nm Technology

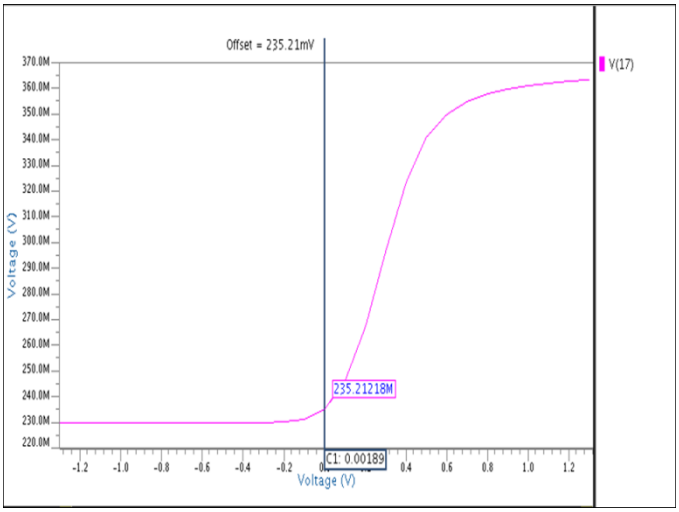


Fig.17: Offset Voltage in Generic 130nm Technology

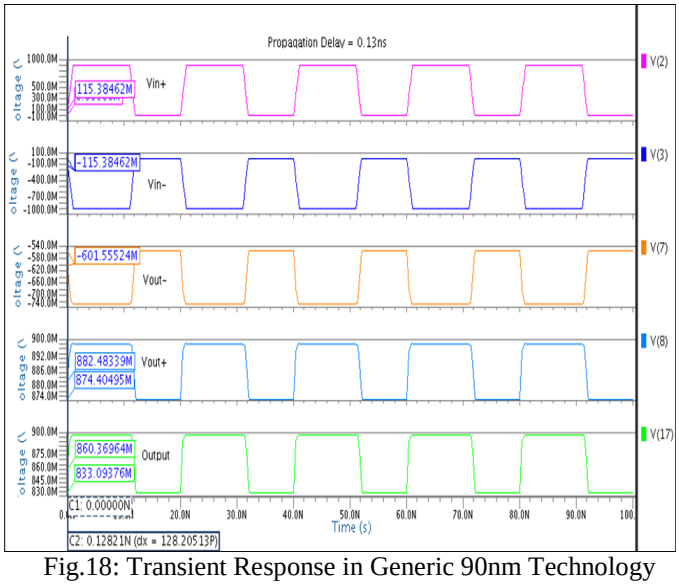


Fig.18: Transient Response in Generic 90nm Technology

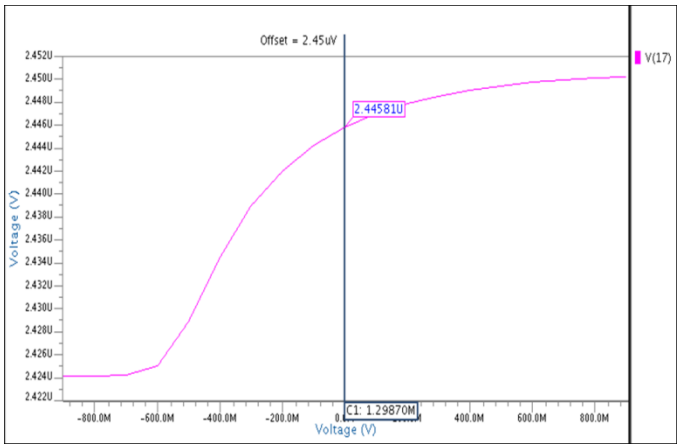


Fig.19: Offset Voltage in Generic 90nm Technology

b. Simulation Results of Differential Current Sensing Comparator

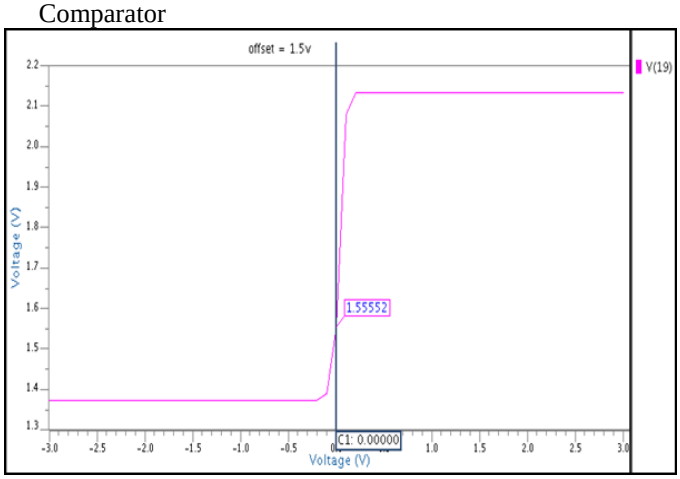


Fig.20: Offset Voltage in TSMC 0.35µm Technology

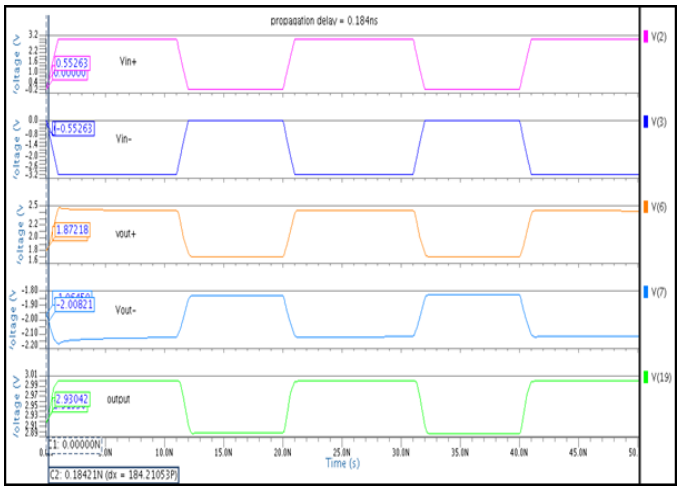


Fig.21: Transient Response in TSMC 0.35µm Technology

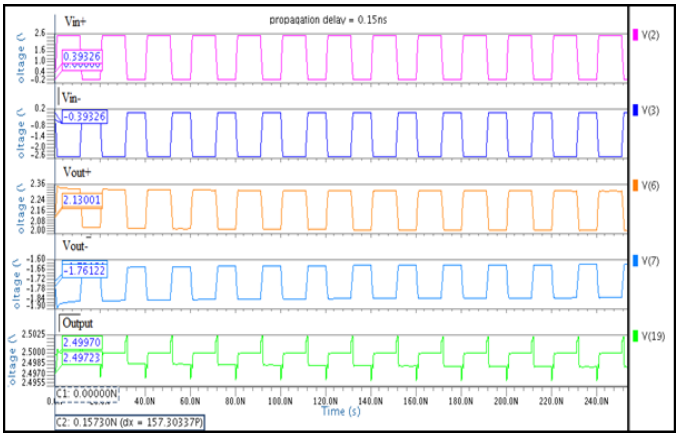


Fig.22: Transient Response in TSMC 0.25µm Technology

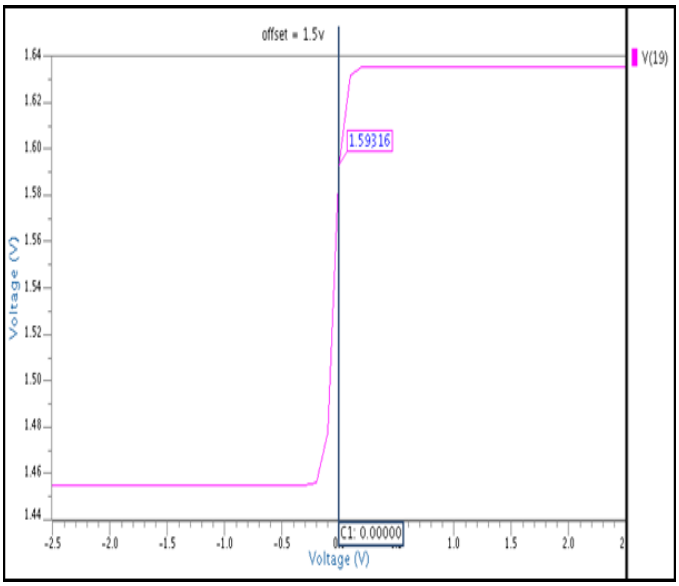


Fig.23: Offset Voltage in TSMC 0.25µm Technology

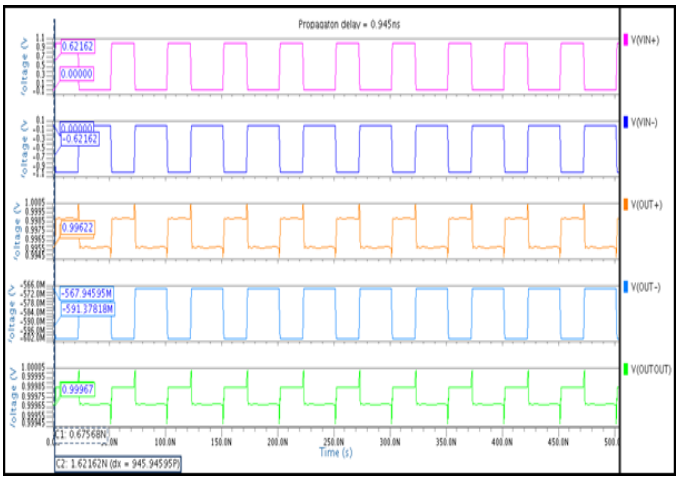


Fig.24: Transient Response in Generic 130nm Technology

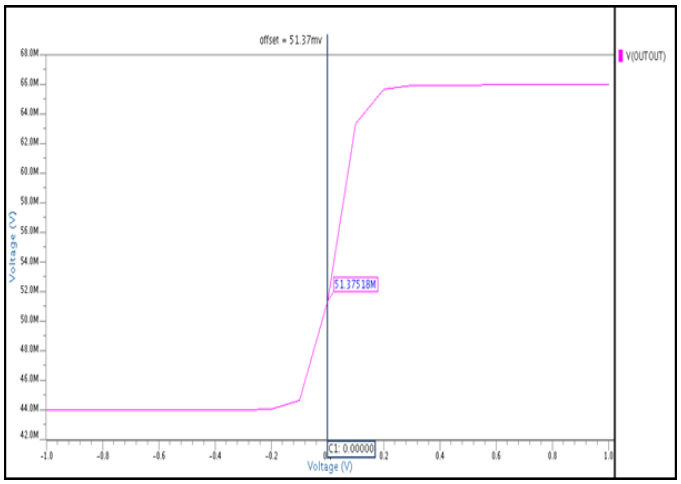


Fig.25: Offset Voltage in Generic 130nm Technology

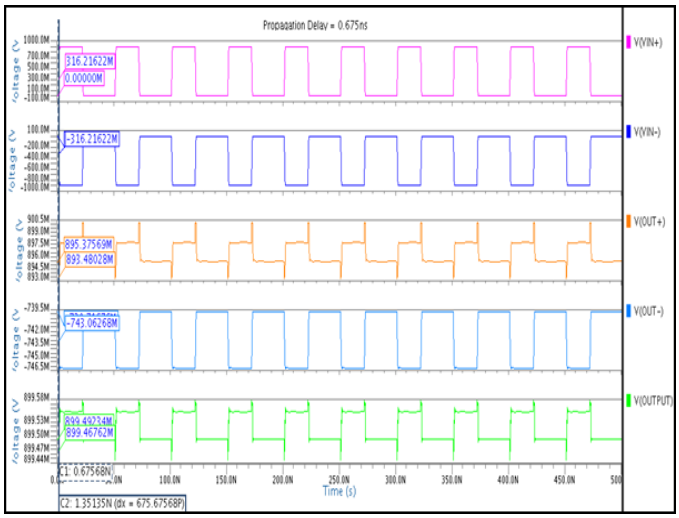


Fig.26: Transient Response in Generic 90nm Technology

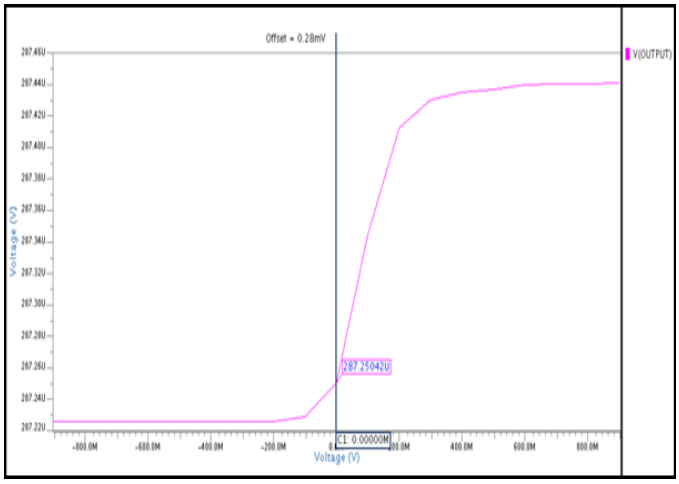


Figure 27. Offset Voltage in Generic 90nm Technology

c. Charge Sharing Dynamic Latch Comparator

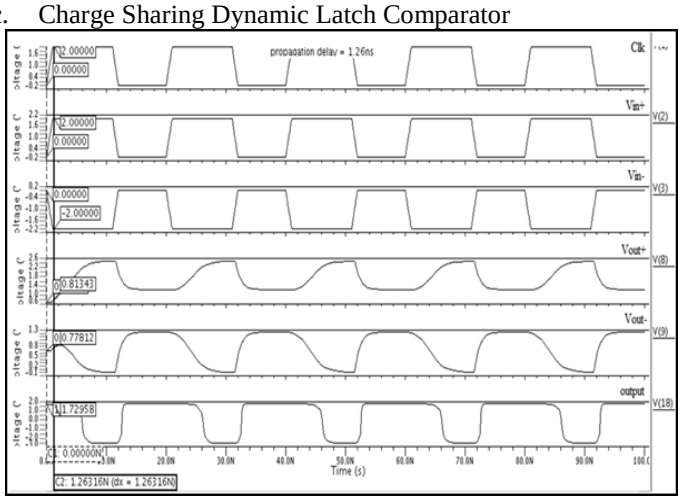


Fig.28: Transient Response in TSMC 0.35µm Technology

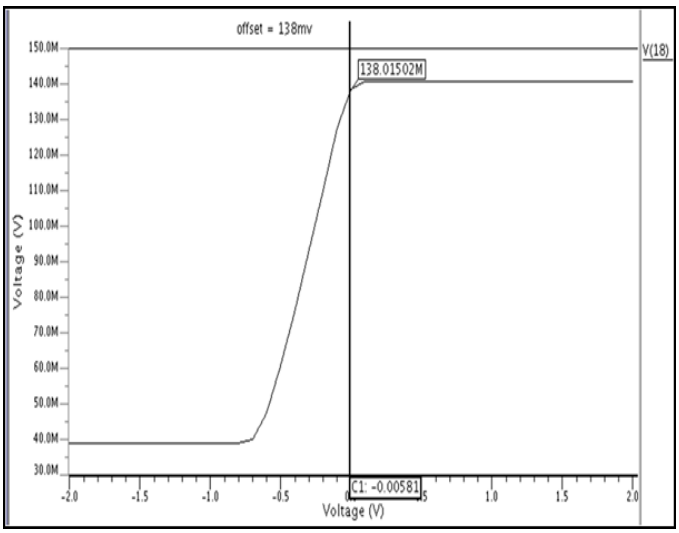


Fig.29: Offset Voltage in TSMC 0.35µm Technology

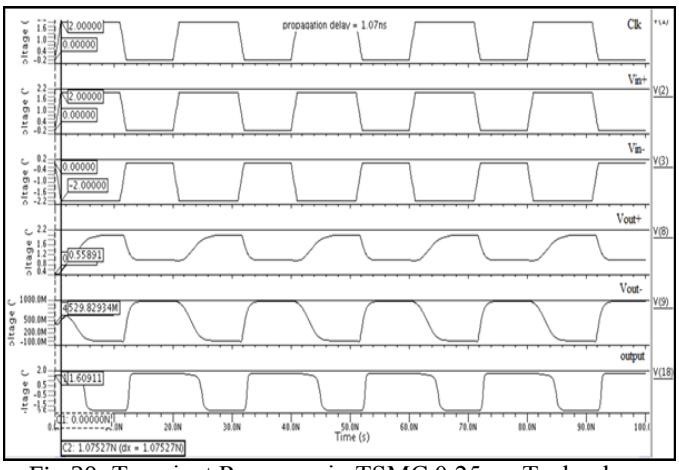


Fig.30: Transient Response in TSMC 0.25µm Technology

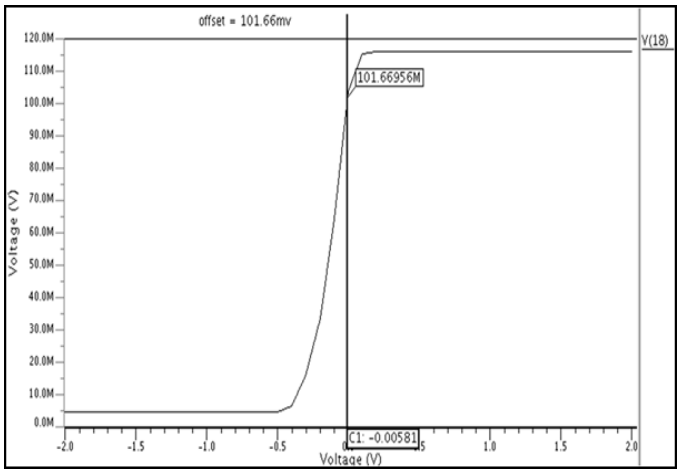


Fig.31: Offset Voltage in TSMC 0.25µm Technology

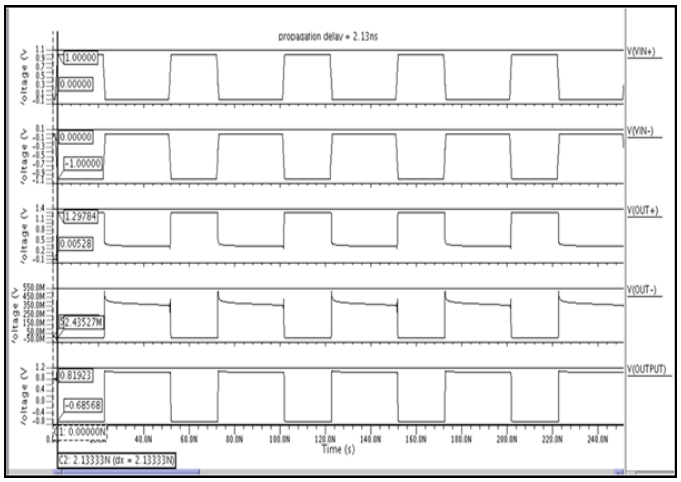


Fig.32: Transient Response in Generic 130nm Technology

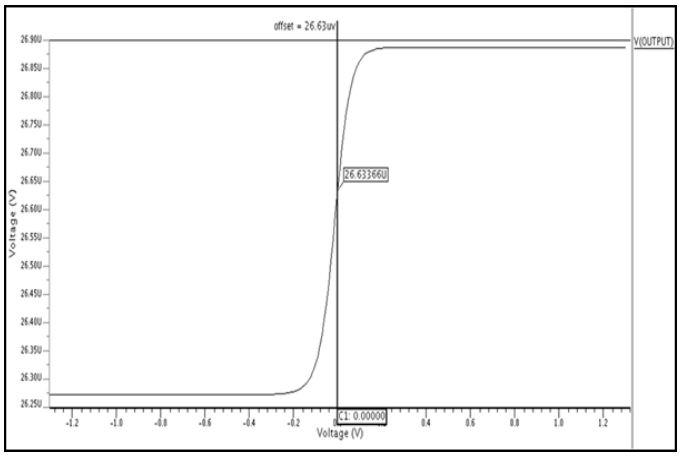


Fig.33: Offset Voltage in Generic 130nm Technology

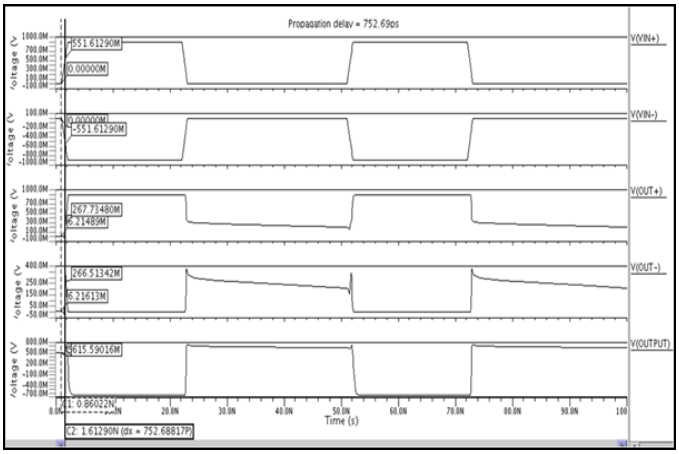


Fig.34: Transient Response in Generic 90nm Technology

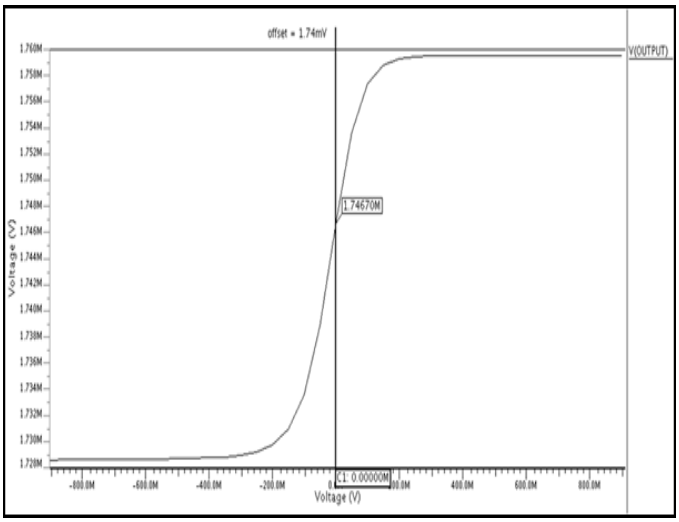


Fig.35: Offset Voltage in Generic 90nm Technology

d. Modified High Speed CMOS Voltage Comparator

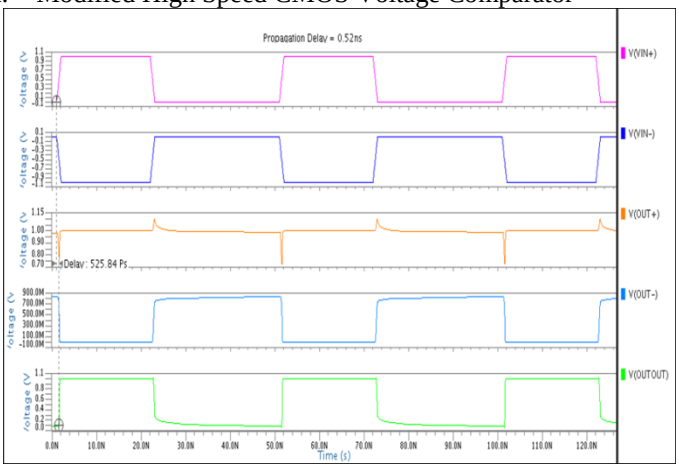


Fig.36: Transient Response in Generic 130nm Technology for Typical Transistor (TT)

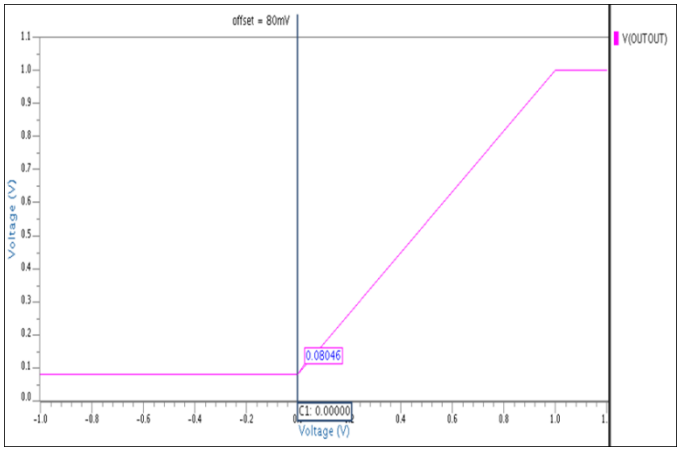


Fig.37: Offset Voltage in Generic 130nm Technology for Typical Transistor (TT)

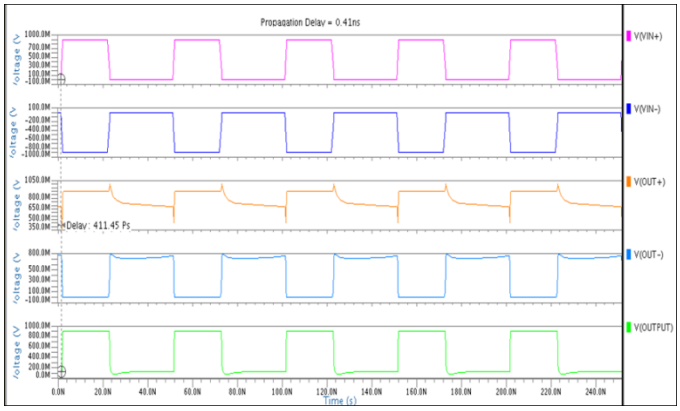


Fig.38: Transient Response in Generic 90nm Technology for Typical Transistor (TT)

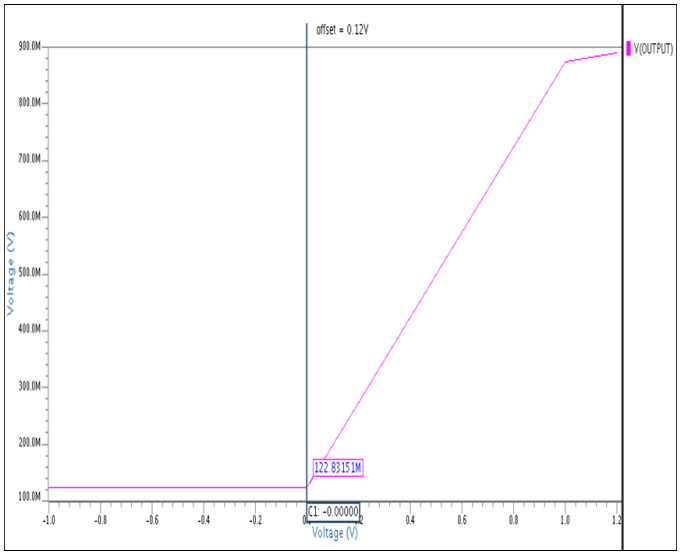


Fig.39: Offset Voltage in Generic 90nm Technology for Typical Transistor (TT)

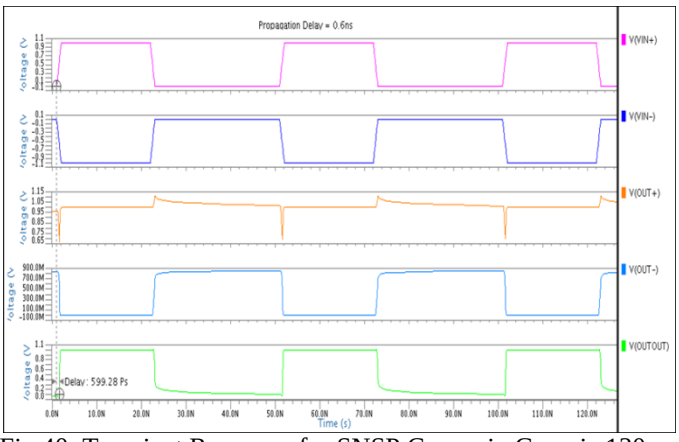


Fig.40: Transient Response for SNSP Corner in Generic 130nm Technology

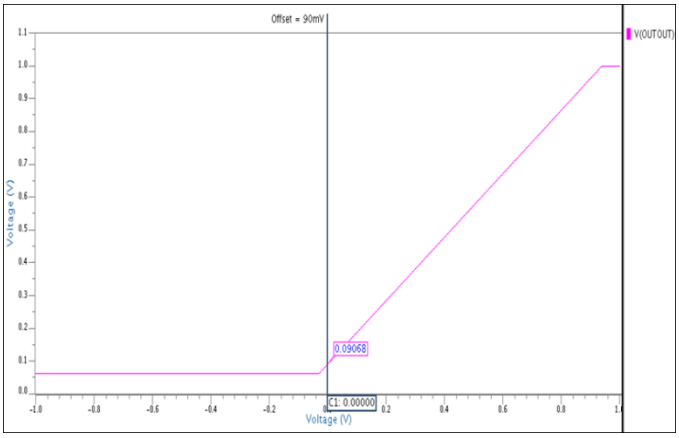


Fig.41: Offset Voltage for SNSP Corner in Generic 130nm Technology

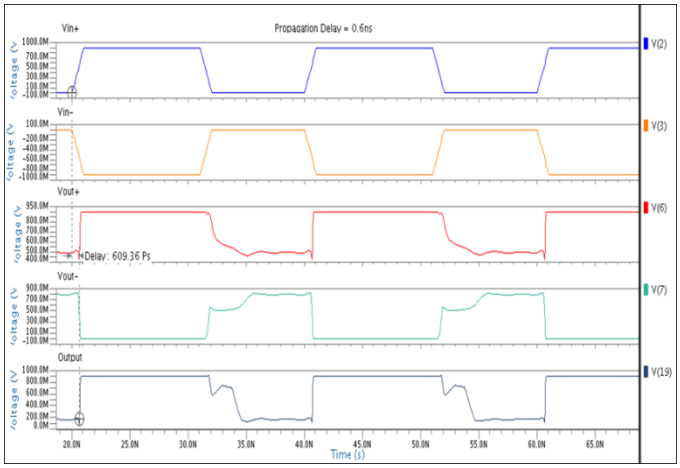


Fig.42: Transient Response for SNSP Corner in Generic 90nm Technology

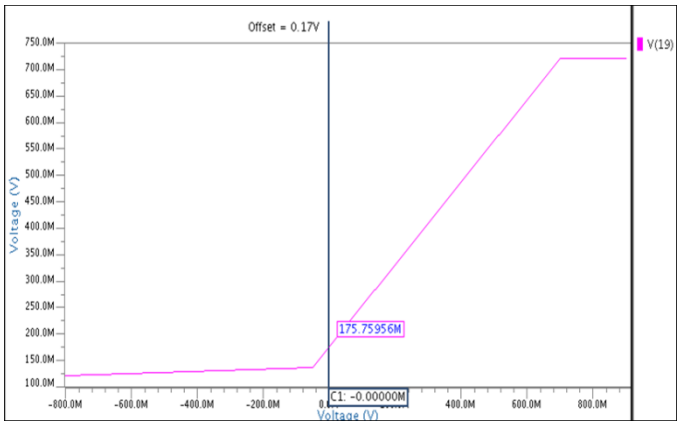


Fig.43: Offset Voltage for SNSP Corner in Generic 90nm Technology

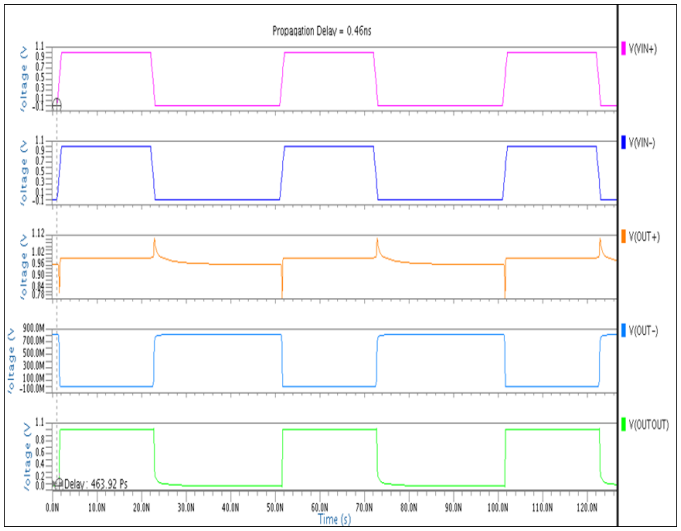


Fig.44: Transient Response for FNFP Corner in Generic 130nm Technology

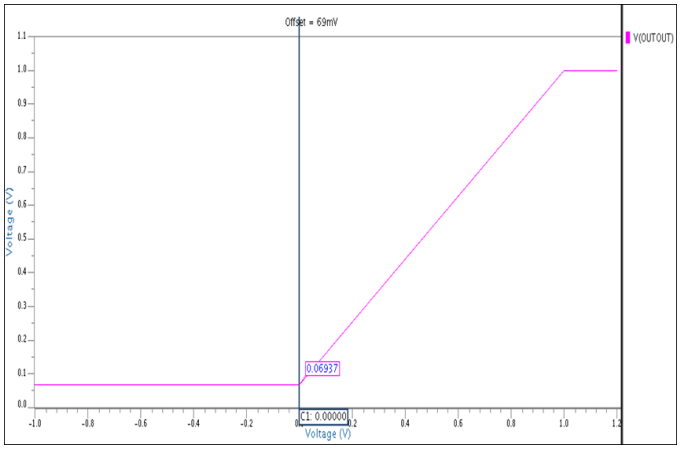


Fig.45: Offset Voltage for FNFP Corner in Generic 130nm Technology

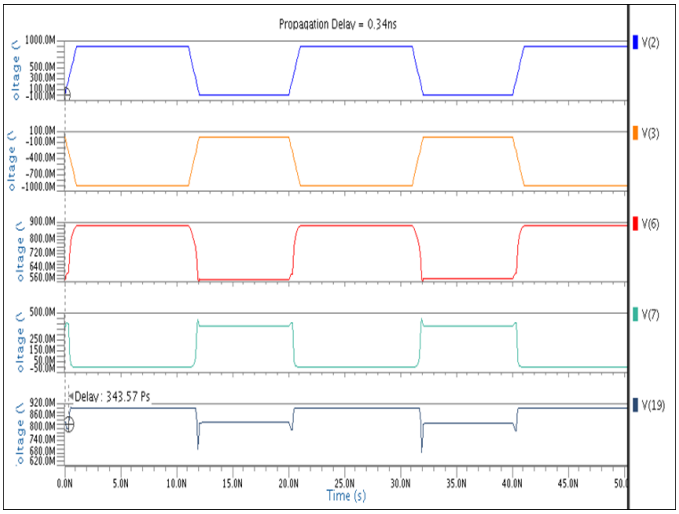


Fig.46: Transient Response for FNFP Corner in Generic 90nm Technology

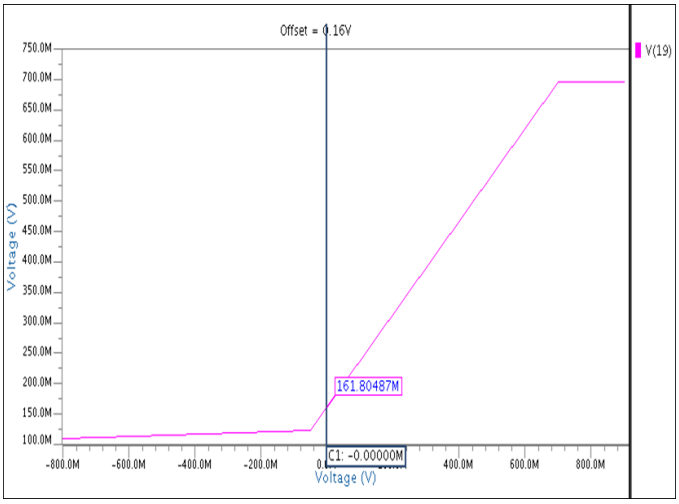


Fig.47: Offset Voltage for FNFP Corner in Generic 90nm Technology

V. CONCLUSION

In this paper, various architectures of comparator suitable for high speed applications have been characterized and simulated. The comparator is designed in TSMC 0.35um, 0.25umand in Generic 130nm and 90nm technologies.The comparator is characterized in terms of the offset, propagation delay, ICMR, power dissipation. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as offset voltage, speed, power for A/D Converters.

VI. REFERENCES

[1]. Philip E. Allen and Douglas R. Hallberg. CMOS Analog Circuit Design. Oxford University Press, Inc USA-2002, pp.259-397,.

[2]. R. Jacob Baker Harry W. Li David E. Boyce. CMOS Circuit Design, Layout and Simulation. IEEE Press Series on Microelectronics Systems, 2005.

[3]. J. Millmand and C. C. Halkies. Integrated Electronics: Analog and Digital Circuits and Systems. McGrawHill, New York, 1972.

[4]. M. Bazes. "Two novel fully complementry self-biased cmos differential amplifiers". IEEE Journal of Solid-State and Circuits, vol. 26,pp. 6134-6137, February 1991.

[5]. P. Uthaichana and E. Leelarasmee, "Low Power CMOS Dynamic Latch Comparators," IEEE, pp. 605-608, 2003.

[6]. HeungJun Jeon and Yong-Bin Kim "A Low-offset High-speed Double-tail Dual-rail Dynamic Latched Comparator" ,IEEE 2004.

[7]. Vipul Katyal, Randall L. Geiger and Degang J. Chen "A New High Precision Low Offset Dynamic Comparator for High Resolution High Speed ADCs", IEEE 2006.

[8]. Bernhard Goll and Horst Zimmermann "A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V", IEEE Transactions on Circuits And Systems—II: Express Briefs, Vol. 56, No. 11, Nov. 2009.

[9]. HeungJun Jeon and Yong-Bin Kim " A CMOS Low Power Low Offset and High Speed Fully Dynamic Latched Comparator", IEEE,2010.

[10]. Jian-feng Wang Ji-hai Duan, " Design of An Ultra High-Speed Voltage Comparator", Second Pacific-Asia Conference on Circuits Communications and System (PACCS), 2010.

[11]. Paul M. Furth, Yen-Chun Tsen, Vishnu B. Kulkarni and Thilak K. Poriyani "On the Design of Low-Power CMOS Comparators with Programmable Hysteresis.", IEEE,2010

[12]. Shairah Abdul Halim, Nurul Aisyah Nadiah Binti Zainal Abidin, A'zraa Afhzan Ab Rahim " Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18µm Technology",IEEE,2011.

[13]. Anh T. Huynh, Chien M. Ta, Praveen Nadagouda, Robin J. Evans, and Efstratios Skafidas " A 7GHz 1mV-Input-Resolution Comparator With 40mV-Input-Reffered-Offset Compensation Capability in 65nm CMOS",IEEE,2011.

[14]. Li Zhang, "A High-speed Comparator for a 12-bit 100MS/s Pipelined ADC", Fourth International Conference on Intelligent Computation Technology and Automation, 2011.

[15]. D. lackuline Moni and P. Lisha "High-Speed and Low-Power Dynamic Latch Comparator", IEEE, 2012.

[16]. HeungJun Jeon and Yong-Bin Kim "Low-Power, Low-Offset, and High-Speed CMOS Dynamic Latched Comparator" Analog Integrated Circuit Signal Process (2012) 70:337–346

[17]. Wan Rosmaria Wan Ahmad, Siti Lailatul Mohd Hassan, Ili Shairah Abdul Halim, Noor Ezan Abdullah and Ifzuan Mazlan, "High Speed With Low Power Folding And Interpolating ADC Using Two Types of Comparator in CMOS 0.18um Technology", IEEE Symposium on Humanities, Science and Engineering Research,2012.

[18]. Mayank Nema and Rachna Thakur " Design of Low-Offset Voltage Dynamic Latched Comparator" IOSR Journal of Engineering Vol. 2(4) pp: 585-590, Apr. 2012,

[19]. Christopher J. Lindsley, M.S. thesis, "A Nano-Power Wake-Up Circuit for RF Energy Harvesting Wireless Sensor Networks", Oregon State University, 2008.

[20]. HeungJun Jeon, M.S. thesis, "Low-power high-speed low-offset fully dynamic CMOS latched comparator", Northeastern University, 2010.

[21]. Vipul Khatyal, Ph.D thesis, "Low power high speed and high accuracy design methodologies for Pipeline Analog-to-Digital converters", Iowa State University,2008

[22]. Wazir Singh, M.S. thesis, "Study and Design of Comparators for High Speed ADCs", Thapar University, 2011

[23]. Priyesh P. Gandhi, M.Tech thesis," Design & Simulation of Low Power High Speed CMOS Comparator in Deep Sub-micron Technology", Nirma University, 2010

[24]. Prasun Bhattacharya, M.Tech thesis," Design of A Novel High Speed DynamicComparator With Low Power Dissipation for High Speed ADCs", National Institute of Technology Rourkela, 2011

[25]. Silpakesav Velagaleti, M.Tech thesis, "A Novel High Speed Dynamic Comparator With Low Power Dissipation And Low Offset, National Institute of Technology Rourkela, 2011

[26]. Dhanisha N. Kapadia, Priyesh P. Gandhi, "Implementation of CMOS Charge Sharing Dynamic Latch Comparator in 130nm and 90nm Technologies", IEEE Conference on Information and Communication Technologies, Nooral Islam University, Tamilnadu 11-12 April 2013

[27]. Dhanisha N. Kapadia, Priyesh P. Gandhi, "Design and Comparative Analysis of Differential Current Sensing Comparator in Deep Sub – Micron Region", IEEE Conference on Information and Communication Technologies, Nooral Islam University, Tamilnadu 11-12 April 2013

[28]. Dhanisha N. Kapadia, Priyesh P. Gandhi, "Design and Simulation of High Speed CMOS Differential Current Sensing Comparator in 0.35um and 0.25um Technologies", International Journal of Electronics and Communication Engineering and Technology, Vol. 3, Issue 3, October-December 2012. (Impact Factor: 3.59)

[29]. Dhanisha N. Kapadia, Priyesh P. Gandhi, "Simulation of Different Characteristics of CMOS Charge Sharing Dynamic Latch Comparator in 0.35um, 0.25um and 0.18um Technologies", International Journal of Emerging Technology and Advanced Engineering Vol. 2, Issue 11, Nov 2012. (Impact Factor: 0.8)

[30]. Dhanisha N. Kapadia, Priyesh P. Gandhi, Nipa B. Modi, "Characterization of High Speed CMOS Resistive Dividing Comparator in Different CMOS Technologies", International Journal of Engineering Research & Technology, Vol.1, Issue 9, Nov 2012. (Impact Factor: 3)

[31]. Dhanisha N. Kapadia, Priyesh P. Gandhi, "Characterization of Resistive Dividing Comparator in Deep Sub-Micron Region", International Journal of Electronics Communication and Computer Engineering, Vol. 3, Issue 6, Nov. 2012. (Impact Factor: 1)

Table 1 Comparison of Different Architectures of Voltage Comparator in 130nm

Parameters	Resistive Dividing comparator	Differential Current Sensing Comparator	Charge Sharing Comparator	Proposed Comparator
Propagation Delay(ns)	0.94	0.945	1.26	0.52
Speed(GHz)	1.06	1.06	0.79	1.92
ICMR(V)	-0.5 to 0.9	-0.69 to 0.77	-0.2 to 0.16	-0.3 to 0.4
Offset	227.15nV	51.37mV	0.026mV	80mV
Power Dissipation	167mW	133.76mW	167.32mW	9.19uW

Table 2 Comparison of Different Architectures of Voltage Comparator in 90 nm

Parameters	Resistive Dividing comparator	Differential Current Sensing Comparator	Charge Sharing Comparator	Proposed Comparator
Propagation Delay(ns)	0.81	0.675	0.75	0.41
Speed(GHz)	1.23	1.48	1.33	2.44
ICMR(V)	-0.11 to 0.82	-0.69 to 0.72	-0.24 to 0.18	-0.1 to 0.8
Offset	9.23mV	0.28mV	1.74mV	0.12V
Power Dissipation	71mW	12.12mW	4.89mW	7.45uW