Perfromance Comparison of Comparators Used In SAR ADCs for Ultra Low Power Biomedical Applications

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***Abstract*—**SAR ADCs are primarily used in biomedical applications to perform analog to digital conversions. Low power consumption is of paramount importance in biomedical applications as it directly translates to improved battery life and reduced frequency of surgical operations to replace depleted batteries. In SAR ADCs, the comparator is the most power consuming block. This paper presents three unique comparator architectures used in low power applications. The first architecture comprises of a two stage opamp based comparator with a power dissipation of 1.4715µW .The second architecture proposes the use of hysteresis/positive feedback loop to reduce noise distortions in the comparator output. The resulting power dissipation was found to be 266.73 µW. The last architecture explores a novel concept where an SR latch based mechanism is used to reduce the total ON time of the comparator. The resulting power dissipated was found to be equal to 46.36 pW. The circuits are simulated in standard CMOS 0.18µm technology.

Keywords*—ADC; SAR ADC; Comparator;low-power*

I. INTRODUCTION

Signals that originate inside the human body are analog in nature and cannot be operated upon by signal processing equipment. In order to be able to process these signals, they are first converted into a digital form using specialized analog to digital converters (ADCs)

In the world of biomedical implant devices, power consumption is a major parameter for optimization. As the size of batteries fitted onto implant devices is fixed, employing circuit architectures with low power consumption directly translates to increased life time of the implanted devices and reduced frequency of surgical operation to replace the battery on these devices. Low power consumption also translates to lower heat dissipation thus preventing damage of tissues when these devices are implanted into sensitive regions of the body. SAR ADCs are chosen for biomedical applications as they offer lower power consumption compared to other ADC architectures such as flash ADCs but at the same time offer decent accuracy and speed of conversion suited for biomedical applications.

In the design of SAR ADCs for biomedical applications, power consumption and area are the two most important design constraints. Tradeoffs exist between area and power consumption as designing for low power leads to an increase in chip area. The paper primarily focuses on optimization of power while trying to reduce the area occupied as much as possible

II. BLOCKS OF THE SAR ADC

The Successive approximation register (SAR) is a class of analog to digital converters that converts an uninterrupted analog waveform into a digital format suitable for various signal processing operations. SAR ADC uses a binary search algorithm to iterate through all possible quantization levels. The primary characteristics of SAR ADC include low power consumption and good accuracy

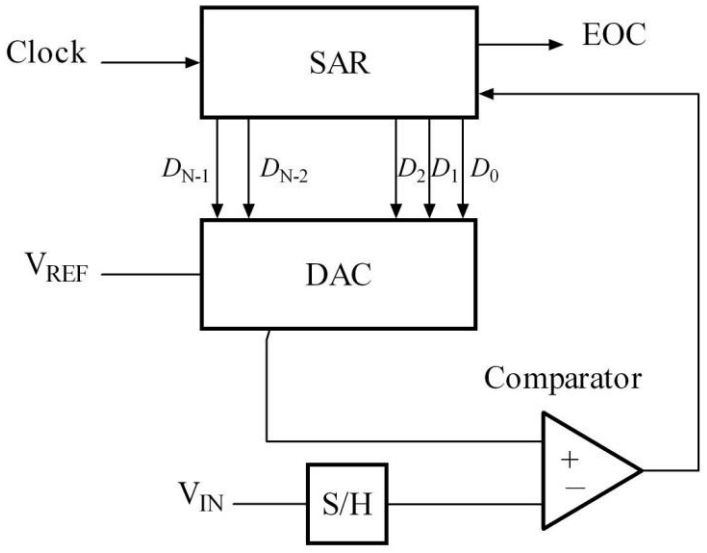

Fig.1: block diagram of SAR ADC

2.1. Sample and hold circuit: The sample and hold is an analog circuit that samples the voltage of a constantly time varying analog waveform and holds its value at a fixed level for a specified period of time.

The sample and hold circuit in its simplest form consists of a switch and a capacitor. A transmission gate is used as a switch instead of a single NMOS/PMOS transistor as it passes a full logic 1 and logic 0. A MOSFET is modelled as a capacitor by shorting its drain, source and bulk.

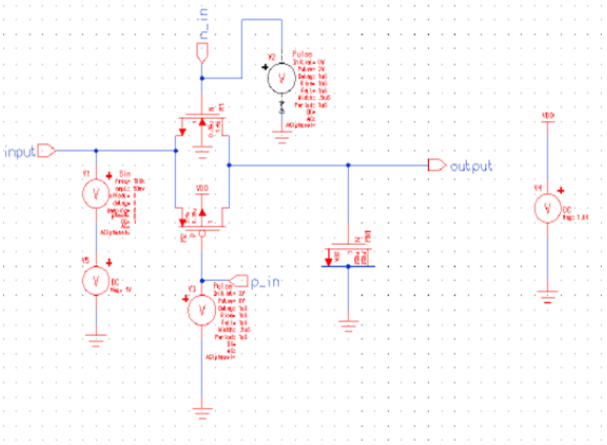

Fig.2: Sample and Hold circuit

Simulation results are shown in Fig 7.

2.2. Comparator: The comparator compares the analog signals at its two input terminals and outputs either a logic high or logic low. The output of the DAC is fed to the non-inverting terminal and the output of the sample and hold circuit is fed to the inverting terminal of the comparator. The output from the comparator is supplied to the SAR logic block. The comparator can be considered as the most important block of the SAR ADC as it performs the A/D conversion.

2.3. Digital to Analog Converter: The DAC performs the reverse function of the ADC. The output of the SAR logic block is digital in nature and hence needs to be converted into a continuous time varying analog form before it can be fed to the comparator. This conversion is carried out by the DAC.

2.4. Successive Approximation Register: The SAR logic block is based on an implementation of the basic binary search algorithm. D flip-flops are used to implement this logic. The digital input from a comparator is fed to the SAR block and then based on whether the signal from the comparator was a logic 1 or 0, appropriate shift operations are performed and a digital bit sequence is produced. This bit sequence is then fed to the DAC.

III. COMPARATORS

The comparator has been identified as the block that consumes the most power and hence has been the focus of optimization efforts in order to decrease power consumption. Three novel architectures have been explored.

A. TWO STAGE OPAMP BASED COMPARATOR:

The two stage amplifier consists of a cascade of a V – I stage and an I – V stage. The first stage consists of a differential amplifier which converts differential voltages into currents. These differential currents are then applied to a current mirror load recovering the differential voltage. This section thus acts as a voltage amplifier. In The second stage, input voltage is converted into current using a Common Source MOSFET. A current sink is used as load to the MOSFET which again converts the current to a voltage at the output. The second stage is nothing more than a current sink inverter.

The dual stage comparator is as shown in Fig.3.

The static power dissipation was found to be around 1.4715 µW. The total area consumed by the circuit is 420 µm².

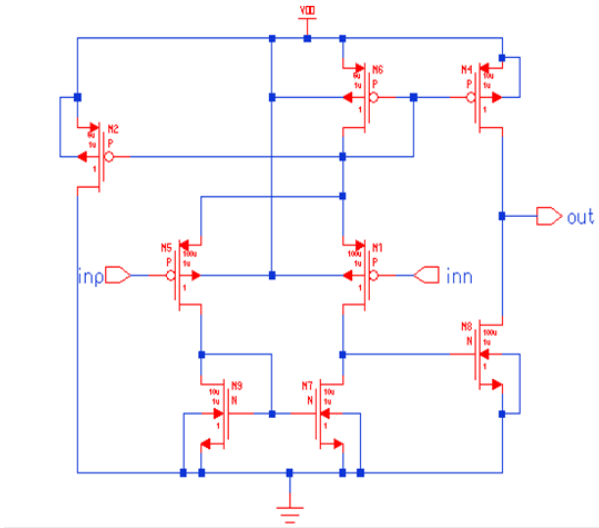

Fig.3: Two stage opamp

Simulation results are as shown in Fig.10

B. Comparator with Hysteresis:

Hysteresis based comparators are used primarily in noisy environments in which signal transitions at threshold points are to be detected. Hysteresis is employed primarily to prevent the false triggering of the comparator. The comparator output is changed only if the analog signal makes a transition over the pre-defined upper threshold point (UTP) and lower threshold point (LTP).

Hysteresis in effect is illustrated in Fig.4. An instance of false triggering due to noise is shown in Fig 4.a. Fig4.b shows hysteresis in effect. The output transitions are made only if the analog signal passes the predetermined UTP and LTP.

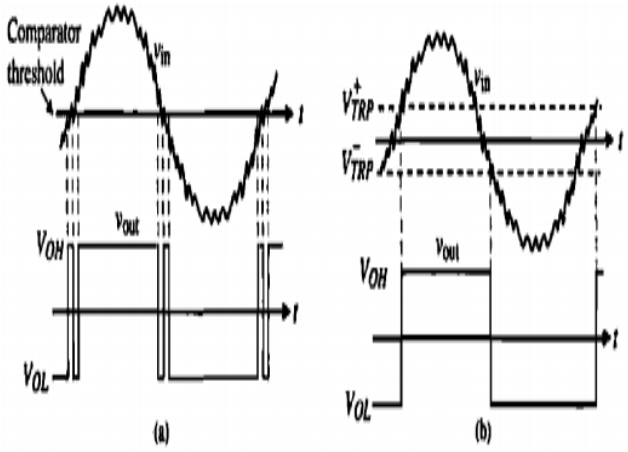

Fig.4: Illustration of hysteresis on comparator output

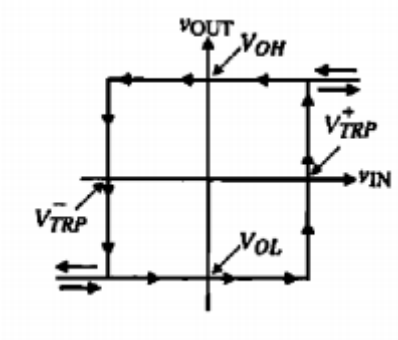

Fig.5: Comparator transfer curve with hysteresis

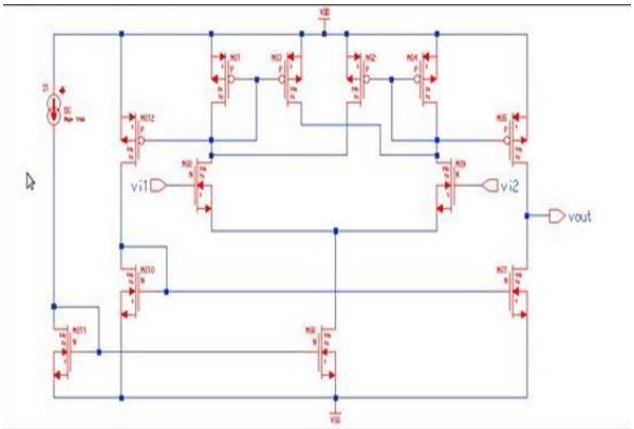

Fig.6: comparator with hysteresis

Hysteresis is achieved via internal positive feedback. The circuit has two feedback paths. First is current-series feedback through the common-source of transistors Ml and M2. This path has negative feedback. The second path is a voltage-shunt feedback through

Gate—drain of transistors M6 and M7. This path has a positive feedback. Hysteresis is now dependent on the value of feedback. If the negative feedback exceeds the positive feedback, then the total net feedback is negative and no hysteresis would take place. Conversely, if the magnitude of positive feedback exceeds the negative feedback, hysteresis will occur.

Static power dissipation was found to be equal to 266.73µW while the area occupied was equal to 14.4 µm².

C. SR Latch Based Comparator:

The base circuit consists of a differential pair and a cross coupled inverter. The circuit operates in two phases, the reset phase and the evaluation phase.

The differential pair feeds current into the cross coupled inverters. The cross coupled pair has large gain and amplifies the signal to a full logic 1 or logic 0.

When clock is at logic 0 i.e. the reset phase, PMOS M5 is 'ON'. The node Di of the comparator will charge to Vdd via M5.

NMOS transistors M6 and M7 which either create or cut-off access of differential pair to the cross coupled inverters.

When the clock is low, M1, M6 and M7 are off hence there is no path from differential pair to cross coupled inverter. Thus there is no current flow through the differential pair.

During the evaluation phase when the clock is at logic 1, transistors M6 and M7 are switched 'ON'. M1 is also 'ON' and current flows through it.

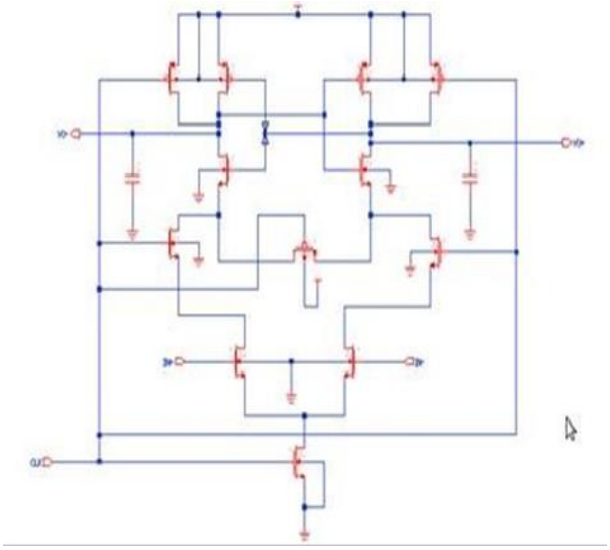

Fig.7 Base comparator model

The charged Di node starts to discharge via M6 and M7 to the transistors that comprise of the differential pair i.e. M2 and M3.These transistors have high kickback noise at their gates.

M6 and M7 are used to prevent this kickback noise. Hence M2 and M3 will have increased current flow in evaluation phase.

The reset transistors M6 and M7 need to be larger in size than M4 and M5 because they need to drive the high current density of the latch.

MODIFIED SR LATCH CIRCUIT:

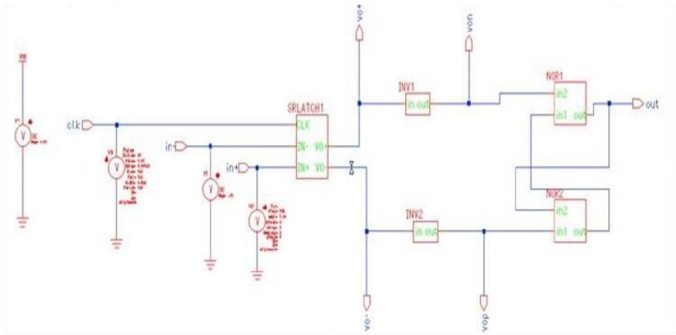

Fig 8: modified circuit

The output of the base comparator circuit is given to a SR latch constructed out of NOR gates.

Custom made NOR gates are used in the simulation to reduce power consumption.

When clock is at logic 0,output is reset to Vdd and conversely when the clock goes to logic 1, the voltage at the two comparator terminals i.e. the input and reference voltage are compared and a resulting logic high or logic low output signal is produced.

Table 1. Comparator output logic

Voltage comparison	Output
Vin > Vref	Logic high
Vin<Vref	Logic low

Simulation results are as shown in Fig.12

IV. SIMULATION RESULTS

The simulation results of the Sample and Hold circuit are as shown in Fig 9.

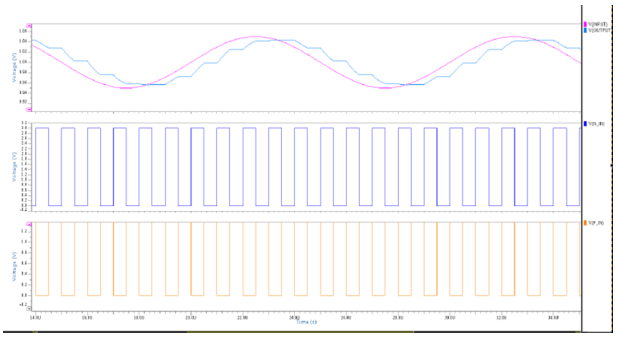

Fig.9: Sample and hold output

The input signal is a sine wave that is sampled with respect to a sampling pulse. The resultant output is a staircase waveform.

Fig.10 illustrates the obtained output waveform of the two stage comparator. As long as the input waveform from the sample and hold circuit is above the reference DC level which comes from the DAC block , the output of the comparator is a logic high as shown.

Fig.11 shows the simulation results of Comparator using hysteresis .A 10 kHz sine wave is compared with respect to a reference voltage of 200mV. When the input is above 200mV Vref, the output is a logic1 as shown in Fig.11 else it is a logic 0.

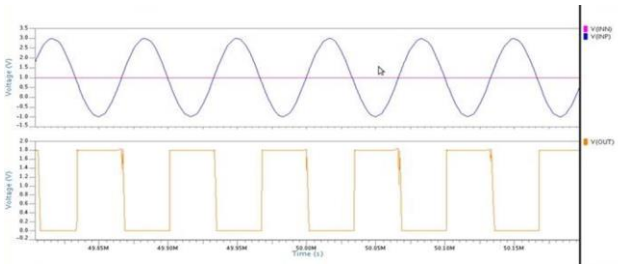

Fig.10: simulation result of two-stage comparator

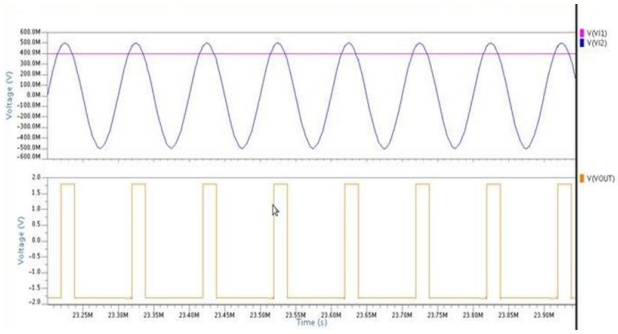

Fig.11: simulation result of the comparator with hysteresis

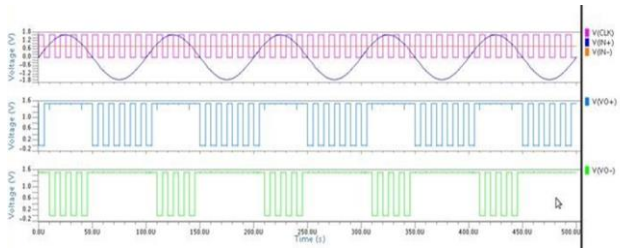

Fig.12: SR-Latch modified comparator waveform

Fig.12 shows the simulation results of the SR latch based comparator. A 10 kHz, 1.5V sinusoidal signal is fed to the positive , non-inverting terminal Vi+, while a 0.75V DC voltage is fed to the negative inverting terminal V- as a reference voltage. A 0.1 MHz clock signal is used to drive the comparator.

If Vi+ is greater than Vi-, the output is a logic 1 else it is a logic 0.

Table 2: comparison of comparators

Comparator type	Power Dissipated	Area occupied
Two-Stage opamp	1.4715µW	420µm²
Comparator with Hysteresis	266.7301µW	14.4µm²
SR-Latch based comparator	46.36pW	2.75184µm²

V. CONCLUSION

We have made comparisons of the different architectures of comparators which are to be used with SAR ADCs and the results are illustrated in Table 2. Keeping in mind our primary design constraints of power and area it is clearly visible that the SR Latch based comparator emerges as the best choice to be used in SAR ADCs for biomedical applications. The SR latch based comparator offers the least power dissipation as the comparator is kept ON only for as long as the analog to digital conversion is taking place and is switched OFF otherwise thus greatly reducing static power consumption. By carefully restricting the sizes of the W/L ratios of the MOSFETs present in the circuit the overall area occupied was further reduced.

In order to further reduce the power consumed efforts are made to drive the transistors in the subthreshold region. This can be achieved my setting the V_{GS} of the MOSFETs lesser than but close to their V_T. This feat can be achieved by carefully controlling the W/L ratios of the MOSFETs in order to decrease the current flowing through the circuit. In this manner the current flow and hence the power consumed can be substantially reduced.

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