International Journal of Modern Science and Technology *Vol. 1, No. 9, December 2016. Page 311-317.*
http://www.ijmst.co/ ***ISSN: 2456-0235.***

Research Article

Low Power Flash ADC and DAC Optimized with Pull down Circuit Control

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Abstract

Analog signal is characterized by the signal whose amplitude is continuously changing with respect to time while the amplitude and time is discrete in case of signal. The existing system describes the design of FLASH ADC using clocked digital comparator (CDC) will leads to setup and hold time violation and consumes power. The proposed system use latch based digital comparator with level based which reduces the power and increases the speed. ADC is controlled by a pull down network which triggers selected ADC as per the selection logic. The length of transistor is fixed and depending upon the width of transistor, internal references voltages are generated in the range of 0.63 to 1.02V.The proposed 4-bit flash ADC using CDC is designed using multiplexer based decoder and simulated with the help of Tanner-EDA tool in Tsmc 0.18 cmos technology.

Keywords: Multiplexer; Decoder; Clock Comparator; CMOS Switch.

Introduction

A signal in the real world is mostly analog in nature, for example, sound, light, video etc. In order to obtain a digital signal, an analog signal is required to be converted into a digital signal by using a circuit called analog to digital Converter[1].The electronics world is faced with various challenges when attempting to integrate analog signals and quantities with digital and discrete systems. , the existence of a tool that enables this integration is vital to many electrical engineers in today's world. The Analog-Converter (ADC) is not a new concept by any means, but is still a topic of interest when it comes to technology, due to its inevitable necessity in many systems being used today[2].

Analog design engineers focuses on presenting a new option among the many present, with distinct features that are aimed to satisfy various applications for analog-to-digital converters [3]. Analog signals with digital systems ADCs are used in different application from mobile communication devices to measure equipment. Since, the performance parameters like sampling rate, resolution, and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. Therefore, it is important to choose a proper ADC for each particular application and it is one of the commonly used high speed and low resolution applications.

Flash ADC is known for its fastest speed of operation among all the ADC architectures available and hence it is used for many of the practical applications [4]. The very large a and the High speed of the ADC enables very high frequency applications (in a few GHZ) range such as optical communication links, high density disk drives, radar processing, electronic Test equipment's, digital oscilloscopes, wideband Radio Receivers and so on. The flash ADC is also called as the parallel ADC because of its parallel architecture [5].

Analogue-to-digital converters (ADC) constitute the main element in state-of-the-art electronic systems. The advancement of the digital signal processing industry, researchers are faced with the increasing challenge of designing an innovative ADC. Nowadays, the ADC is included in the chip of an electronic system and is no longer a separate circuit for data converters, thus raising the ADC design requirements with regard to such characteristics as high speed, low power, less area, high resolution, low noise, etc. New methods and approaches are being constantly developed in order to enhance the performance of ADCs [6]. Among the various types of ADCs, the flash ADC is the best, not only renowned for its data conversion rate, but

Received: 30.11.2016; Received after Revision: 02.12.2016; Accepted: 03.12.2016; Published: 04.12.2016

also as a component in other ADCs, such as the pipeline and multi bit Sigma Delta ADCs [7].

Analogue-to-digital converters are the foundational blocks that form an interface between the analogue and digital domains [8]. Since the ADC is the primary block in mixed signal applications, it slows down data processing applications and restricts the performance of the system [9]. This method presents the architectures of converters beginning with the basic definition of an ADC is the primary block in mixed signal application, it slows down data processing applications and restricts the performance of the system [10]. This architectures of several A/D converters beginning with the basic definition of an ADC, followed by descriptions of various ADC architectures including Flash, Sigma, Delta, Pipeline, Successive Approximation [11] and Dual Slope ADCs. 3 bit, 4 bit, 8 bit and many technologies are available [12].

Flash ADC

The flash ADC, also known as a parallel ADC, is the fastest among all the other ADCs because of its parallel architecture, making it suitable for high bandwidth applications. However, it uses up a lot of energy for low resolutions and is costly for high resolutions. It is used primarily in high frequency applications and in the other ADC architectures such as the pipeline and multi-bit sigma delta ADCs some applications of flash ADCS include data acquisition, satellite communication radar processing.

Flash ADC consists of two structures.

(i) Clocked digital comparator
(ii) Multiplexed based decoder

Existing System

Clocked digital comparator

Generally 3 conversion processes are performed in ADC. Here, clocked digital comparator contains 2 inverter and transmission gate. Transmission gate acts as a sampler. The sampling frequency works on which clock operates and always the sampling frequency must be more than twice of input frequency. So, CDC acts as sampler and quantizer.

Multiplexed Based Decoder

The efficient flash ADC designed mostly with multiplexed based decoder. Multiplexer operates with high speed with minimum power compared to other mos logic styles as shown in figure 1 and tanner implementation of CDC shown in figure 2.

Flash ADC architecture

Implementation of FLASH ADC architecture using Tanner is shown in the figure 3.

DAC Architecture

A digital to analog converter (DAC) converts a discrete (digital signal) signals to continuous (analog signal) usually switches resistors and op-amps used to implement conversion in 2 types: (i) Binary Weighted Resistor and (ii) R-2R ladder.

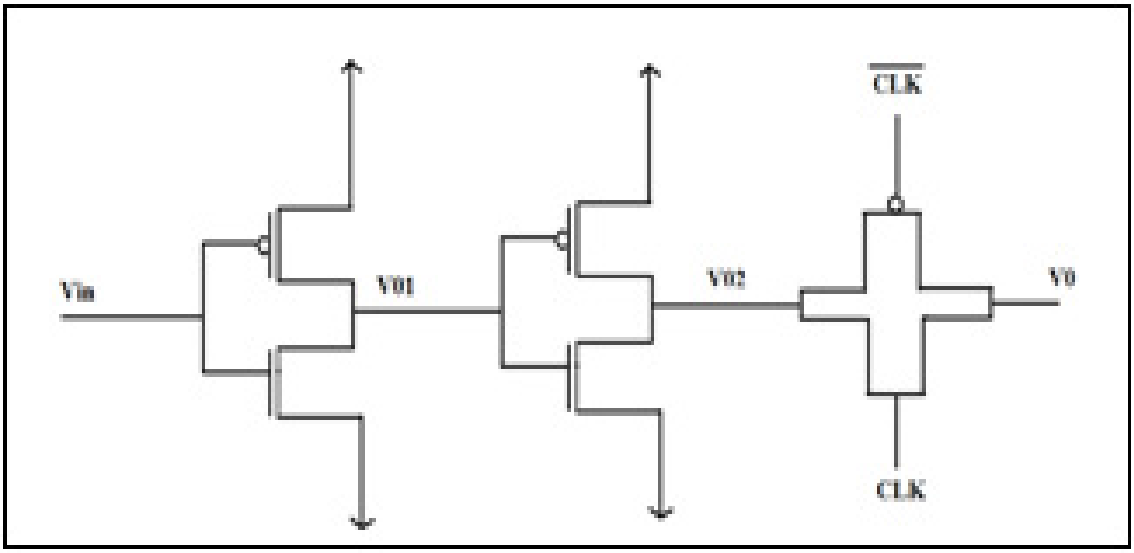

Figure 1. Clocked Digital Comparator

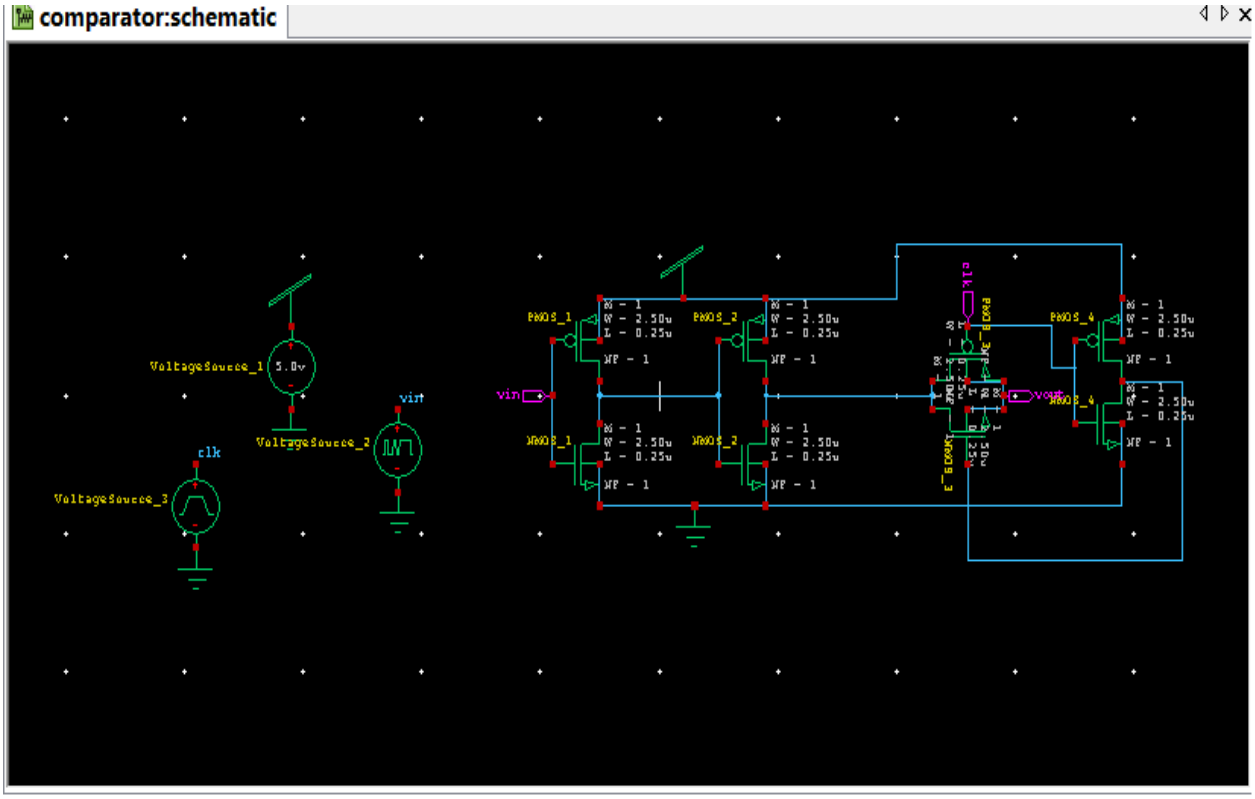

Figure 2. Clocked Digital Comparator

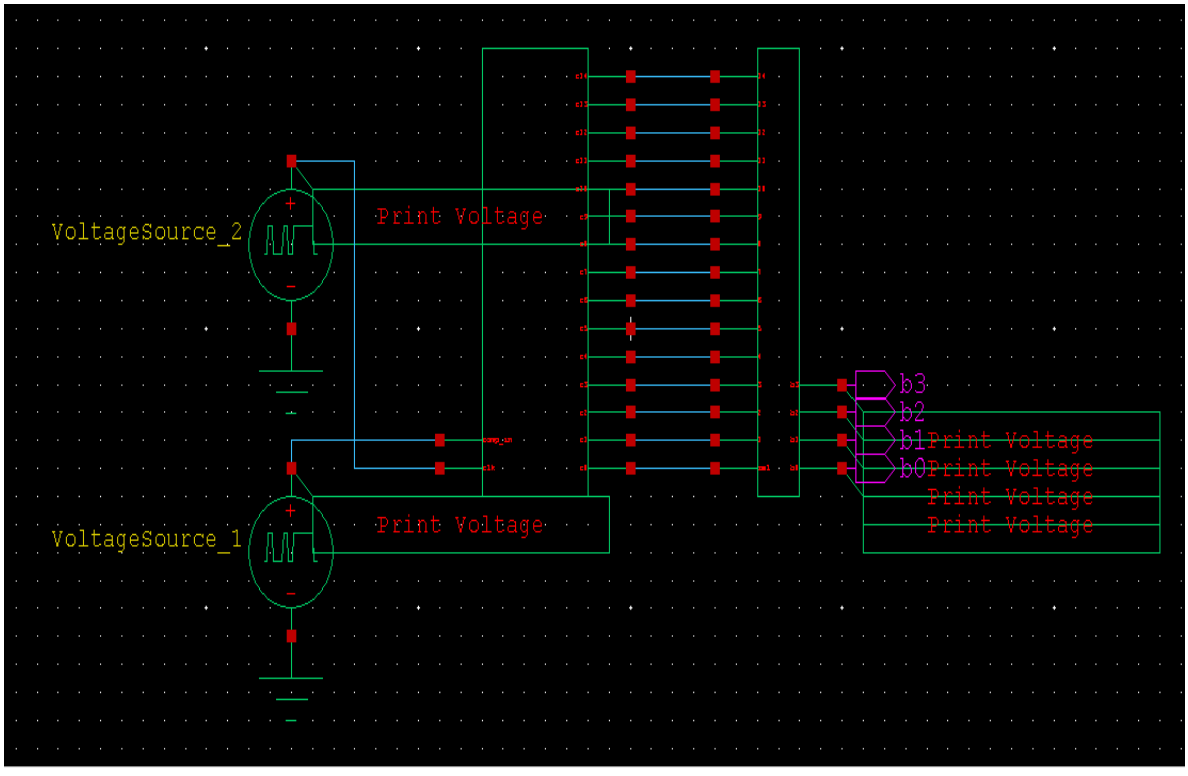

Figure 3. Flash ADC Architecture

Binary weighted ladder

Weighted resistors are used to distinguish each bit from the most significant to least significant. Transistors are used to switch between Vref and ground (bit high or low) as it requires high precision resistors we prefer, R-2R ladder Network.

R-2R ladder

Each bit corresponds to a switch. If the bit is high corresponding switch is connected to the inverting input of the op-amp. If the bit is low the corresponding switch is connected to ground.

Output waveform

The Waveform of DAC architecture is shown in figure 4 and figure 5.

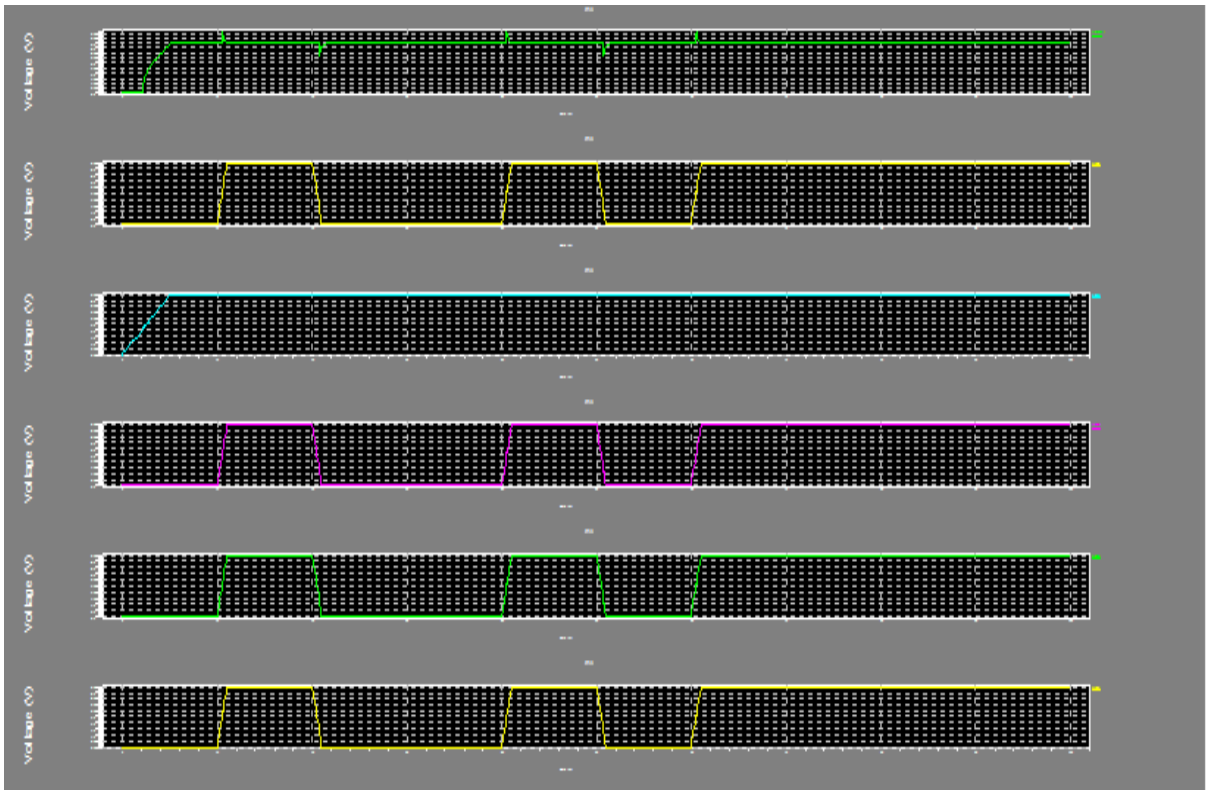

Figure 4. Existing output waveform

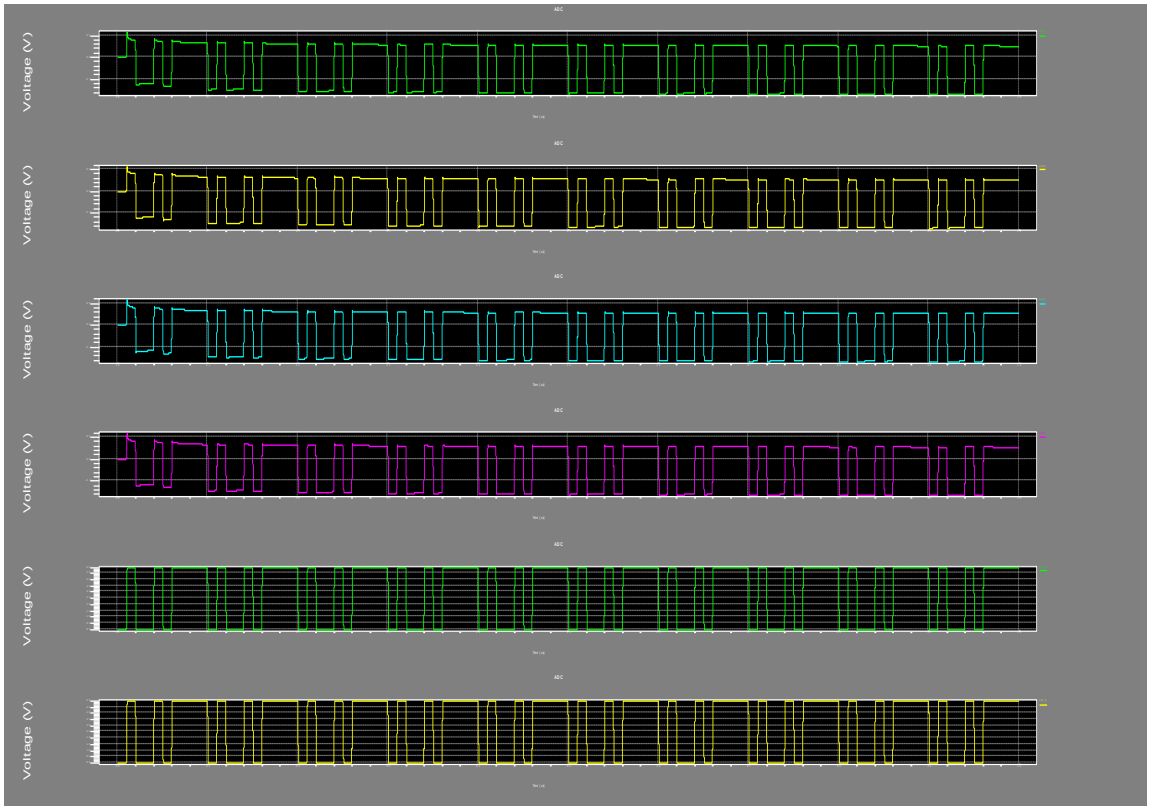

Figure 5. Flash Output waveform

Proposed System

The DAC circuit was designed by using pull down circuit as shown in the figure 6.

Pull down circuit

A Network that provides a low resistance path to Gnd when output is logic '0' and

provides a high resistance to Gnd using PMOS in pull down network, then its gate terminal should be provided with a negative voltage. Similarly if we use NMOS in pull up network, then its gate terminal should be provided with a voltage that is more positive than Vdd. So the voltages corresponding to logic states at input are different from that at output. Hence by using these two 'CMOS' gates cannot be interfaced directly as shown in figure 6 and 7.

Output waveform

The output waveform of pull down circuit is shown in figure 8.

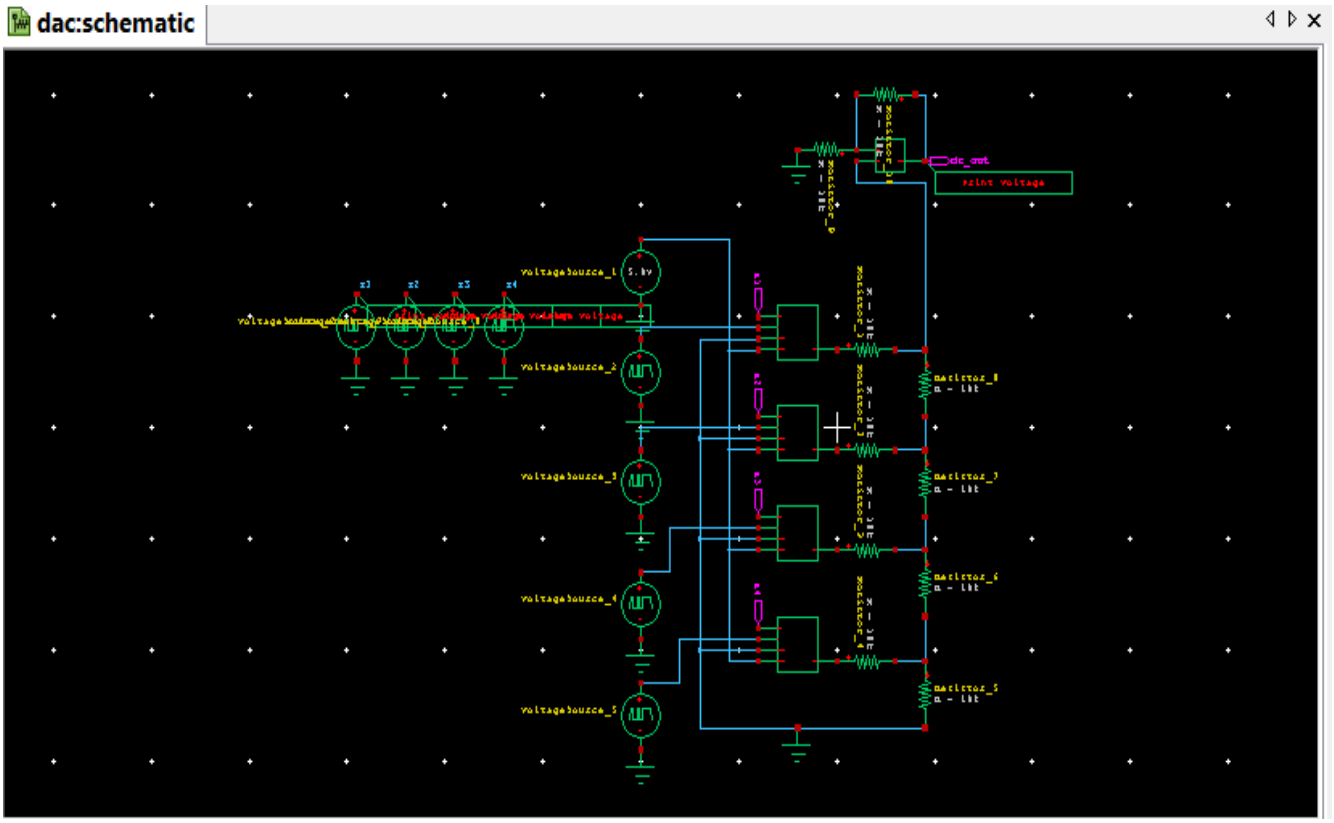

Figure 6. Pull down circuit

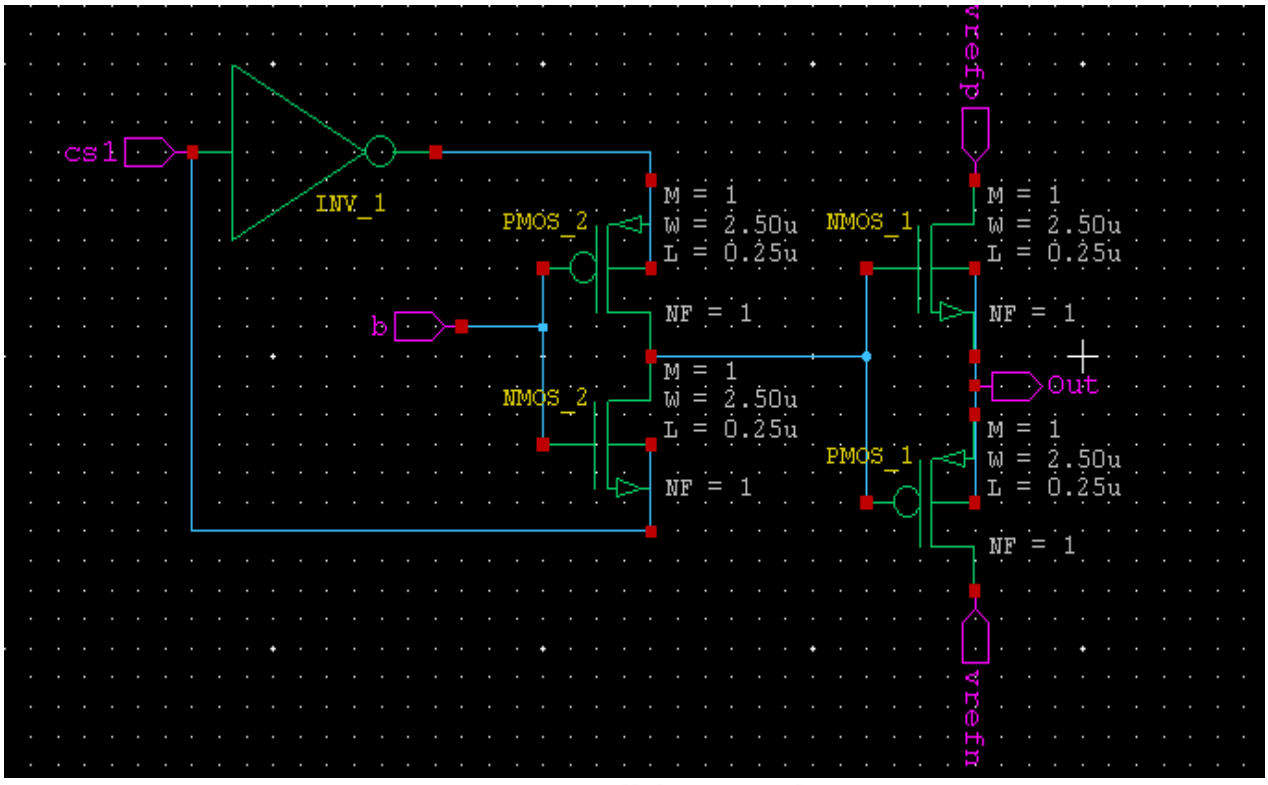

Figure 7. Pull down switch

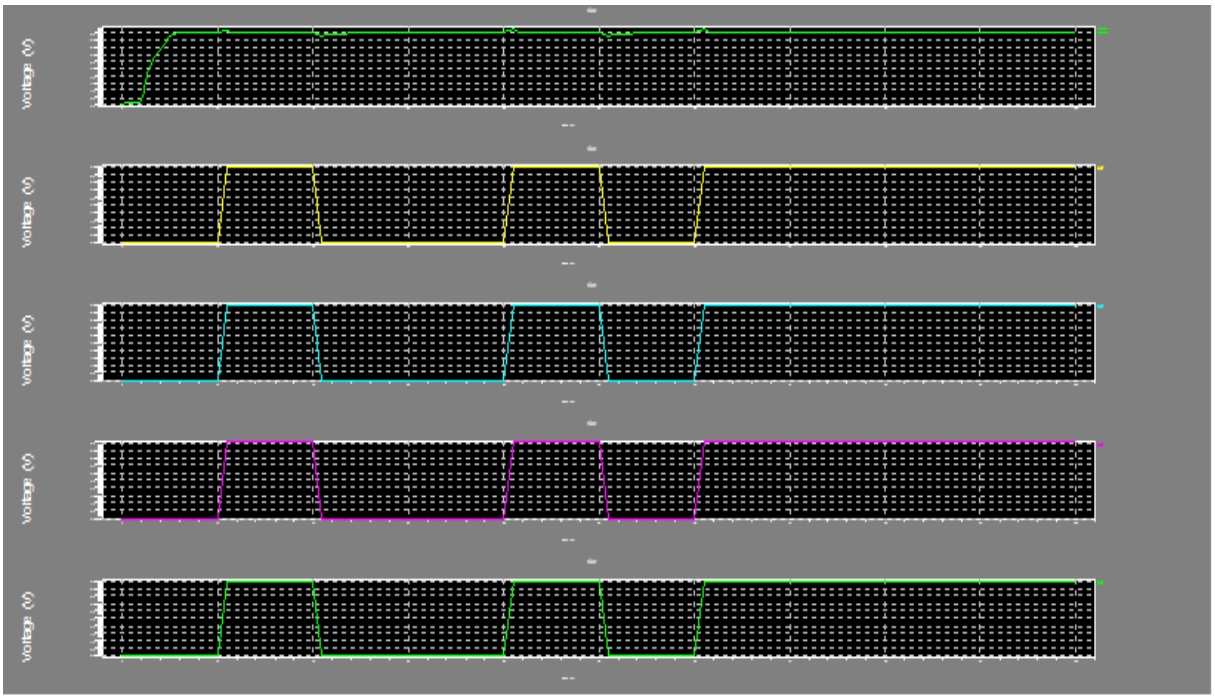

Figure 8. Output waveform of DAC with pull down circuit

Conclusions

The FLASH ADC consists of clocked digital comparator and multiplexed decoder. Decoder is mainly used to reduce the complexity of the circuit. Here Flash Architecture is one of the faster conversion methods. It is used mainly to increase the speed and reduce the power conversion of the circuit. Then in DAC Architecture, R-2R ladder circuit is used. To reduce the power consumption further pull down circuit methodology is used. By considering this methodology of designing the 4 bit flash ADC with the Tanner tool 13 software, we can convert the analog input signal to the 4 bit digital output.

Conflict of interest

Authors declare there are no conflicts of interest.

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