# 4-Mbit (128K x 32) Pipelined Sync SRAM

# Part Number: DPA71339G02A

\ The DPA71339G02A integrates 128K x 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}_1$), depth-expansion chip enables ($CE_2$ and $CE_3$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW}_{[A:D]}$ and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at the rising edge of the clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst address can be internally generated as controlled by the advance pin $\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports byte write operations. Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

The DPA71339G02A operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatiable.

- **-55˚ to +125˚C operating temperature**
- **Hermetically sealed ceramic package**
- **Registered inputs and outputs for pipelined operation**
- **128K x 32 common I/O architecture**
- **3.3V core power supply**
- **2.5V or 3.3V I/O power supply**
- **Fast clock-to-output times**
  - **2.6 ns (for 250-MHz device)**
- **Provide high-performance 3-1-1-1 access rate**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequence**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **"ZZ" Sleep mode option**
- **This product uses Cypress CY7C13339G die and is tested to meet military and space operational environment requirements.**

## Logic Block Diagram



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