Design, Simulation and Comparative Analysis of CMOS Ripple Carry Adder

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Abstract: In this research paper, based on 90 nm technology 2 designs for Full Adders and 2 designs for 4 bit Ripple Carry Adder have been discussed, analysed at schematic and compared on the basis of Area utilisation and Power consumption. For fast and productive circuits we require power and area efficient designs i.e. designs that consume less area and power. Rapid and explicit performance of a digital system is appreciably affected by the operation of the resident adders. From the simulations it has been perceived that one design of Full Adder and 4 bit Ripple Carry Adder based on that Full Adder design is better as compared to other design of full Adder and 4 bit Ripple Carry Adder based on that Full Adder design because of reduction in Area utilisation and Power consumption i.e. reduction of area by 17.02 percent and power by 2.07 percent for Full Adder and reduction of area by 35.03 percent and power by 26.07 percent for 4 bit Ripple Carry Full Adder.

Keywords: *CMOS, Flip Flop, Shift register, SISO, SIPO and VLSI.*

I. INTRODUCTION

Nowadays, the requirements of movable electronic devices are growing day by day. But hindrances like power utilisation, size and ability still persist and the demand to be overwhelmed in the prevailing designs. Power utilisation is the most significant concern in VLSI design. As per the modern rage in technology, the quantity of transistors is ceaselessly growing on a chip that leads to rise in the entanglement and power usage of a chip. The growing power expenditure causes rise in the temperature of the chips, which controls the circuit behaviour. So, it is necessary to tackle with these complications. Adders are renowned to be the most primary and foundational unit in every digital circuit used for accomplishing essential estimations and processing. The modern rage handles the scaling up to nanometer scale. But in nanometer CMOS technologies Leakage power has become a consequential perturbation [1]. So, the circuits are required to be executed with low power, dense packing size, and small propagation delay. So, arithmetic cells which utilise low-power and give high capacity are of appreciable [2]. It is significant to optimize adder circuits for strengthen the performance. We can optimise adder circuits at either logic level or at circuit level. Boolean equations can be recognised using Logic-level optimisation so that a faster or smaller circuit can be acquired. Circuit level optimization manipulates transistor sizes and circuit topology optimizes speed [3]

II. ADDERS DESCRIPTION

For many processing operations adders are renowned to be the most significant, Adders are considered to be the fundamental part for counting, multiplication and filtering. One of the applications of filters is the Low Pass Filter used in the receiving unit of microwave power generation circuit [4]. This results in the consideration of Adders to be the most important and the basic unit to the designers of the digital system [5]. In computer arithmetic Binary addition is considered to be the most primary frequently used application [6]. Basically, adders are used for computing addition of 2 numbers and are widely used in ALUs and Processors to compute addresses, increment and decrement operators and various other computations. Half adder uses ALU (arithmetic logic circuitry) of the computer to calculate the two bits binary addition [7]. Full adder is made from Half Adder which necessitates 3 inputs; an input carry is the third input which helps in cascading the carry bit between two different adders [7]. Various depictions like excess-3 or binary coded decimal can be generated by using Adders [8]. There are two classifications of Adders namely: half adder and full adder [8].

A. Half Adders

Let us suppose that our two binary variables be x and y. x + y is the representation of binary sum, which means

$$0+0 = 0 \quad 0+1 = 1 \quad 1+0 = 1 \quad 1+1 = 10$$

Last case result is binary 10 (i.e., 2 in base 10) [8]. The operation performed by the half adder is to add two binary digits known as augend and addend which results in the generation of two outputs named as ‘Sum’ and ‘Carry’. For the generation of ‘Sum’ XOR is employed to both inputs whereas by using AND gate ‘Carry’ is generated [8].

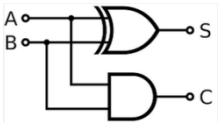

Fig. 1. Half adder.

Fig. 1 shows half adder whose truth table is depicted in Table 1 [2].

TABLE 1. TRUTH TABLE FOR HALF ADDERS

INPUTS		OUTPUTS	
A	B	S	CY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

It is very convenient to execute 1-bit adder with the help of the XOR Gate for the output 'SUM' and an AND Gate for the 'Carry' [8]. Binary digit quantities can be added by using Half Adder [8]. Sum and carry values are obtained by using Half Adders which both are binary digits [9]. In binary number system it is possible for the sum to be out of range which leads to the initialisation of the concept of carry out [9].

B. Full Adders

The logical circuit that accomplish the addition operation on three binary digits is termed as Full Adder [8]**.** We can add two 8-bit bytes together by using the full-adder logic [8]. Fig.2, Fig.3, Fig.4 shows various models of full adders.

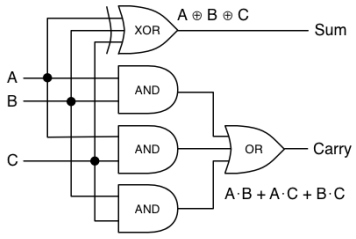

Fig. 2. Full adder.

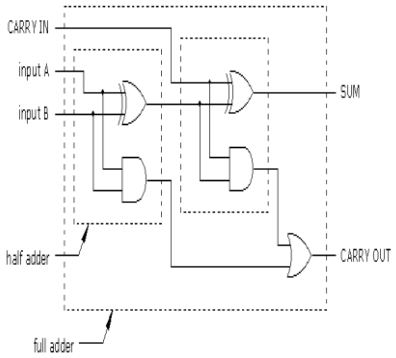

Fig. 3. Full adder using 2 Half adders.

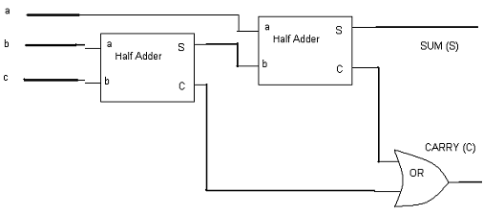

Fig. 4. Full adder using 2 Half adders' component diagram

Table 2 shows truth table for full adders.

TABLE 2.TRUTH TABLE FOR FULL ADDER

INPUTS			OUTPUTS	
A	B	C	CY	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full adder circuit can be executed with the help of two half adder circuits. In Half Adder circuit initially A and B are added to create a partial Sum, first half adder results in C-IN and Sum which are added in the second half adder to generate the final Sum output [8]. The basic building block in the arithmetic unit of Digital signal processors and application specific integrated circuits is the Full Adder which is also used in variety of digital electronic devices [10]. Comparator Logic Style based on the Basic full adder based contributes to low power and area as compared to other Logic Style [11].

C. Ripple Carry Adder

Result of binary sum 1+1 is 10 is inspected as a 0 and 1 is transferred to the left to result "carryout is 1" as shown in Fig. 5 taken from [12]. Logical circuit can be designed by the Ripple carry adder using numerous full adders to add n-bit numbers.

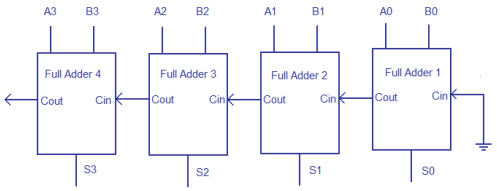

Fig. 5. Ripple carry Adder

C (in) is the input of every Full adder in the Ripple Carry Adder whose output is C (out) which is the input of the adder following that particular adder. RIPPLE CARRY ADDER is the name assigned to such type of adder, because every next full adder receives the input which is the carry bit of the previous Full Adder. The Half Adder can replace the first Full Adder because no carry bit is required for the first adder [12].

III. SCHEMATIC DESIGN SIMULATIONS

Half adder, Full adder and 2 designs of Ripple carry adders are designed using two designs of Full adders and are simulated using DSCH at Schematic level.

Fig. 6 shows the half adder design at Schematic level in which truth table of Half Adder is verified. During HIGH state of both the clocks at the input, output of LED connected with Sum O/P is 0 and the output of LED connected with Carry O/P is 1 which is depicted with glowing LED in Red colour.

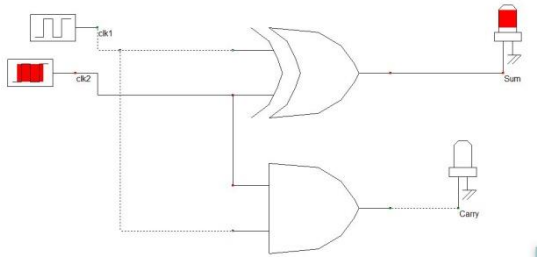

Fig. 6. Half adder design

Fig.7 shows DSCH timing Simulation Diagram of Half adder which verifies the truth table. In this 'clk1' and 'clk2' are the two clock inputs where as 'Carry' and 'Sum' are the two outputs of the Half Adder.

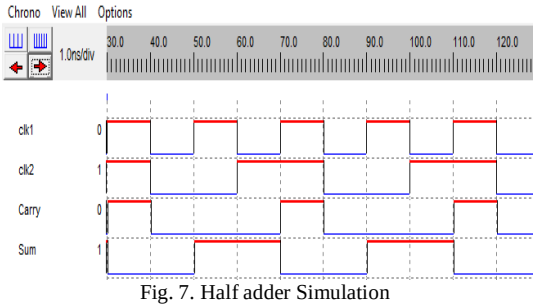

Fig. 7. Half adder Simulation

Fig. 8 shows the Full Adder design1 at Schematic level in which truth table of Full Adder is verified. During HIGH state of one of the three clocks at the input, output of LED connected with Sum O/P is 1 which is depicted with glowing LED in Red colour and the output of LED connected with Carry O/P is 0.

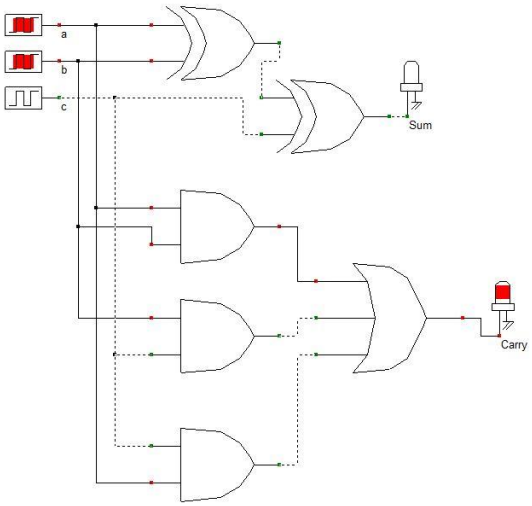

Fig. 8. Full adder design1

Fig. 9 shows Schematic level timing Simulation Diagram of Full Adder design1 which verifies the truth table. In this 'a', 'b' and 'c' are the three clock inputs where as 'Carry' and 'Sum' are the two outputs of the Full Adder design1.

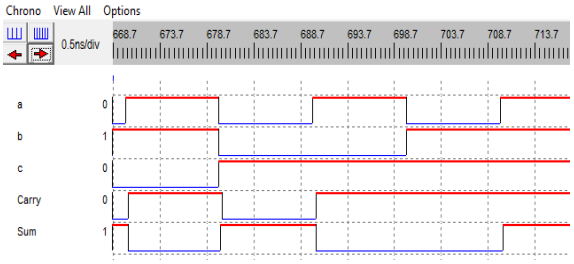

Fig. 9. Full adder design1 simulation

Fig. 10 shows 4-Bit Ripple Carry Adder Design 'A' using Design1 of Full Adder at Schematic level. In this design four Full Adders using design1 are cascaded serially. Each carry bit is used as the ripple or input to the next Full Adder.

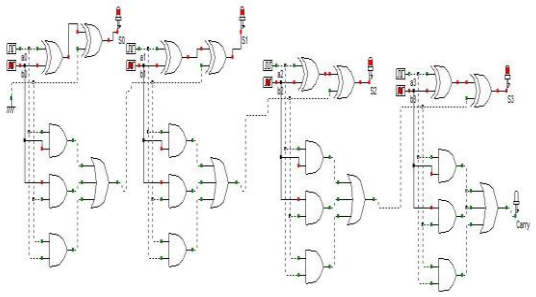

Fig. 10. 4-Bit Ripple Carry Adder Design 'A'

Fig. 11 shows 4-Bit Ripple Carry Adder Design 'A' timing simulation using Design1 of Full Adder at Schematic level. Finally we get four sum outputs as S0, S1, S2, S3 and one carry output as 'Carry'.

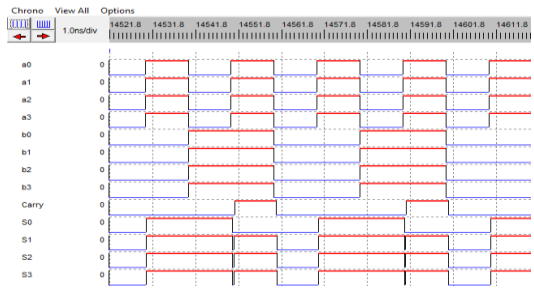

Fig. 11. 4-bit Ripple carry adder design 'A' simulation

Fig. 12 shows the Full Adder design2 which is made using 2 half adders at Schematic level in which truth table of Full Adder is verified. During HIGH state of one of the two clocks at the input, output of LED connected with Sum O/P is 1 which is depicted with glowing LED in Red colour and the output of LED connected with Carry O/P is 0.

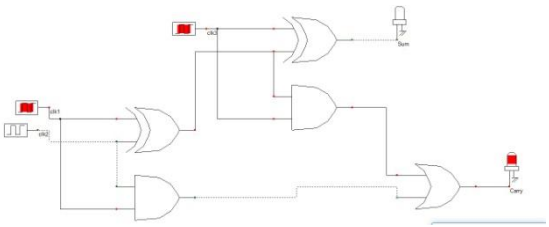

Fig. 12. Full adder design2

Fig. 13 shows Schematic level timing Simulation Diagram of Full Adder design2 which verifies the truth table. In this 'clk1', 'clk2' and 'clk3' are the three clock inputs where as 'Carry' and 'Sum' are the two outputs of the Full Adder design1.

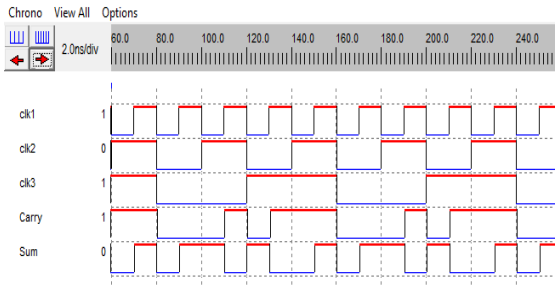

Fig. 13. Full adder design2 simulation

Fig. 14 shows 4-Bit Ripple Carry Adder Design 'B' using design2 of Full Adder at Schematic level. In this design four Full Adders using design1 are cascaded serially. Each carry bit is used as the ripple or input to the next Full Adder.

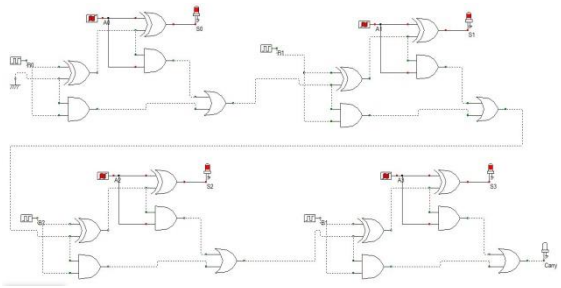

Fig. 14. Ripple carry adder design 'B'

Fig. 15 shows 4-Bit Ripple Carry Adder design 'B' timing simulation using Design2 of Full Adder at Schematic level. Finally we get four sum outputs as s0, s1, s2, s3 and one carry output as 'Carry'.

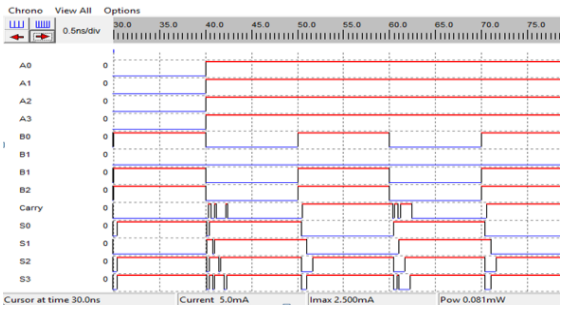

Fig. 15. 4-bit Ripple Carry adder design 'B' timing simulation

IV. LAYOUT ANALYSIS

Layout Design of various Adders are developed using MICROWIND. Simulations are also achieved in MICROWIND using BSim4 model to figure out the minute variations and to capture maximum non ideal parameters.

Fig. 16 shows Layout design of Half Adder. This helps in physical level analysis in which 'clk1' and 'clk2' are the two clock inputs and 'sum' and 'carry' are the two inputs.

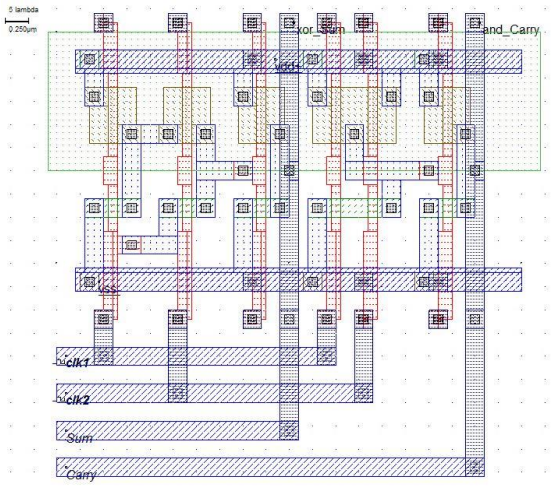

Fig. 16. Half adder Layout design

Fig. 17 shows the BSIM4 Simulation of Half adder Layout design which is used to capture more Non ideal parameters as compared to other 3 levels i.e. Level1, Level2 and Level3 Simulations. In BSIM4 simulation even minute spikes can be identified. Power consumption is 22.312 micro watts.

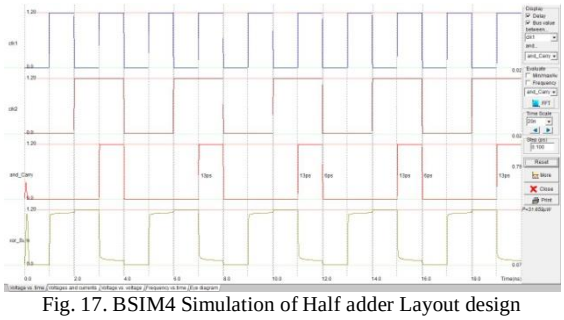

Fig. 17. BSIM4 Simulation of Half adder Layout design

Fig. 18 shows Layout design of Full Adder design1. This helps in physical level analysis in which 'a', 'b' and 'c' are the three clock inputs and 'Sum' and 'Carry' are the two corresponding outputs.

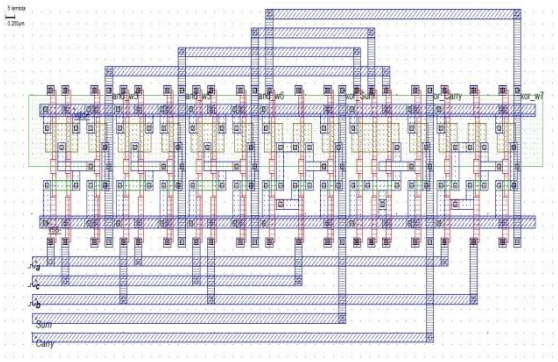

Fig. 18. Full adder Layout design1

Fig. 19 shows the BSIM4 Simulation of Full adder design1 using Layout design which is used to capture more Non ideal parameters as compared to other 3 levels i.e. Level1, Level2 and Level3 Simulations. Minute Spikes identification capability of BSIM4 simulation makes it highly proficient. Power consumption is 66.528 micro watts.

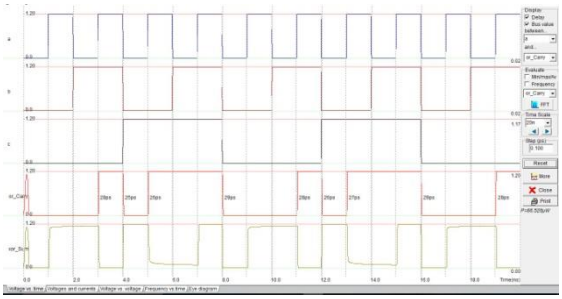

Fig. 19. BSIM4 Simulation of Full adder Layout design1

Fig. 20 shows 4-Bit Ripple Carry Adder Design 'A' using Layout Design1 of Full Adder. This is the layout design in which four Full Adders using design1 are cascaded serially. Each carry bit is used as the ripple or input to the next Full Adder.

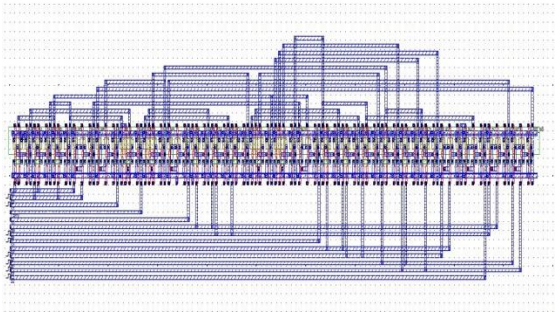

Fig. 20. 4-Bit Ripple Carry adder Layout design 'A'

Fig. 21 shows the BSIM4 Simulation of 4-Bit Ripple Carry Adder Design 'A' using Design1 of Full Adder using MICROWIND which is used to capture more Non ideal parameters as compared to other 3 levels i.e. Level1, Level2 and Level3 Simulations. Minute Spikes identification capability of BSIM4 simulation makes it highly efficient. Power consumption is 0.290 milli watts.

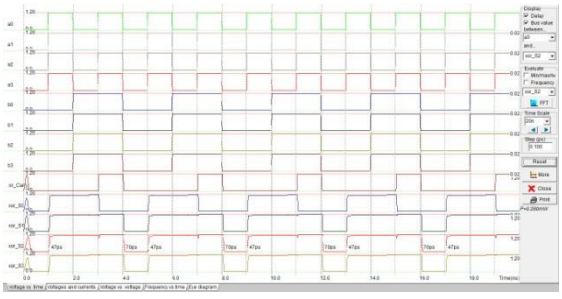

Fig. 21. BSIM4 Simulation of 4-Bit Ripple adder design 'A' using Design1 Full Adders

Fig. 22 shows Layout design of Full Adder design2 generated using two half adders. This helps in physical layout analysis in which 'clk1', 'clk2' and 'clk3' are the three clock inputs and 'Sum' and 'Carry' are the two corresponding outputs.

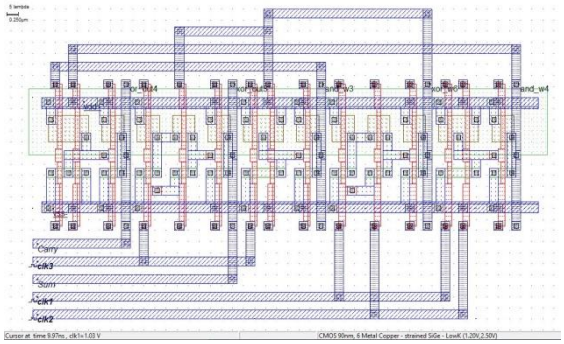

Fig. 22. Full adder Layout design2

Fig. 23 shows the BSIM4 Simulation of Full adder Layout design2 using 2 half adders which is used to capture more Non ideal parameters as compared to other 3 levels i.e. Level1, Level2 and Level3 Simulations. Minute Spikes identification capability of BSIM4 simulation makes it highly proficient. Power consumption is 65.145 micro watts.

Fig. 23. BSIM4 Simulation of Full adder layout design2

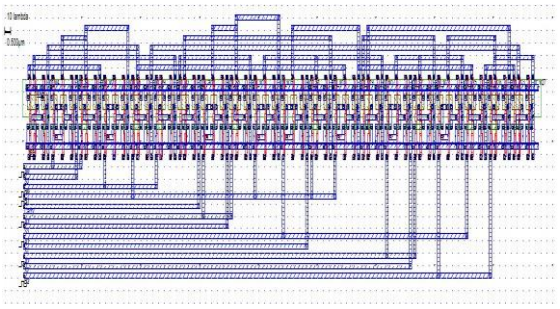

Fig. 24. 4-Bit Ripple Carry Adder Layout design 'B'

Fig. 24 shows 4-Bit Ripple Carry Adder Layout design 'B' using Full adder Layout design2. This is the layout design in which four Full Adders using design2 are cascaded serially. Each carry bit is used as the ripple or input to the next Full Adder.

V. RESULTS AND DISCUSSIONS

Table 3 shows comparison of various designs of Adders based n Electrical Properties viz. No. of Electrical Nodes, No. of NMOS, No. of PMOS and Size layout viz. Height and width (in micro meter), Area (in micro meter square) and Power Consumption (in micro Watt).Voltage Supply in 'Vdd high' is 2.50 volts and 'Vdd low' is 1.20 volts and Routing details include Grid size of 8 lambdas for all the implementations.

TABLE 3.TABLE SHOWING COMPARISON OF THE VARIOUS ADDERS' DESIGN BASED ON ELECTRICAL PROPERTIES AND SIZE LAYOUT

Serial No.	Design Type	Area (in micro meter square)	Power Consumption (in micro Watt)
1.	Half Adder	100.5	31.659
2.	Full Adder design1	98.7	66.528
3.	Full Adder design2	81.9	65.145
4.	4 bit-Ripple Carry Adder design 'A' using Full adder using design1	719.6	280
5.	4 bit-Ripple Carry Adder design 'B' using Full adder using design2	467.5	207

VI. CONCLUSION

Based on 90 nm technology 2 designs for Full Adders (Design1 and Design2) and 2 designs for 4-bit Ripple Carry Adder (Design 'A' and Design 'B') have been discussed, analysed at schematic and compared on the basis of Area utilisation and Power consumption. For fast and productive circuits we require power and area efficient designs i.e. designs that consume less area and power. Rapid and explicit performance of a digital system is appreciably affected by the operation of the resident adders. From the simulations it has been perceived that Design2 is better than Design1 and Design 'B' is better than Design 'A' based because of reduction in Area utilisation and Power consumption i.e. reduction of area by 17.02% and power by 2.07 % in Design2 as compared to Design1 and reduction of area by 35.03 % and power by 26.07 % in Design 'B' as compared to Design 'A'.

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