A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion

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***Abstract*—A passive 2nd-order sigma-delta modulator based on a cascade of first-order lowpass filters was designed, fabricated, and tested. A lumped RC filter is added in the loop of a conventional 1st-order passive sigma-delta modulator in order to improve the linearity of its transfer function. A low power edge-triggered comparator was designed and fabricated along with lumped components in ON Semiconductor's C5 500-nm process. The implementation achieved a THD below 1% for all frequencies between 10 Hz and 5 kHz. With a 5 V supply the power consumption of the sigma-delta modulator is 64.5 uW to 150 uW depending on the input signal.**

I. Introduction

There is a well-known trade-off between power consumption and speed/accuracy in the design of analog to digital converters (ADC). In applications such as remote sensing, often the power consumption is prioritized over accuracy. For a sigma-delta (Σ-Δ) ADC a large portion of the power consumption comes from the use of an active integrator circuit. Thus, a logical place to look when trying to reduce the power consumption of a Σ-Δ ADC is to eliminate the active integrator. In this work we investigate performing the integration function using a simple passive filter. This is also the path taken by several other researchers [1] and [2]. However, in both [1] and [2] a conventional passive 1st- or 2nd-order loop filter is used [3]. An alternative 2nd-order passive Σ-Δ topology proposed in this paper offers low-power consumption while preserving sufficient accuracy. The topology may be implemented using switched-capacitor techniques which would result in near zero static power consumption. Investigating this approach can be the focus of future research activities.

II. Passive Sigma-Delta Topologies

The conventional 1st-order Σ-Δ modulator is shown in Fig. 1 [3]. This topology uses a comparator, two resistors and a capacitor. When operating properly the average currents through each resistor are equal. The two resistors must match for the gain of the modulator to be unity. The capacitor performs the integration function. This topology has significant nonlinearity due to the voltage swing at the positive comparator input which is the voltage across the integrator (integrating capacitor) [3]. The output voltage is a function of the input voltage, quantization error voltage, and integration node voltage as shown in Eq. (1). The signal transfer function (STF), noise transfer function (NTF), and distortion term (DT) are given in Eqs. (2), (3), and (4) respectively. Note that the signal undergoes lowpass filtering during the conversion while the noise is highpass filtered and then, ideally, removed with a digital filter. Unfortunately, the distortion term also shows a lowpass response which can corrupt the input signal and be impossible to remove. Note that when using an active integrator the distortion term isn't present in the output of the modulator because the voltage across C1 is held constant.

$$V_{out} = \frac{1}{1+sR_1C_1}V_{in} + \frac{sR_1C_1}{1+sR_1C_1}V_{Qe} + \frac{-2}{1+sR_1C_1}V_{int} \quad (1)$$

$$STF = \frac{1}{1+sR_1C_1} \quad (2)$$

$$NTF = \frac{sR_1C_1}{1+sR_1C_1} \quad (3)$$

$$DT = \frac{-2}{1+sR_1C_1} \quad (4)$$

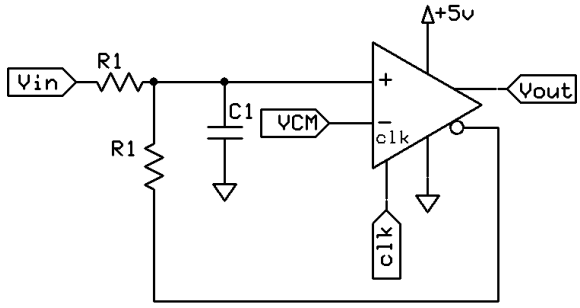

Figure 1 – Conventional 1st-order Σ-Δ modulator.

The modified 2nd-order Σ-Δ modulator proposed in this paper is shown in Fig. 2. This topology takes the conventional 1st-order ΣΔ modulator and adds an RC filter between the feedback summing node and the positive input of the comparator. The motivation for the addition of the RC filter is to try to reduce the voltage swing at the positive node of the comparator. Equation (5) shows the output voltage as a function of the input voltage, quantization error voltage and integration node voltage. The signal transfer function, noise

transfer function and distortion term for the proposed topology are shown in (6), (7), and (8) respectively. It can be seen from the NTF that the noise shaping is indeed 2nd-order.

$$V_{out} = \frac{1 + sR_2C_2}{1 + sR_2C_2 + sR_1C_1} \cdot V_{in} + \frac{s(sR_1C_1R_2C_2 + R_1C_1)}{1 + sR_1C_1 + s^2R_1C_1R_2C_2} \cdot V_{Qe} + \frac{1}{1 + sR_1C_1 + (1 + sR_2C_2)} \cdot V_{int} \quad (5)$$

$$STF = \frac{1 + sR_2C_2}{1 + sR_2C_2 + sR_1C_1} \quad (6)$$

$$NTF = \frac{s(sR_1C_1R_2C_2 + R_1C_1)}{1 + sR_1C_1 + s^2R_1C_1R_2C_2} \quad (7)$$

$$DTF = \frac{1}{1 + sR_1C_1 + (1 + sR_2C_2)} \quad (8)$$

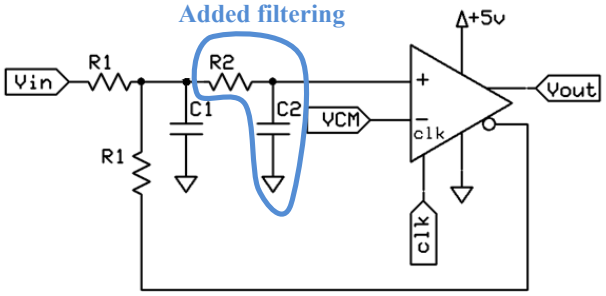

Figure 2 – Proposed 2nd-order Σ-Δ modulator.

To compare the different topologies, a simulation was performed using an ideal comparator to remove the effects of any component nonlinearities and focus on just the effect of the added RC filter. For the 1st-order modulator, the values of R1 and C1 were set to 1 MΩ and 10 pF respectively. For the 2nd-order modulator the values of R1, R2, C1, and C2 were set to 50 kΩ, 1 MΩ, 10 pF, and 10 pF respectively. A 0 to 5V 10 ms ramp (red trace) applied to the input with the filtered outputs of the 1st- (blue trace) and 2nd-order (green trace) modulator are shown in Fig. 3. Clearly, the performance of the modified 2nd-order modulator is improved over the conventional 1st-order topology.

III. Integrated Circuit Implementation

To investigate the real world performance of this novel topology, an integrated circuit implementation was designed, fabricated and tested. The heart of the Σ-Δ modulator is the clocked comparator. The clocked comparator was designed for minimal power consumption. The schematic of the comparator is shown in Fig. 4. The comparator is composed of a cross coupled latch connected to an S-R latch which causes the output to only change on the rising edge of the clock. In order to reduce contention current the input devices are long L NMOS. Additional details covering the design considerations can be found in [4].

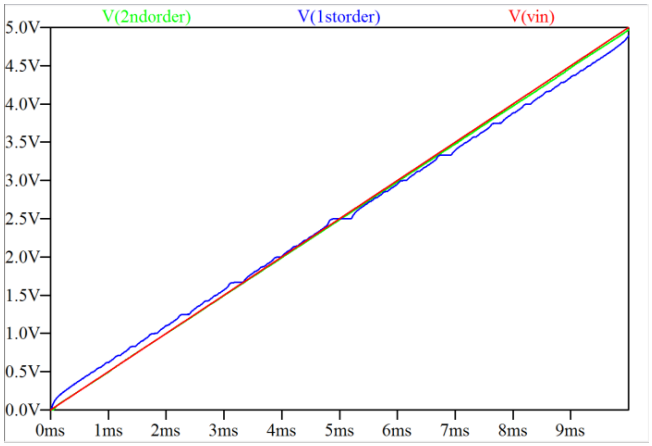

Figure 3 – Linearity comparison between 1st- and 2nd-order modulators.

On-chip passive lumped components are added to the comparator in order to implement the Σ-Δ modulator of Fig. 2 in integrated circuit form. The values for R1, R2, C1 and C2 are (nominally) 50 kΩ, 1 MΩ, 10 pF and 10 pF respectively. The resistors were fabricated using the high-resistance poly2 layer in the C5 process. The capacitors are formed using plates of poly1 and poly2 layers (poly-poly caps).

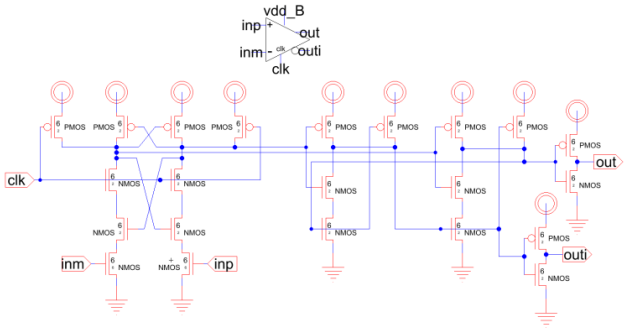

Figure 4 – Schematic of the low-power comparator.

A microphotograph of the chip is shown in Fig. 5. The proposed modulator can be seen in the lower right-hand corner of the chip in the red square and the corresponding layout, measuring 270 µm by 400 µm, is seen in Fig. 6.

IV. Integrated Circuit Test Results

The integrated circuit was tested in order to quantify its DC performance, AC performance, and power consumption. A 2nd-order 16 kHz low-pass filter with a Q of 0.33 was added to the output of the modulator in order to convert the one-bit data stream back into analog. The supply voltage was 5 V and the common-mode voltage was set to 2.5 V. A 5 V, 10 MHz square wave was used as the clock signal. DC linearity was tested by comparing input and output voltages using a 6.5

digit multi-meter. AC testing was done using a low distortion oscillator and looking at the total harmonic distortion (THD) at the output.

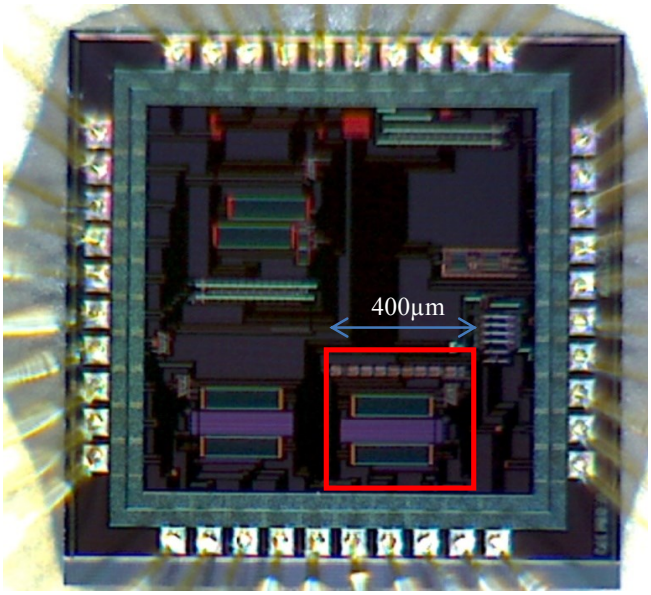

Figure 5 – Chip microphotograph. The proposed modulator is surrounded by the red box.

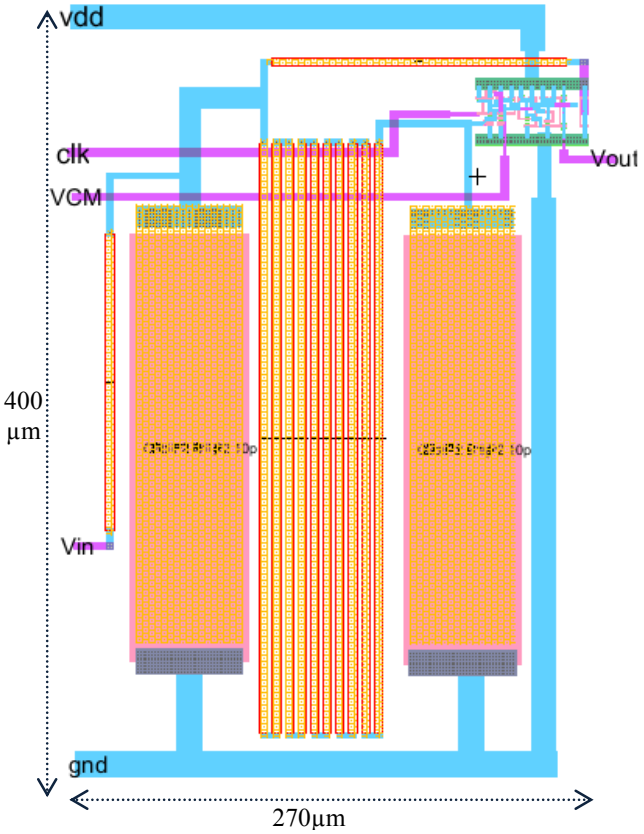

Figure 6 – Layout of the proposed modulator.

The measured DC transfer curves are seen in Fig. 7. There is an offset of a few hundred mV near ground and a considerably larger offset near *VDD* (+ 5 V). This is to be expected in a Σ-Δ modulator using ground and *VDD* for the fed back reference voltages. The filtered output voltage of the Σ-Δ modulator is limited to 4.2 V which is due to limitations of the comparator working with large input signals. There is also a small amount of gain error. While gain error is undesirable it is not as important as nonlinearity in the performance of an ADC.

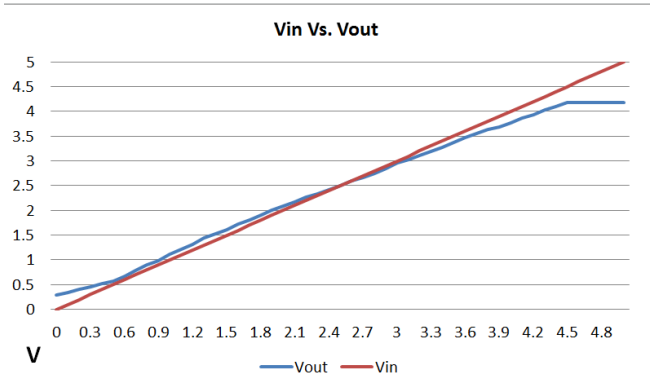

Figure 7 – Input and output DC transfer curve.

While DC plots are usually not given for Σ-Δ ADCs here we have added significant filtering in order to make the output (nearly) static. This result is shown in Fig. 8 where the x-axis is the Σ-Δ ADC's input voltage. The y-axis indicates the difference between the ideal output and the measured output in Volts. The differential nonlinearity (DNL) plot for the topology shows that DNL is kept to within 0.4 % when the input voltage is bounded between 0.4 V and 4.2 V. Note that here we use percentages because the "effective" least significant bit (LSB) is determined by the amount and type of digital filtering used on the output of the modulator. Since the slope of the line is relatively linear, the corresponding AC performance of the Σ-Δ modulator should be quite good. Note, as mentioned earlier, that here we are trading off accuracy for power consumption, discussed in more detail shortly.

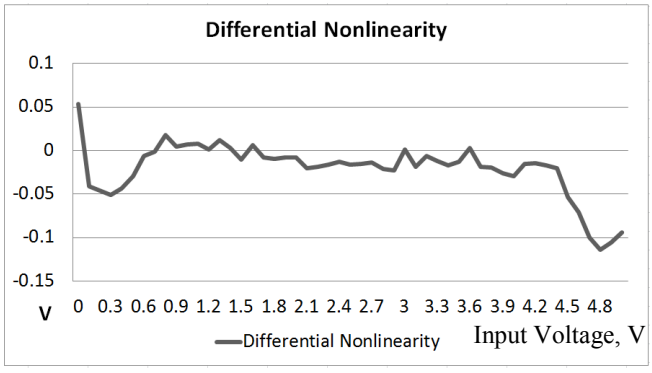

Figure 8 – Using filtering added to the output of the modulator in order to make it stable for determining DNL.

The measured harmonic distortion of the Σ-Δ modulator is shown in Fig 9. The input signal is a 1.5 V sine wave with a 2.5V DC offset. The total harmonic distortion (THD) remains under 40 dB below the fundamental for all frequencies between 10 Hz and 5 kHz. The dominant contributor to the THD is the 4th harmonic. Interestingly, the 2nd harmonic is the smallest component of the THD. Note that this data was harvested using a digital oscilloscope with an 8-bit vertical front-end (< 50 dB SNR which is comparable to performance of the modulator that is being tested).

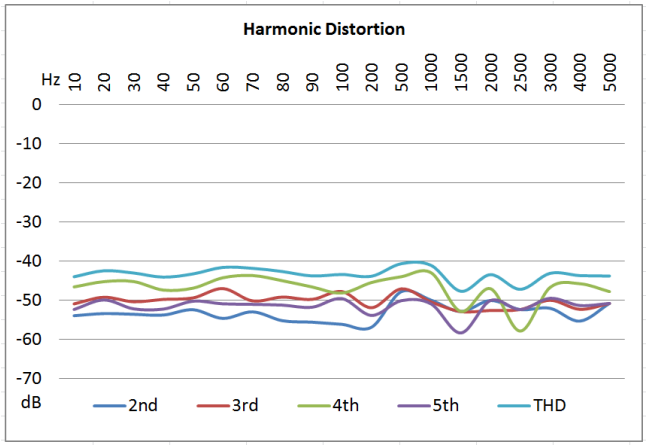

Figure 9 – Measured total harmonic distortion of the modulator.

Power consumption of the Σ-Δ modulator is quite low despite a 5 V supply voltage. Using a 10 MHz clock the measured supply current is only 12.9 µA when the output of the Σ-Δ modulator is at the extreme ends of its transfer function. For the worst case of when the Σ-Δ modulator is switching between high and low for an equal amount of time the measured supply current is 30 µA. This is the case in the middle region of the Σ-Δ modulator's transfer function. These values correspond to average power consumption between 64.5 µW and 150 µW. Using a modern process with a ~ 1 V supply voltage and dimensions well under 500 nm the power consumption of the topology may reach nW levels making this topology very useful in sensors powered by energy harvested from mechanical vibrations and/or solar cells.

Note that in this work power is continuously dissipated by the resistors used in the modulator. Since these resistors are large this power is fairly small and it may be possible to further reduce the power and the layout area (significantly) by replacing the resistors with switched-capacitors (SC). The drawback of this approach is the need for a clock generation circuit to provide non-overlapping clocks to the SC resistors. The benefit is essentially zero power dissipation at all times except for when the clock is transitioning high or low. The other test structures seen on the chip in Fig. 5, outside the red box, will be used to investigate this possibility in future work.

The performance of the proposed Σ-Δ modulator is compared to two other designs in Table 1. Although performance is worse than the other two designs, it is important to keep in mind that the proposed modulator is implemented in a 500-nm process with a 5 V supply. Also the results for the proposed Σ-Δ modulator are measured and not simulated.

Parameter	2nd Order ∑-Δ Modulator in This Work (Measured)	2nd Order ∑-Δ Modulator in [5] (Simulated)	2nd Order ∑-Δ Modulator in [2] (Simulated)
Process	500 nm	350 nm	350 nm
Resolution (ENOB)	8-bit	12-bit	10-bit
Power Consumption	100µW (typical)	120 µW	50 µW
Signal Bandwidth	5 kHz	1 kHz	4 kHz

Table 1 – Comparing performance of the proposed ∑-Δ modulator to [2] and [5].

V. CONCLUSION

The low power Σ-Δ modulator proposed in this paper retains relatively good precision despite the elimination of the active-integrator to reduce power dissipation. Although the linearity isn't as good as a Σ-Δ modulator implemented using an active integrator, the presented circuit should find use in applications which heavily prioritize power consumption and don't require high precision. Although the Σ-Δ modulator was implemented in a 500-nm CMOS process the concepts presented should scale to smaller, lower-power, processes.

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