Gate Dielectric Reliability in the Sub Threshold Regime

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***Abstract*—The dielectric reliability of devices operating in the high bias, low gate current sub threshold state that can occur in analog and mixed signal designs is investigated using substrate hot carrier injection to accelerate breakdown. The complexities of this stress mode are elucidated and a reliability projection methodology is presented.**

Keywords - Reliability, Breakdown, TDDB, Sub-threshold, Dielectric, Oxide, SiON, Hydrogen

I. INTRODUCTION

The high cost of technology development has led to the proliferation of silicon-on-chip applications with multiple transistor elements to attain additional capability through design rather than scaling. In cascoded design schemes where transistors are used as voltage dividers, this can result in over-design voltages being applied to one or more device terminals. An example is shown in Fig. 1, where 3.3 V is applied to the drain of a 1.8 V (EOT = 2.7 nm) NFET and the device operates in the low drain current sub threshold (depletion/weak inversion) regime. With an applied gate voltage of 2.6 V, the source voltage will float to approximately $V_G - V_T = 2.2$ V in the sub threshold state. The drain voltage feeding into the next transistor stage will then be 2.2 V.

If the bias conditions shown in Fig. 1 resulted in the device operating in the on-state (strong inversion), breakdown would be driven by $V_{GS} = 0.4$ V, so the failure rate would be negligible. However, the surface charge is a quadratic rather than exponential function of band bending in depletion and weak inversion [1] since there are not a sufficient number of electrons to screen the bulk field. Accordingly, breakdown of the transistor that is operating in the sub threshold state will be driven by $V_{GB} = 2.6$ V, which predicts high failure rates in some applications. This would require incurring the cost of extra mask sets to define 3.3 V transistor components if the sub threshold operating conditions shown in Fig. 1 are truly unreliable. However, I_G is low in weak inversion since it is supply limited, which raises the possibility that reliability could be favorable since breakdown is both energy and fluence driven [2]. The problem is how to accelerate breakdown in this low I_G, low E_{OX}, and high V_{GB} deep depletion regime.

In this work, we use substrate hot electron stress (SHE) to develop breakdown models for sub threshold operation.

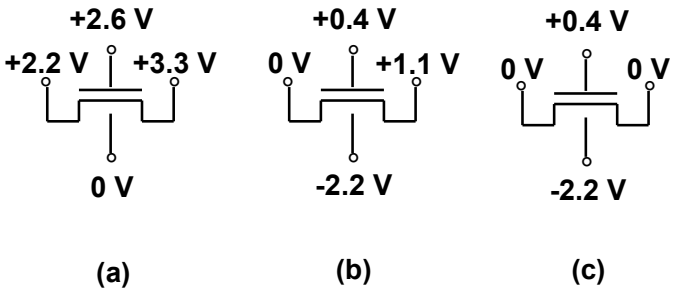

Figure 1. (a) Example of the biasing of a cascoded device operating in depletion/weak inversion. (b) Simplified equivalent biasing scheme. (c) Bias configuration for 3-terminal reliability projection.

II. RESULTS

An idealized cross section of the SHE device structure is shown in Fig. 2. It is a 4-terminal MOSFET or 3-terminal gated diode (with $V_D = V_S$) with an external PN junction that is forward biased to supply electrons. The oxide field, silicon field, and electron fluence can be separately controlled respectively by V_G, V_B, and I_{INJ} [3]. SHE has been used to study charge trapping [4], to separate the effects of energy and field on breakdown [5], to investigate vibrational excitation (VE) of silicon-hydrogen bonds as a mechanism for trap generation [6], and to profile trap distributions in high-k films [7]. As V_{GD} is small, we are primarily interested in modeling the effects of high V_{GB} in this work. We use the 3-terminal configuration as shown in Fig. 1(c) and refer to the combined source-drain terminal as the drain with a bias V_D.

The gate current versus stress time for uninterrupted stress (UIS) is shown in Fig. 3. SHE increases I_G by more than seven orders of magnitude and can accelerate breakdown even in this low E_{OX} sub threshold state. Due to the low E_{OX} and the low free surface charge density during stress, the first SBD event cannot be accurately detected for UIS because (i) I_{SBD} is difficult to resolve from the background current, (ii) I_G is initially a decreasing function of time due to charge trapping since de-trapping rates are reduced at low E_{OX} [8], and (iii) the application of a substrate bias further "softens" breakdown due to low surface electron density, which reduces the energy (since it is proportional to the square of the electron density) that can be dissipated during the transient formation of the SBD

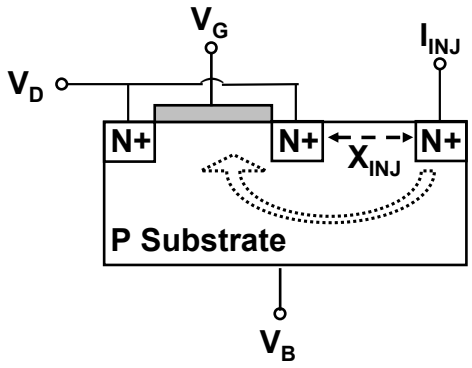

Figure 2. Idealized cross section of an SHE test structure in 3-terminal configuration, where $V_D = V_S$. X_{INJ} is the separation between the injector and NFET drain.

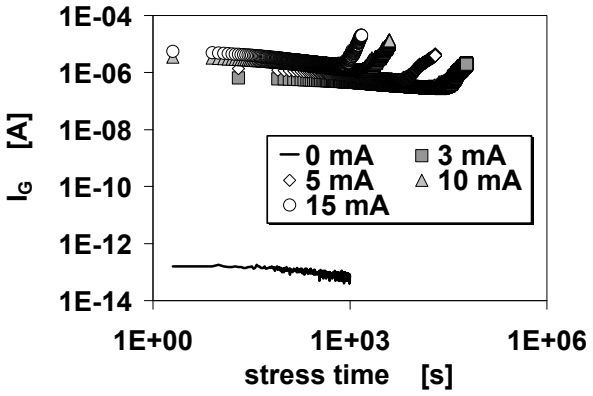

Figure 3. Gate current versus stress time for UIS with injector current as a parameter. $V_G = +3.0$ V, $V_D = +3.0$ V, $V_B = -2.2$ V.

path [9]. The first SHE SBD event can be detected in a conventional SILC measurement where only the gate is biased, so the stress must be periodically interrupted to perform a sense operation. For UIS, only the onset of wear out is measured.

When trap generation during electrical stress results from desorption of silicon-hydrogen (Si-H) bonds through multi-electron vibrational excitation (VE), the general form of the voltage and current dependence of the trap generation efficiency $\zeta(V,I)$ is given by [10], [11]

$$\zeta(V,I) = cI_O^{M-1}V^N, \quad (1)$$

where c is a constant, I_O is the total current impinging on the interfaces and M is the number of electrons required to desorb one Si-H bond. The charge to breakdown is proportional to $1/\zeta(V,I)$ so that for VE, the *voltage scaling* of Q_{BD} will follow the TDDB Power Law Model [11], [12]. From (1), when only one electron is involved in the hydrogen release process, $\zeta(V,I)$ becomes independent of current and breakdown will be controlled only by fluence and energy.

Q_{BD} versus I_{INJ} for UIS is shown in Fig. 4 for the off-state, weak inversion/depletion, and on-state conditions. In all cases, $Q_{BD} \sim I_{INJ}^{-1}$. From (1), the mechanism that follows this current dependence is two electron VE of Si-H bonds. Fig. 5 shows that the injector has little effect on the time-0 activation energies for transport, which are nearly zero as expected for band-to-band-tunneling (BTBT) in the substrate. During stress, $I_{INJ} >> I_B(BTBT)$ so that $I_O \alpha I_{INJ}$ whereas under operating conditions, $I_{INJ} = 0$ so that $I_O \alpha I_B(BTBT)$. Accordingly, I_O will be proportional to the sum of $I_{INJ} + I_B(BTBT)$. For 2-electron VE, the *current scaling* relationship from stress to operating conditions will be

$$Q_{BD} \alpha [I_{INJ} + I_B(BTBT)]^{-1}. \quad (2)$$

. The proportionality relationship in (2) applies whether trap generation occurs solely at the polysilicon-SiON interface, solely at the Si-SiON interface, or simultaneously at both interfaces. It can be seen that the $I_B(BTBT)$ term prevents the charge to breakdown from becoming infinite when the injector is disabled. Otherwise, it would not be possible to use (2) to extrapolate Q_{BD} to operating conditions

The Weibull slopes (β's) for the first SBD event are shown in Fig. 6 and the corresponding bulk and interface trap generation power law exponents "m", where $N(Q) = bQ^m$ are shown in Fig. 7. β drops sharply when $V_{GD} > 0$. Since β depends on the stress condition, a reliability assessment cannot be obtained for this experiment. There is a corresponding drop in the bulk trap generation power law exponent from approximately 1/2 to 1/6, which is numerically consistent with the observed change in β as predicted by the cell based percolation model [13]. It has been shown that the application of a substrate bias can modify the trap generation reaction, which results in a change in the trap generation power law exponent "m" and corresponding Weibull slope [14]. m = 1/2 means that a positively charged species such as H^+ is a product of the bulk trap reaction [15] whereas m = 1/6 corresponds to a dimerized species such as H_2 [16]. The similarity of the V_G dependence of the Weibull slope (Fig. 6) and bulk trap generation (Fig. 7) shows that bulk traps control SBD in this stress regime. No clear systematic trend is observed for the reaction that generates interface traps.

In LV-SILC measurements where the stress is periodically interrupted and the current is sensed at $V_G \sim V_{FB}$ [17], I_G and I_D sense traps at the polysilicon-SiON interface. I_G and I_B sense traps at the Si-SiON interface [18]. The I_D increase is due to tunneling from polysilicon-SiON interface traps into the pwell conduction band. The electrons subsequently diffuse out the drain contact as shown in Fig. 8(a)-(b). The increase in I_B is due to tunneling from either the polysilicon conduction band or from traps at the polysilicon-SiON interface into Si-SiON interface traps, followed by recombination with holes in the pwell as shown in Fig. 8(c)-(d). A tunneling/recombination mechanism between metal gate Fermi Level and p++ substrates was first proposed in the 1960's to explain the high conductance in samples that were known to have high as-processed interface trap densities [19]. $I_D(t)/I_D(0)$ and $I_B(t)/I_B(0)$ are shown in Fig. 9 and Fig. 10 respectively. For $V_{GD} > 0$, more traps are generated at the poly-SiON interface compared to

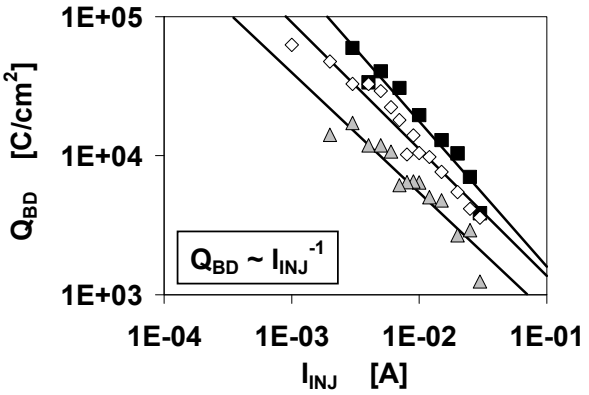

Figure 4. Q_{BD} versus injector current for UIS with V_B = -2.0 V. Squares: V_G = +3.0 V, V_D = +3.0 V (off-state). Diamonds: V_G = +3.4 V, V_D = +3.0 V (depletion/weak inversion). Triangles: V_G = +3.4 V, V_D = +1.0 V (on-state).

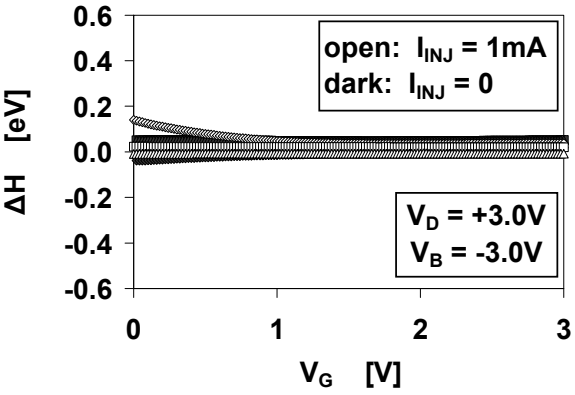

Figure 5. Time-0 activation energies for I_G (diamonds), I_D (squares), and I_B (triangles). $\Delta H \sim 0$ for all terminal currents.

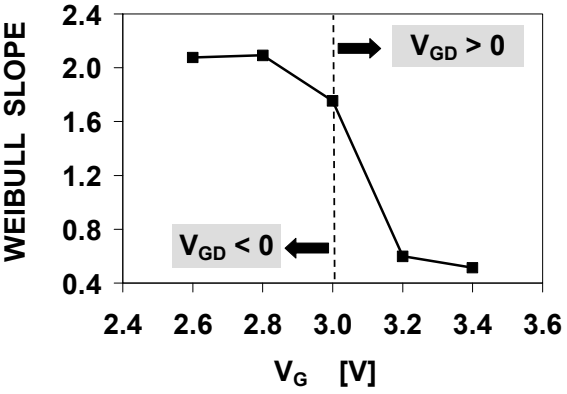

Figure 6. Weibull slope versus gate stress voltage. V_D = +3.0 V and V_B = -2.2 V during stress.

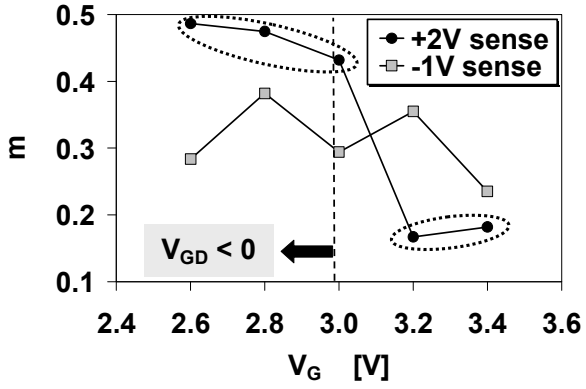

Figure 7. Trap generation power law exponents versus gate stress voltage with V_D = +3.0 V and V_B = -2.2 V during stress. Only V_G is biased during the sense operation. V_G = +2.0 V senses bulk traps and V_G = -1.0 V senses interface traps.

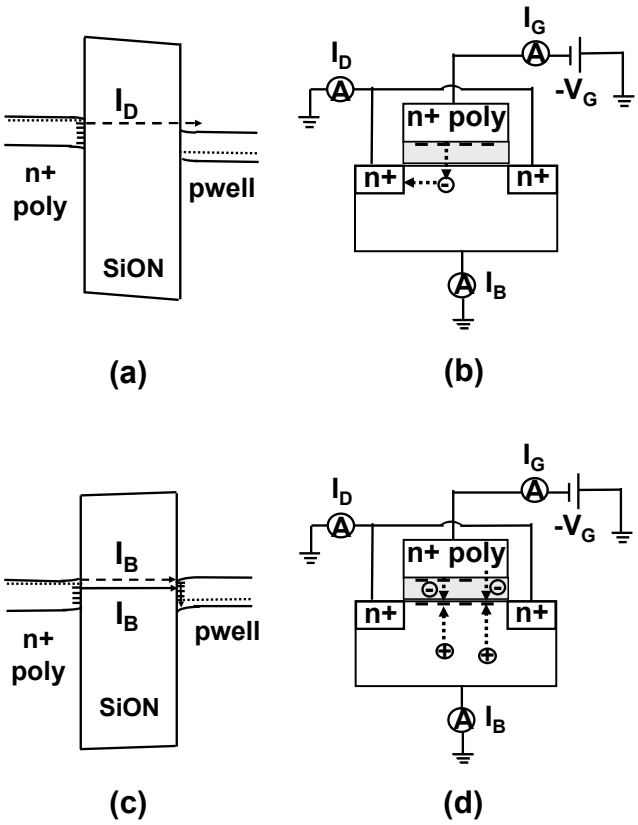

Figure 8. Band diagrams and device cross sections illustrating the current flow for LV-SILC for an NMOS device sensed at $V_G \sim V_{FB}$. (a), (b) Tunneling from n+ polysilicon interface traps into the pwell conduction band. The electrons subsequently diffuse out the drain contact and give rise to LV-SILC peaks in the drain and gate currents. (c), (d) Tunneling from either polysilicon interface traps or polysilicon conduction band into pwell interface traps, followed by recombination with holes. This process results in LV-SILC peaks in the substrate and gate currents. After Nicollian, ref. [18].

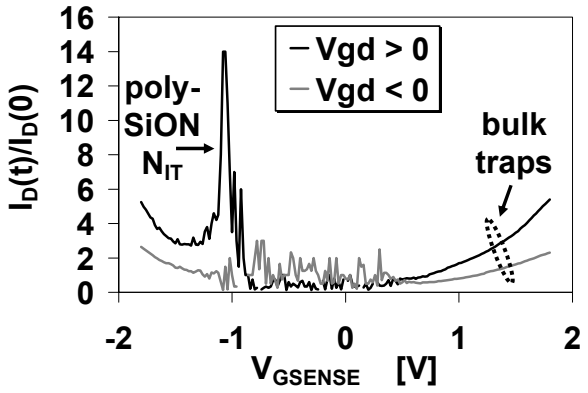

Figure 9. $I_D(t)/I_D(0)$ versus sense voltage after 1,000 C/cm^2 fluence. Only V_G is biased during the sense operation. V_D = +3.0 V and V_B = -2.2 V during stress. For $V_{GD} > 0$, V_G = +3.4 V during stress whereas for $V_{GD} < 0$, V_G = +2.6 V during stress.

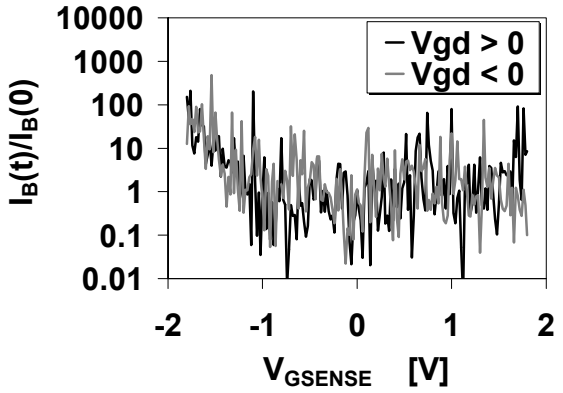

Figure 10. $I_B(t)/I_B(0)$ versus sense voltage after 1,000 C/cm^2 fluence. Only V_G is biased during the sense operation. V_D = +3.0 V and V_B = -2.2 V during stress. For $V_{GD} > 0$, V_G = +3.4 V during stress whereas for $V_{GD} < 0$, V_G = +2.6 V during stress.

$V_{GD} < 0$. The species liberated increases the density of bulk traps. No significant effect of V_{GD} on Si-SiON interface traps is observed, but this could be a resolution issue due to the low magnitude of I_B.

The cause for this puzzling behavior arises from the parasitic lateral NPN bipolar transistor formed between the injector (emitter), pwell (base), and drain (collector). Fig. 11 shows the ratio of I_D/I_{INJ} and I_B/I_{INJ} versus I_{INJ} with X_{INJ} as a parameter. At low I_{INJ}, I_B is primarily due to electrons from the forward biased injector diffusing out the substrate contact so that $I_B \sim I_{INJ}$. At high I_{INJ}, I_B drops sharply. This is a high level injection effect where the large concentration of electrons in the pwell results in an increase in the electric field, which enhances impact ionization in the drain space charge region. The created holes diffuse out the substrate contact, which oppose the electron flow and reduce I_B. The generated electrons increase I_D. Fig. 12 shows that at fixed X_{INJ}, increasing V_B also

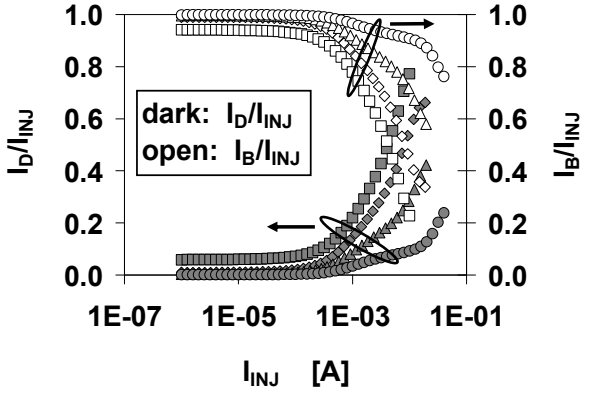

Figure 11. I_D/I_{INJ} (y1-axis) and I_B/I_{INJ} (y2-axis) versus I_{INJ} with X_{INJ} as a parameter. V_G = +3.4 V, V_D = +3.0 V, and V_B = -2.2 V. $X_1 < X_2 < X_3 < X_4$. Squares: X_1. Diamonds: X_2. Triangles: X_3. Circles: X_4.

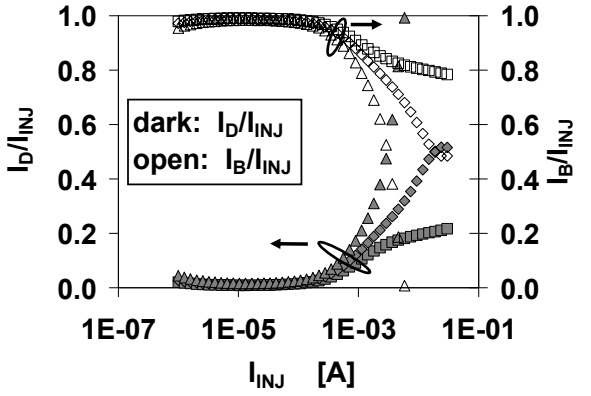

Figure 12. I_D/I_{INJ} (y1-axis) and I_B/I_{INJ} (y2-axis) versus I_{INJ} at fixed X_{INJ} with V_B as a parameter. V_G = +3.4 V and V_D = +3.0 V. Squares: V_B = -1.0 V. Diamonds: V_B = -2.0 V. Triangles: V_B = -3.0 V.

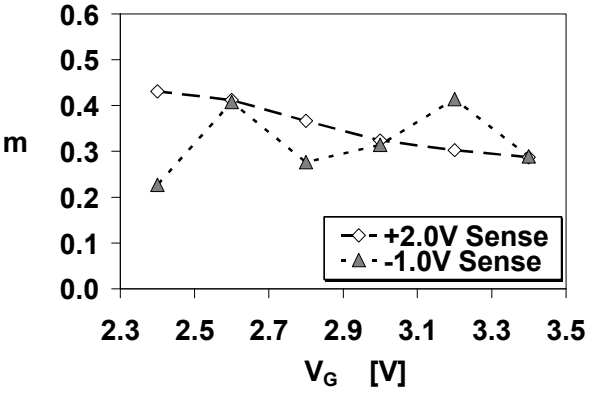

Figure 13. Trap generation power law exponents for constant V_{GD} = +0.4 V stress with V_B = -2.2 V, where parasitic bipolar effects have been minimized. V_G = +2.0 V senses bulk traps and V_G = -1.0 V senses interface traps.

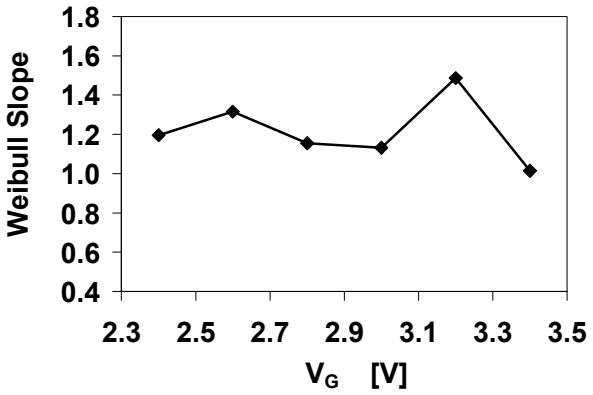

Figure 14. Weibull slopes for constant V_{GD} = +0.4 V SHE stress with V_B = -2.2 V where parasitic bipolar effects have been minimized.

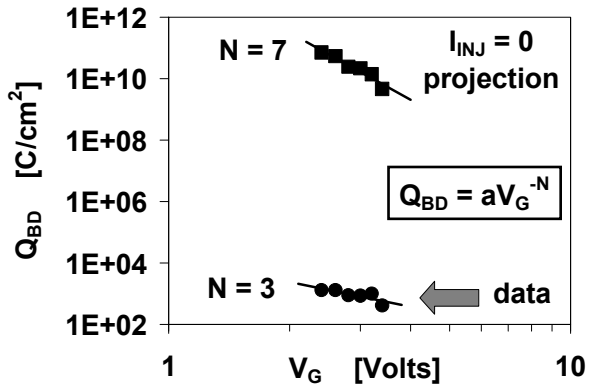

Figure 15. Q_{BD} versus V_G for constant V_{GD} = +0.4 V stress at V_B = -2.2 V where parasitic bipolar effects have been minimized.

increases high injection effects. The behavior seen in Fig. 11 and Fig. 12 is known as the Reverse Base Current Effect [20]. Some of the carriers that are generated through this process will impinge on the interfaces and affect trap generation. The value of I_{INJ} where this becomes significant decreases with decreasing X_{INJ} (the base width of the NPN is X_{INJ} in the idealized structure; it is larger when trench isolation separates the injector from the drain). Accordingly, the stress must be carefully optimized to obtain a robust reliability model. More generally, these parasitic bipolar effects need to be considered for any experiment where SHE is applied.

Trap generation power law exponents and Weibull slopes are shown in Fig. 13 and Fig. 14 respectively for an optimized constant V_{GD} = +0.4 V stress. β is independent of stress voltage and there are no abrupt changes in the trap generation reactions. Q_{BD} for the stress data, and current scaled to operating conditions using (2) are shown in Fig. 15. SHE accelerates Q_{BD} by about 7 orders of magnitude, corresponding to 14 orders of magnitude for t_{BD}. The V_G dependence of I_B(BTBT) at fixed V_{GD} results in a higher TDDB Power Law Model "N" for *projected* Q_{BD}. Nonetheless, the N = 7 TDDB Power Law Model exponent is lower than conventional on-state stress, indicating that V_B has more influence on the energy of the carriers that generate bulk traps than V_G. Projected to operating voltage, temperature, gate area, and cumulative fail fraction, gate dielectric reliability requirements can be met for sub threshold operation for an optimized SHE experiment that minimizes parasitic bipolar effects.

III. CONCLUSIONS

The dielectric reliability of devices operating in the low current sub threshold state was investigated using substrate hot carrier injection to accelerate breakdown. The trap generation mechanism was found to be due to two-electron vibrational excitation of silicon bonds for all conditions analyzed where an injector was utilized including the off-state, on-state, and sub threshold state. Consequently, extrapolating charge to breakdown to operating condition requires scaling of both current and voltage. A quantitative model was developed to enable reliability projections.

Applying SHE for accelerated TDDB stress introduces complexities in the data analysis. Under the high injection conditions that can arise during SHE stress, the parasitic lateral NPN bipolar transistor formed between the injector (emitter), pwell (base), and drain (collector) can give rise to the Reverse Base Current Effect that results in data that are not useful for reliability projections because the carriers created through the resulting impact ionization modify the reactions that lead to the generation of the trap states that cause breakdown. This in turn causes the Weibull slope to become stress voltage dependent. In general, parasitic bipolar effects should be carefully considered in *any* experiment where SHE is employed.

When properly optimized, SHE stress yields meaningful reliability assessments which showed that it is possible to meet reliability requirements for sub threshold operation; thus saving the cost of adding high voltage components.

ACKNOWLEDGMENT

The authors would like to thank Srikanth Krishnan, Steven Zuhoski, and James Ondrusek for their support of this work. We also appreciate useful discussions with Vijay Reddy and Gianluca Boselli.

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