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***Research Article***

# Effective Multiplexer Power-Delay Space Design using Generic 250 nm Device

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**Abstract**

High speed and low power is utmost requirement of today's VLSI systems and digital signal processing applications. In this paper, we have discussed 8-bit multiplexer design employing CMOS full adder, full adder using Double Pass Transistor and multi output carry Look ahead logic. DPL adder avoids the noise edge problem and speed deprivation at low value of supply voltages associated with complementary pass transistor logic circuits. Multi output carry look ahead adder leads to significant enhancement in the speed of the overall circuitry. The investigation is carried out with simulation runs on GENERIC 250 nm. Finally, the design guidelines are derived to select the most suitable topology for the desired applications. Investigation reveals that multiplexer design using multi output carry look ahead adder proves to be more speed efficient in comparison with the other two considered design strategies.

**Keywords:** Multiplexer; Generic 250 nm; CMOS; full adder.

## Introduction

Multiplexer plays an important role in today's digital signal processing and various other applications. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplexer design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption So, the need of high speed and low power multiplier has increased. Literature delineates outline and execution of fast multiplier [1,2]. Vedic mathematics based segments with different functional blocks can coordinate in an ALU to perform fast multiplication. The 1-bit full adder circuit is a very important component in the design of application specific integrated circuits. This paper presents a novel low-power multiplexer-based 1- bit full adder that uses 12 transistors (MBA-12T) [3,4]. High speed and low power MAC unit is utmost requirement of today's VLSI systems and digital signal processing applications like FFT, Finite impulse response filters, convolution etc. The efficiency of a system mainly depends on the performance of the internal components present in the system. So, the internal components must be designed in such a way that they should consume less power with increase in speed [5,6].

Multiplier modules are common to many DSP applications. The fastest types of multipliers are parallel multipliers. Among these, the Array multiplier is the basic one. However, they suffer from more propagation delay.This paper presents the methods required to implement a high speed and high performance parallel complex number multiplier. The designs are structured using Radix-4 Modified Booth Algorithm and Wallace tree [7,8]. Real time applications such as controlling environmental conditions demand quick response of the processor for processing the acquired signals. Multiplier is an important feature of signal processing. Atypical processor central processing unit devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction [9].

Reversible logic circuits are of interests to power minimization having applications in

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low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In this paper we propose a novel 4x4 bit reversible multiplier circuit. MKG gates was used to construct the reversible multiplier circuit.The proposed reversible multiplier circuit can multiply two 4-bitsbinary numbers. It can be generalized for NxN bit multiplication [10].

**Existing system**

***CMOS full adder***

CMOS full adder design is implemented using stack of PMOS and NMOS transistors. The basic architecture of full adder design consists of 28 transistors and three input variables (a, b and c) and two output variables (sum and carry) of 1-bit each. The two outputs of the adder sum and carry are represented as eq. (1).

$$\text{Sum} = a \oplus b \oplus c \quad \text{Carry} = a.b + b.c + c.a \quad (1)$$

The 8-bit ripple carry adder consists of eight full adder cells in cascade such that output carry of one full adder cell is applied as an input carry to another full adder cell. Multiplication is one of the most fundamental arithmetic operations; it finds application in Digital Signal processing. In this section 8-bit multiplier design is addressed.

***Double pass transistor adder***

The multiplier is designed using the three adders used for partial product addition i.e., Full adder using Double Pass Transistor (DPL) and multi output carry Look ahead logic (CLA). The 8-bit multiplier design comprises a 4 × 4 multiplier and an 8-bit adder for partial product addition as shown in A 4 × 4 array multiplier is designed using full adder cells and AND logic gates using static CMOS. The 4 × 4 array multiplier is depicts the schematic of Full adder using DPL adder shown in figure 1 compensates for the speed degradation of CMOS pass transistors in two ways as demonstrated.

It is a symmetrical arrangement in which any input is connected to the gate of one MOSFET and the source of another. Among the inputs any of A, A′, B, and B′ (A′ represents complement of A) is connected to the gates of NMOS transistor and to the sources of the NMOS and PMOS transistors. This results is shown in figure 2. The balancing of input capacitance therefore, reducing the delay time dependency on the data. Second is the double transmission characteristic of DPL. This results in two outputs, one in normal form and another in complementary form.

There are two inputs for each variable (*a, anot), (b, bnot) and (c, cnot)*. Complementary outputs are *sum*, *sumnot* and *carry*, *carrynot*. The output *sum* of the full adder cell consists of XOR/XNOR logic gates, a multiplexer which has four inputs, two select lines *c* and *cnot*, two outputs complementary in nature, and an output buffer developed using CMOS logic. The output *carry* of the adder consists of AND/NAND logic gates, OR/NOR logic gates, a multiplexer, and a CMOS output buffer. Table 1 depicts the performance summery of 8-bit multiplexer design analyzed in this paper and their performance characteristics are plotted in figure 3.

**Proposed system**

***Multiplexer***

A Multiplexers (MUX) is a combinational logic component that has several inputs and only one output. MUX directs one of the inputs to its output line by using a control bit word (selection line) to its select lines. Multiplexer contains the followings: o data inputs o selection inputs ‘o’ a single output ‘o’ Selection input determines the input that should be connected to the output. The multiplexer sometime is called data selector. The multiplexer acts like an electronic switch that selects one from different. A multiplexer may have an enable input to control the operation of the unit.

***Multi output carry look ahead adder***

In order to achieve high-speed in arithmetic operation, carry propagation time is the deciding factor as it limits the speed of the whole logic circuit which increases with the size of the adder. For n-bit Parallel adder,

$$\text{Total propagation delay} = S + (n-1)\,C \quad (2)$$

where S is propagation delay of sum and C is propagation delay in carry. In parallel adders (ripple carry adder), carry propagates in series or ripple which increases with size of adder. Carry propagation time can be reduced by two ways as demonstrated. One solution is to develop faster gate with reduced delays.

Another solution is to reduce the carry propagation delay at the cost of increasing the

 

complexity of design. For reducing the carry propagation time in a parallel adder, several techniques are used out of which Carry look-ahead adder logic is most widely used. Recently shown that the 8-bit CLA adder was used Manchester Carry Chain (MCC) in multi output domino CMOS logic. The design includes two carry chains i.e. even and odd carry using series connected transistors. The MCC is the most commonly used domino CPL design as demonstrated. The recursive properties of the carries have developed the multi output domino gates.

Table 1. Performance summery of 8 bit multiplexer

| Vdd (volts) | Scheme | Delay (ns) | Power (mW) | Power delay Product |
|---|---|---|---|---|
| 0.5 | CMOS | 6.193 | 0.157 | 1.261 |
| | DPL | 5.025 | 0.223 | 1.500 |
| 0.7 | CMOS | 5.543 | 0.329 | 1.379 |
| | DPL | 3.672 | 0.439 | 1.496 |
| 0.8 | CMOS | 3.440 | 0.632 | 2.346 |
| | DPL | 2.230 | 0.765 | 2.134 |
| 1 | CMOS | 1.532 | 1.762 | 3.320 |
| | DPL | 1.865 | 1.794 | 3.564 |

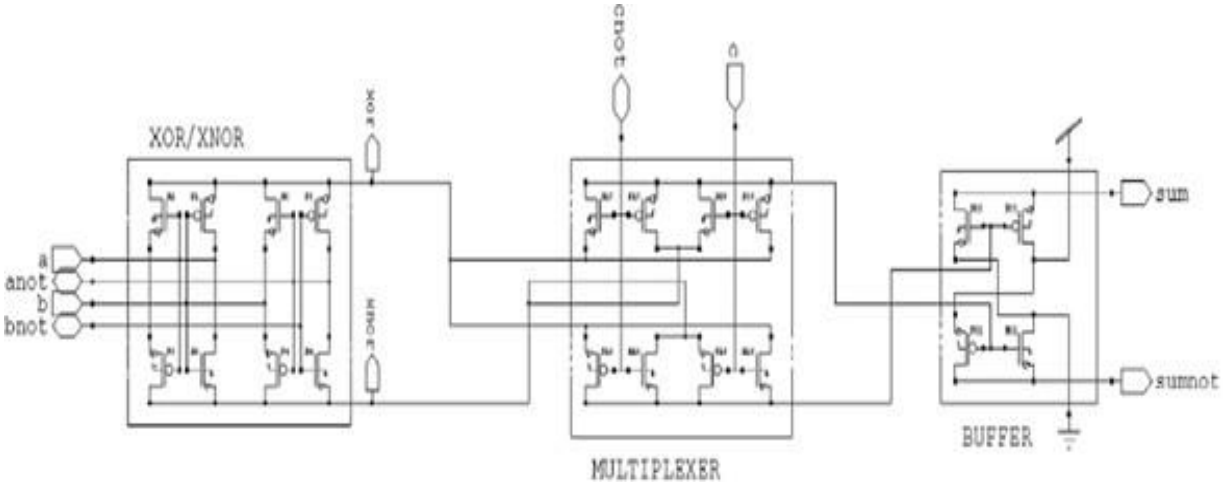


Figure 1. DPL one bit full adder cell

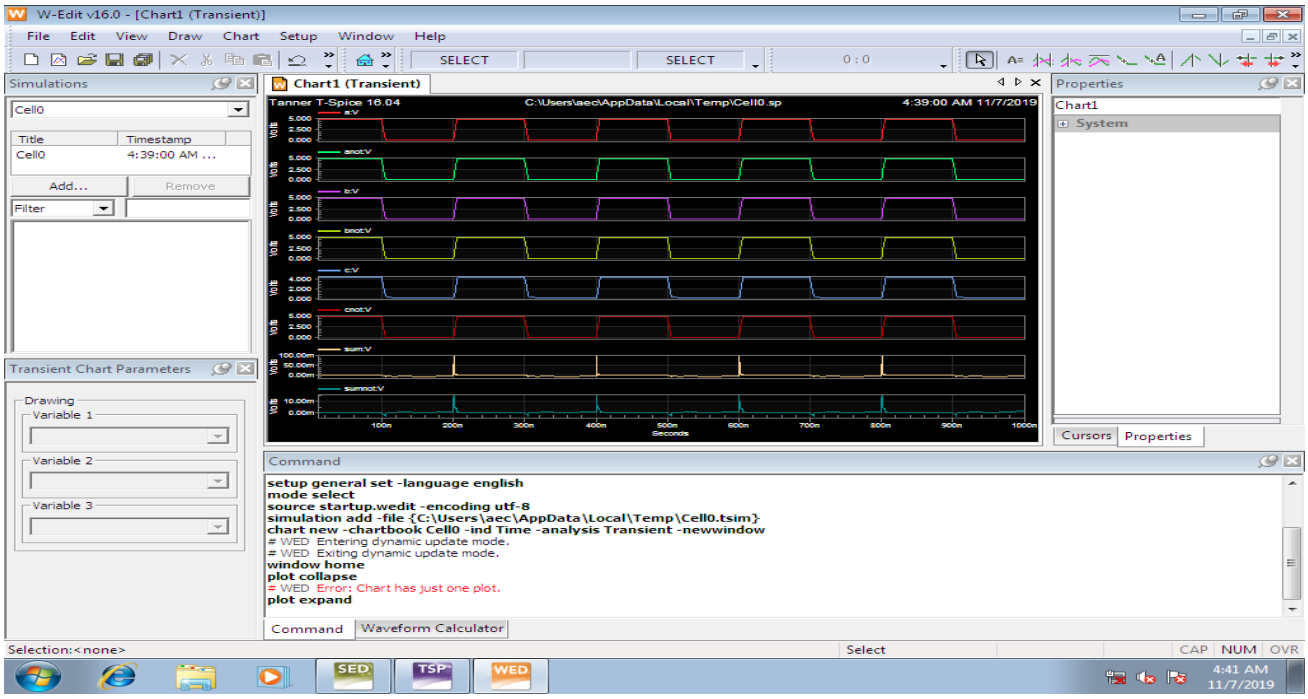


Figure 2. DPL One Bit Full Adder cell output waveform

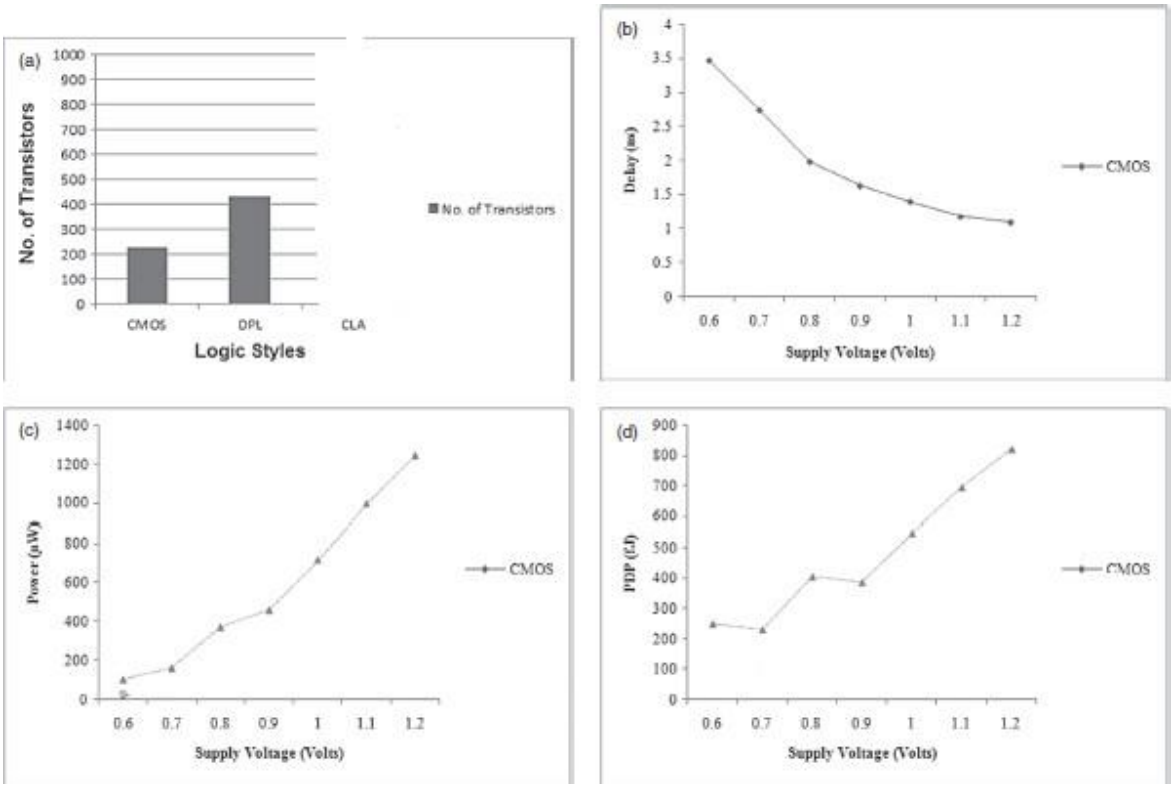


Figure. 3. Comparison analysis of multiplexer (a) Transistor count (b) Delay versus VDD (c) Power versus VDD

## Conclusions

The present work has proposed speed efficient multiplexer architecture designed using double pass transistor logic adder. Further, we have carried out a comparison among the multipliers employing latest adder architectures. The comparison results are obtained in power-delay space. Thus, the design guidelines are derived to make the selection of appropriate multiplier design at the beginning of the design process. At VDD = 0.5 V the 8-bit multiplexer designed using DPL adder has 26.39% less delay than the multiplier with CMOS full adder and 13% improvement in delay as compared to multiplier designed using DPL adder.

## Conflict of interest

The authors declare no conflict of interests.

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