# VHDL IMPLEMENTATION OF COMBINATIONAL CIRCUITS BY USING REVERSIBLE DECODER

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***Abstract*—**In present era reversible logic is the emerging field for research. The aim of this paper is to realize different types of combinational circuits like multiplexer and code converters using reversible logic gates with minimum quantum cost. Reversible decoder is designed using reversible logic gates with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, TR Gate and many more. Reversible logic is defined as the logic in which the number output lines are equal to the number of input lines i.e., the n-input and k-output is said to be reversible if and only if (i) n is equal to k and (ii) each input pattern is mapped uniquely to output pattern. The gate must run forward and backward that is the inputs can also be retrieved from outputs. Fan-out and Feed-back are not allowed in Logical Reversibility. Reversible Logic owns its applications in various fields which include Quantum Computing, Nano- technology, Computer Graphics, low power VLSI Etc., The comparative study in terms of garbage outputs, Quantum Cost, numbers of gates are also presented. The Circuit has been designed and simulated by using Xilinx software.

***Keywords-*** *Number of Gates; Reversible Gates; Garbage Outputs; Quantum Cost.*

## I. INTRODUCTION

Power Consumption has become a very important factor for consideration in present VLSI technology. Designing Combinational circuits by using reversible decoder power consumption is reduced. Ralf Launduer told heat dissipation is not because process in the operation, which is equal to KTln2 joules. Later in 1973 C.H. Bennett described the Power dissipation due to the bit loss each computation in circuit was carried out in reversible manner. Each gate perform a unitary operation, wouldn't occur if the computation is carried out in reversible manner. The amount of heat dissipated in the system holds a direct relationship. Reversible Logic finds its own application in Quantum
computing, Nano-technology, optical computing, computer graphics and low Power VLSI. The amount of heat dissipated in the system holds a direct relationship to the

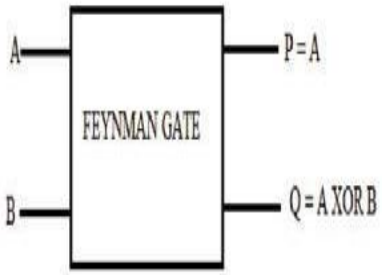
number of bits erased or lost during the computation.

## II. CONCEPT

The Reversible Logic involves the use of Reversible Gates consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vectors and output vectors. Certain limitations are to be considered when designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedback is also not permitted in reversible logic. In Reversible logic using outputs we can obtain full knowledge of inputs. Reversible logic conserves information. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are kept alone without performing any operations. Number of gates count is not a good metric since more number of gates can be taken together to form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement the gate. It is nothing but the number of reversible gates (1×1 or 2×2) required to construct the circuit. Delay is one of the important cost metrics. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research.In this paper, the design of different combinational circuits like Multiplexer circuits, Code converters using Reversible logic gates is proposed with optimum Quantum cost.

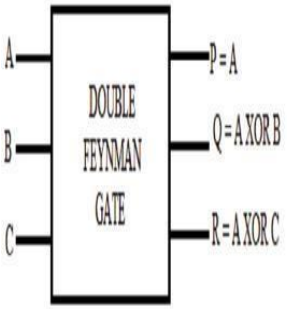
*Fig. 1: NOT Gate and its Truth Table*


| A | P |
|---|---|
| 0 | 1 |
| 1 | 0 |



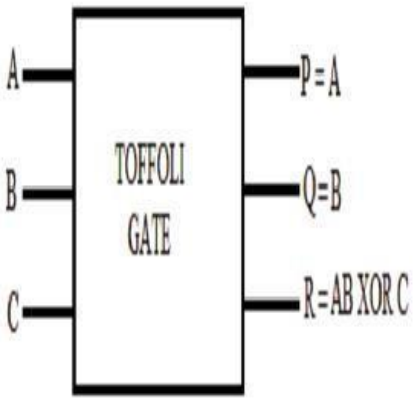

| A | B | P | R |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

*Fig. 2: Feynman Gate and its Truth Table*




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

*Fig.3:Double Feynman Gate and its Truth Table Fig.4 :Toffoli Gate and its Truth Table*




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

Reversible Logic Gates

The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

NOT GATE: The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero as shown in the figure1. Feynman Gate (Fg): Feynman Gate Is A 2×2 Reversible Gate As Shown In Below Figure2. The Feynman Gate Is Also Called As CNOT Gate I.E., Controlled NOT Gate. The Feynman Gate Is Used To Duplicate Of The Required Outputs. The Quantum Cost Of FG Is 1. This Is Also The Primitive Gate Owing Its Importance In Determining Quantum Cost Metric.

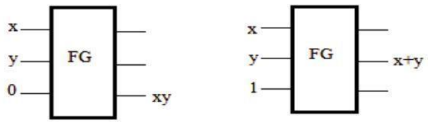
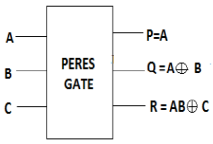



*Fig.5: Fredkin Gate and its Truth Table*

Double Feynman Gate (Dfg): Double Feynman Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure3. The quantum cost of DFG is 2. *Toffoli Gate(Tg): Toffoli Gate is 3×3 reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of TG is 4*

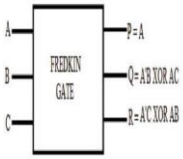
Fredkin Gate (Fdg): Fredkin Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of FDG is 5. Peres Gate (Pg): Peres Gate is a is a 3×3 reversible gate. The outputs are defined as shown in the below figure6. The Quantum Cost of PG is 4.




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

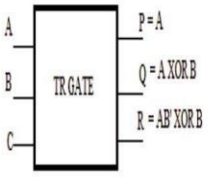
*Fig.6 :Peres Gate and its Truth Table*

TR GATE: TR Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure7. The quantum cost of TRG gate is given by 4




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

*Fig.7 :TR Gate and its Truth Table*




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

*Fig.8: AND Gate and OR Gate using fredkin*

Considering our circuit requirements we need to design AND gate and OR gate using reversible gates. Here we used fredkin gate to design AND and OR gates as shown in figure. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.

## III. EXISTING METHOD

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like code converters, multiplexers, decoders etc., in the existing method the author has given a novel design of 2x4 decoder whose Quantum Cost is less than the previous design. Using fredkin gates for designing 3×8 decoder as shown in figure9. The whole design is done using Fredkin, Feynman gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 3x8 decoder are 12 in which there are 6 fredkin gates and 6 feynman gates. The sum of all the quantum costs of each gate gives total quantum cost of 3x8 decoder.

Basic Gates Using Reversible Gates

Different Reversible Decoder circuits like 2×4, 3×8 decoders are designed using Fredkin Gates, Feynman gates. Some combinational circuits like code convrters, multiplexers etc., are designed using these decoders. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed.

## IV. SIMULATION RESULTS OF PROPOSEDCIRCUITS

### *A.* 2×4 Decoder

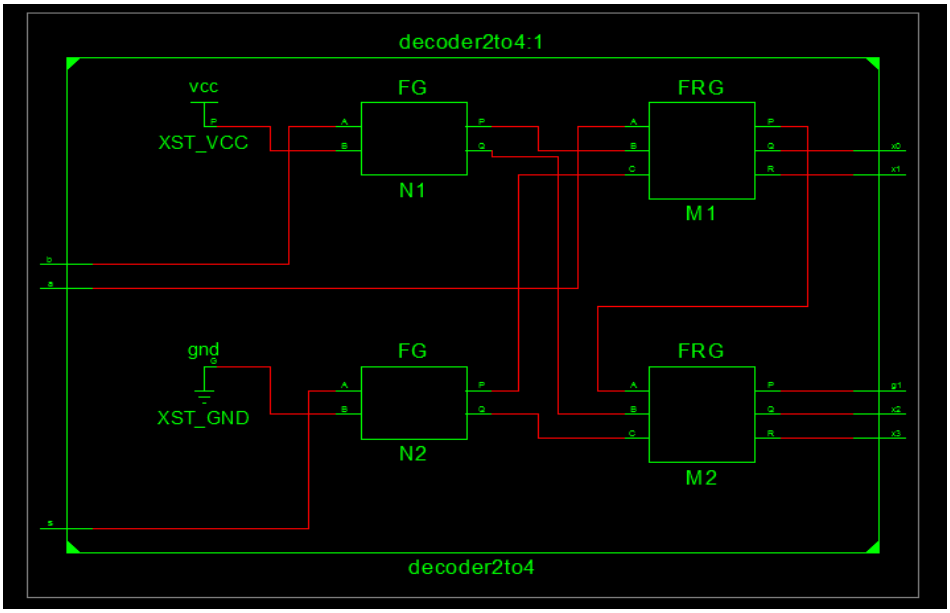




*Fig.10: RTL Schematic of 2×4 reversible decode*

*A.* 3×8 Decoder

*Fig.12: RTL Schematic of 3×8 decoder*

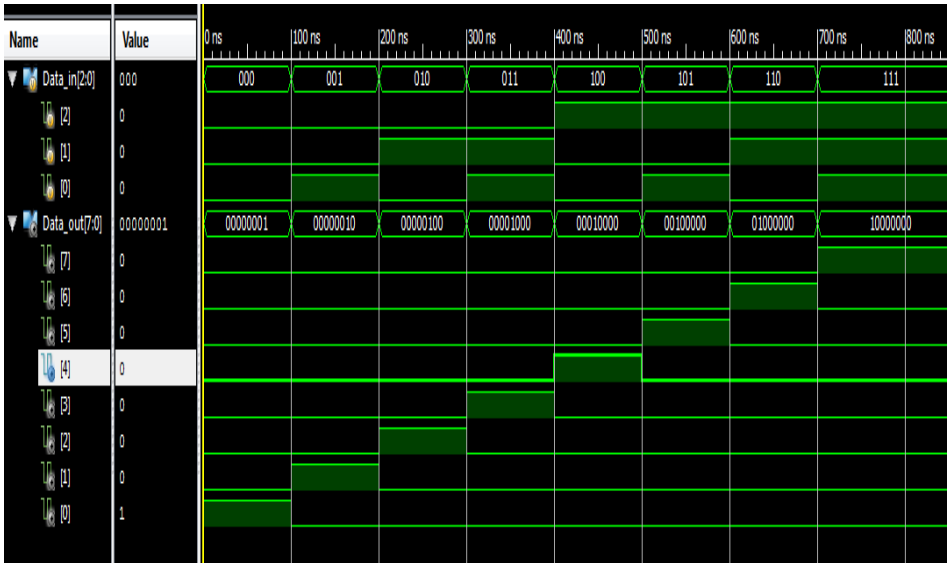



*Fig.11: simulated output for 2×4 decoder*

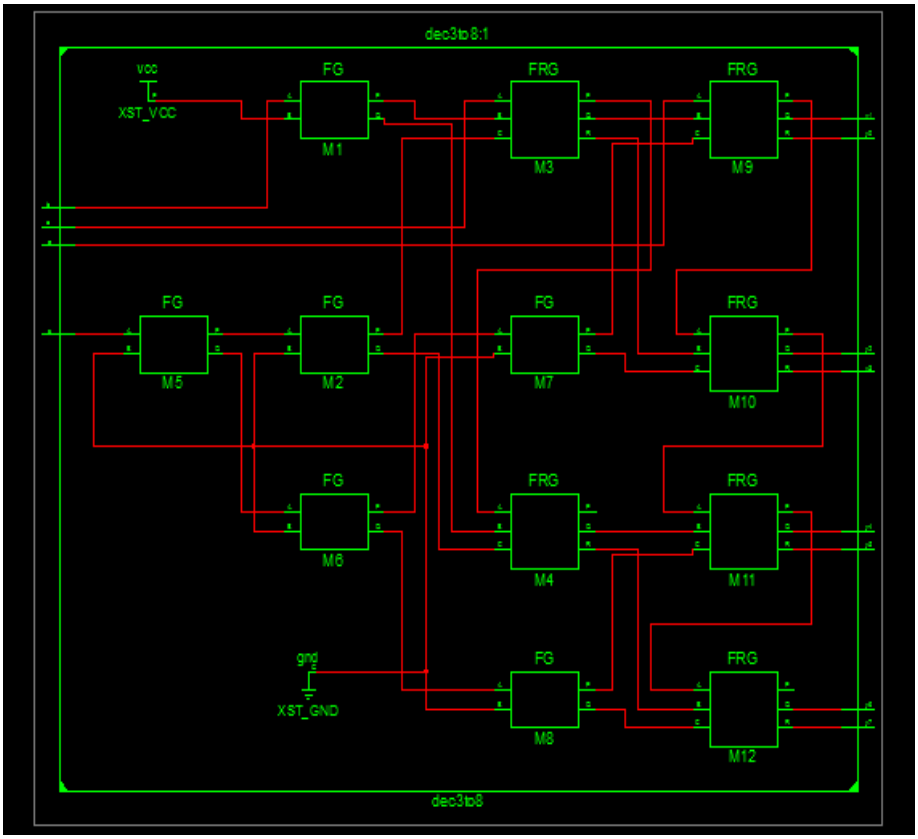



*Fig.13 :Simulated output for 3×8 decoder*

*B.* Gray To Binary Converter

Designing of reversible logic circuit is challenging task, since not enough number of gates are available for design. Reversible processor design needs its building blocks should be reversible in this view the designing of reversible code converters became essential one.

The Most Significant Bit (MSB) of the binary code is always equal to the MSB of the given binary number.To get the next straight binary bit, it uses the XOR operation among the primary bit or MSB bit of binary to the next bit of the gray code. Similarly, to get the third straight binary bit, it uses the XOR operation among the second bit or MSB bit of binary to the third MSD bit of the gray code and so on.

*Fig.15: Simulated output for gray to binary*

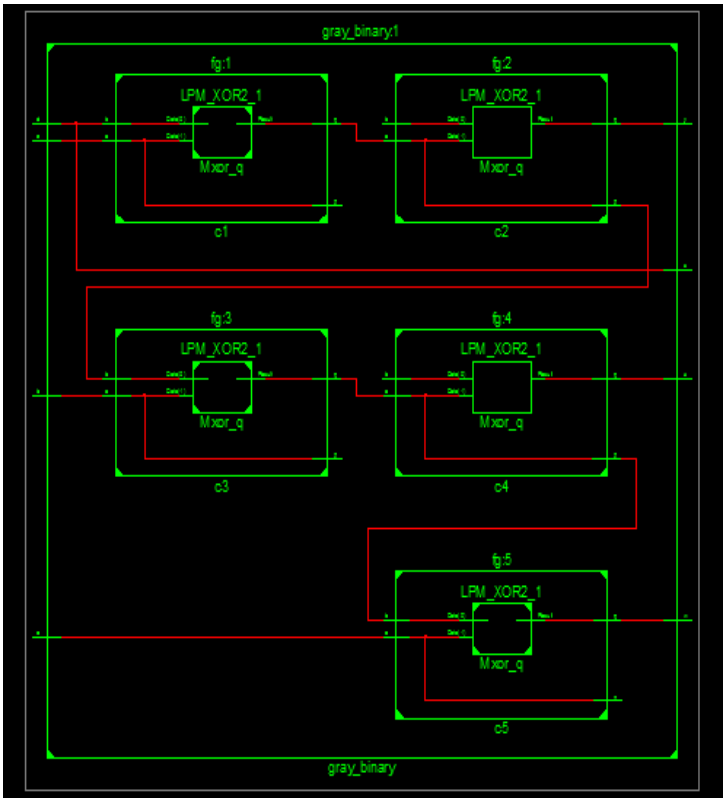



*Fig 14: RTL Schematic of gray to binary*

*C.* Binary To Gray Converter

Binary to Gray code converters used to reduce switching activity by achieving single bit transition between logical sequences. In the digital domain, data or information is represented by a combination of 0's and 1's. A code is basically the pattern of these 0's and 1's used to represent the data. Code converters are a class of combinational digital circuits that are used to convert one type of code in to another.

If Input vector is I(D,C,B,A) then the output vector o(Z,Y,X,W). The circuit is constructed with the help of Feynman Gate (FG) gate. The Most Significant Bit (MSB) of the gray code is always equal to the MSB of the given binary code. Other bits of the output gray code can be obtained by XORing binary code bit at that index and previous index.

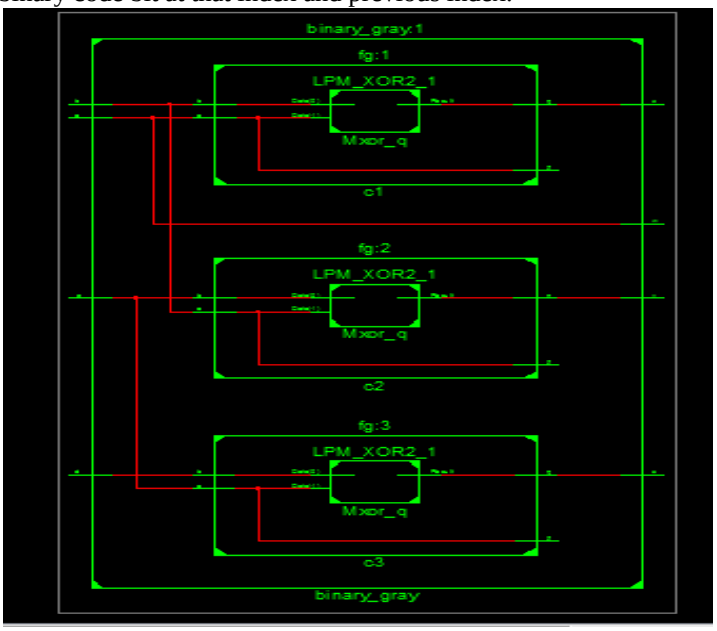



*Fig.16: RTL Schematic of binary to gray*

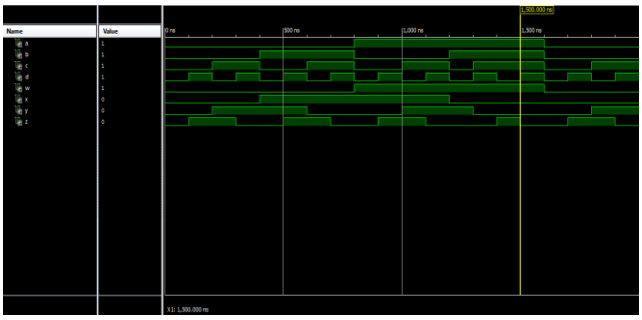


*Fig.17: Simulated output for binary to gray*

*D.* Multiplexer

To design a multiplexer using reversible decoder, reversible 2 input AND gates, 2 input OR gates are required. The 2 input AND Gate and OR gate are designed using Fredkin gate. By using these designed gates we can improve those gates to the required number of input gate. Each output line from decoder is driven to 2 input AND gate along with multiplexer input. The outputs of all AND gates are made to drive to that particular input OR gate. The input binary integer values act as the selection lines. Similarly by using 16×1mux and 2×1mux a 32×1 multiplexer is designed.

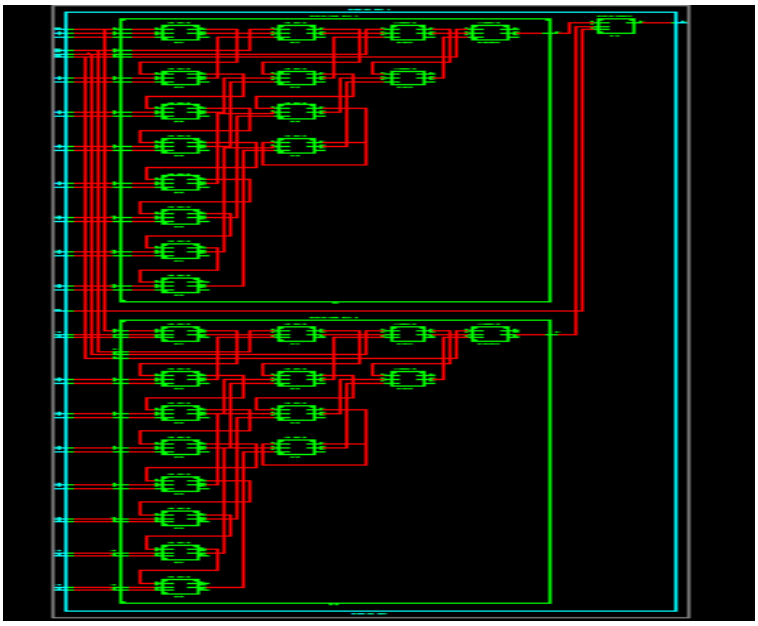


*Fig.18: RTL Schematic of 32×1 multiplexer*

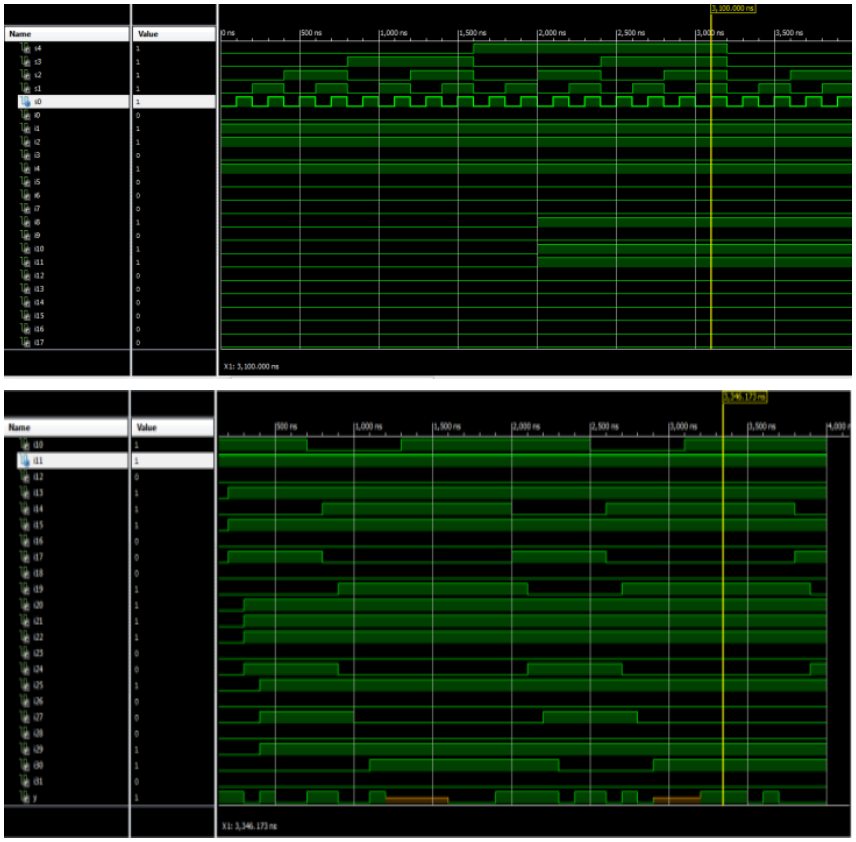


*Fig.19: Simulated output for 32×1 multiplexer*

## V. COMPARATIVE STUDY

The combinational circuits designed using reversible decoder are analyzed in terms of Quantum cost and Garbage outputs.

| CIRCUIT | QUANTUM COST | GARBAGE OUTPUTS |
|---|---|---|
| 2 TO 4 DECODER | 12 | 3 |
| 3 TO 8 DECODER | 36 | 6 |
| GRAY TO BINARY | 5 | 3 |
| BINARY TO GRAY | 3 | 3 |
| 32×1 MULTIPLEXER | 81 | 54 |

## VI. CONCLUSION

In this paper, different combinational circuits like multiplexer, code converters circuits constructed using reversible decoder are designed. These circuits are designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the decoder circuit can be generalized. The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance for minimum quantum cost.

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