LOW POWER LFSR WITH BIST

[1]Pavan Billa,[2]B. Jamuna
[1]*Reasearch scholar, Department of ECE, Tegala Krishna reddy college, Hyderabad*
[2]*Assistant Professor, Department of ECE, Tegala Krishna reddy college, Hyderabad*

Abstract- Testing of digital VLSI circuits entails many challenges as a consequence of rapid growth of semiconductor manufacturing technology and the unprecedented levels of design complexity and the gigahertz range of operating frequencies .There is limitations of peak power dissipation and test application time. Pseudo- random- pattern generator PRESTO (pre selecting toggling) is the proposed technique which uses new observations concerning the output sequence of an LFSR to design a low-transition test pattern generator for test-per-clock built-in self –test to achieve reduction in the overall switching activity in circuit-under-test (CUT).The results obtained shows low power reduction for proposed system .We have carried the simulation and verified the results using ISE simulator and synthesis is done on the XILINX ISE.

Keywords – *PRESTO; PRPG; LFSR; BIST; TPG*

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits the novel test pattern generator which is more suitable for built in self-test (BIST) structures used for testing of VLSI circuits. This paper describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired deterministically monitor the generator near test classifications with fault-coverage-to pattern- count ratios. Additionally, this paper recommends low power test compression that permits determining the test power envelope in a completely expectable, correct, and elastic manner by adjusting the PRESTO-based logic BIST (LBIST) infrastructure [6].Another method focusing on modifying LFSRs. The pattern in [7] decreases the power in the CUT in communal and clock tree in specific. In [8], a low-power

BIST for data path structural design is suggested, which is circuit needy. Toggling levels and improved fault coverage gradient associated with the best-to-date built-in self-test (BIST)-based pseudorandom test pattern generators. It is included of a linear finite state machine (a linear feedback shift register or a ring generator) driving suitable phase shifter, and it originate switch a sum of structures permitting this device to yield binary sequences with preselected toggling (PRESTO) activity. We present a technique to mechanically choice some panels of the generator contribution informal and exact tuning.

The similar method is then active to deterministically monitor the generator to test sequences with better fault-coverage-to pattern- count ratios. Additionally, this paper suggests an LP test compression method that permits shaping the test power envelope in a completely expectable, precise, and flexible style by familiarizing the PRESTO-based logic BIST (LBIST) infrastructure [6]. Additional method absorbed on adapting LFSRs. The scheme in [7] decreases the power in the CUT in general and clock tree in precise. In [8], a low-power BIST for data path construction is planned, which is circuit reliant on.

Though, this dependence implies that no detecting sub sequences must be resolute for each circuit test sequence. Bonhomie et al [9] useda clock though complete the next years, the primary objective of manufacturing test will remain essentially the same to ensure reliable and high quality semiconductor products conditions and consequently also test solutions may undergo a significant evolution. The semiconductor technology, design characteristics, and the design process are among the key factors that will impact this evolution. with new types of defects that one will have to consider to provide the desired test quality for the next technology nodes such as 3-d, it is appropriate to pose the question of what matching design-for-test methods will need to be deployed test compression.

II. PRESTO SCHEME

Fig. 1 shows he basic architecture of PRESTO generator .A *n*-bit PRPG is connected with phase shifter to produce the actual pseudorandom test patterns.

PRPG is implemented using a linear feedback shift register or ring generator, between the PRPG and the phase shifter *n* hold latches are placed. Each hold latch is controlled by an *n*-bit toggle control register. The toggle control register controls the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode,0s indicates the latches in hold mode.

The toggle mode is transparent for data arriving from the PRPG and their fraction determines a scan switching activity. With the content of an additional shift register the control register is reloaded once per pattern. The weights are

determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing probabilities beyond powers of 2. A 4-bit Switching register is employed to activate AND gates, and allows selecting a user-defined level of switching activity. An additional 4-input NOR gate is used to switch the LP functionality off.

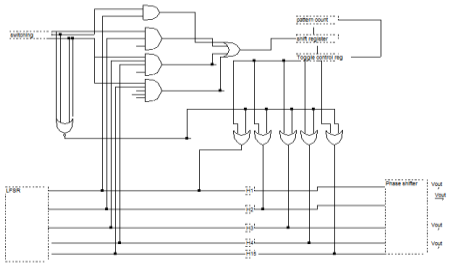

Fig.1: Basic architecture of PRESTO

Linear Feed Back Shift Register (LFSR)

A linear feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The only linear function of single bits is xor, thus it is a shift register whose input bit is driven by the exclusive-or (xor) of some bits of the overall shift register value.

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops.

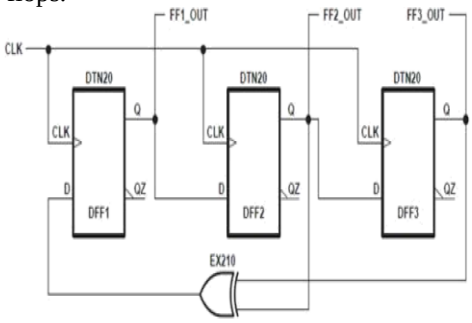

Fig.2: LFSR Architecture

III. FULLY OPERATIONAL GENERATOR

Much higher flexibility in forming low-toggling test patterns can be achieved by deploying a scheme presented in Fig. 2. Essentially, while preserving the operational principles of the basic solution, this approach splits up a shifting period of every

test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a T-type flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND gates on the control register outputs to allow freezing of all phase shifter inputs.

This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the control register can pass test data moving from the PRPG to the scan chains.

Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a manner similar to that of weighted logic used to feed the shift register. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator.

For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register, which determines when to terminate the hold mode.

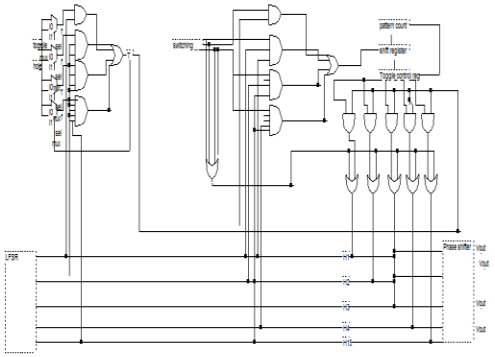

Fig.3: Fully operated PRESTO

A. Switching Activity

Switching activity is essential to measuring power in digital circuits, and it is also important for optimizing digital designs. Power can be static, caused by leakage, or dynamic, caused by switching. Switching activity is crucial because dynamic power is, after all, proportional to the switching activity in the design. Switching activity is the measurement of changes of signal values. It has two parts: probability and toggle density.

B. Probability

In this context is the likelihood that a signal will have the logic value of '1'. A zero probability indicates that the signal is always low.

C. Toggle density

Toggle density is the number of switches per unit time. That unit is generally one clock Cycle. Toggle density is the 'f' in the formula for dynamic power in CMOS circuits.

$$P(\text{dynamic}) = \tfrac{1}{2} C V^2 f.$$

It is the toggle density that is primarily used for power analysis and optimization. Switching activity is a critical element of power analysis and power optimization. For power analysis, switching activity provides a key piece of the power equation.

D. Pattern Counter

In digital logic and computing, a counter is a device which stores the number of times a particular event or a process has occurred, often in relationship to a clock signal. The most common type is Sequential Digital logic circuit with an input line called "Clock" and multiple output lines.

E. Phase Shifter

phase shifter is used to change the phase of the arriving data . phase shifter output is obtained by XOR-ing outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output.

F. Toggle control register

The toggle control register controls the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, 0s indicates the latches in hold mode.

G. Toggle Mode

If the given latch is transparent for data going from the ring generator to the phase shifter as long as its enable input is asserted. It is said to be in the toggle mode.

H. Hold Mode

When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of the generator, thus driving the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode.

The toggle mode is transparent for data arriving from the PRPG and their fraction determines a scan switching activity. With the content of an additional shift register the control register is reloaded once per pattern. The weights are determined by four AND gates producing 1s With the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing probabilities beyond powers of 2. A 4-bit Switching register is employed to activate AND gates, and allows selecting a user-defined level of switching activity. An additional 4-input NOR gate is used to switch the LP(low power) functionality off.

PRESTO Generator controls As shown in the previous sections, performance of the PRESTO generator depends primarily on the following three factors (note that in the BIST mode they are delivered only once, at the very beginning of the entire test session):

1) the switching code (kept in the switching register)
2) the hold duty cycle (HC)
3) the toggle duty cycle (TC)

Low power Decompressor

Embedded cores are becoming commonplace in large system-on-a-chip (SOC) designs. Along with the benefits of higher integration and shorter time to market, intellectual property (IP) cores pose several difficult test challenges. The volume of test data for an SOC is growing rapidly as IP cores become more complex and an increasing number of these cores are integrated in a chip. In order to effectively test these systems, each core must be adequately exercised with a set of pre-computed test patterns provided by the core vendor. However, the input/output (I/O) channel capacity, speed and accuracy, and data memory of automatic test equipment (ATE) are severely limited.

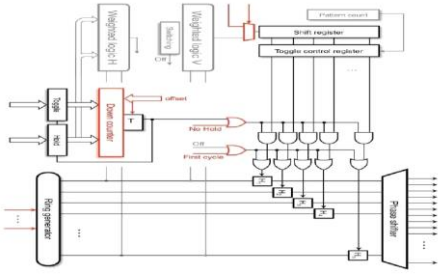

Fig.4: LP decompressor architecture

The initial value of the T flip flop decides whether the decompressor will begin to operate either in the hold mode or in the toggle mode, while the initial value of the counter, determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases. First, the encoding procedure may completely disable the hold phase by loading the Hold register with an appropriate code, for example, 0000. If detected that there is no Hold signal, it overrides the output of the T flip-flop by using an additional OR gate. Therefore, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle produced at the end of the

ring generators initialization phase reload all latches with the current content of this part of the de-compressor.

IV. EXPERMENTAL RESULTS

Simulation results are useful to check whether the outputs are coming as expected or not while running. It will be useful for the user to verify the outputs in advance and then building an appropriate circuit physically only if the simulation results are obtained as expected.

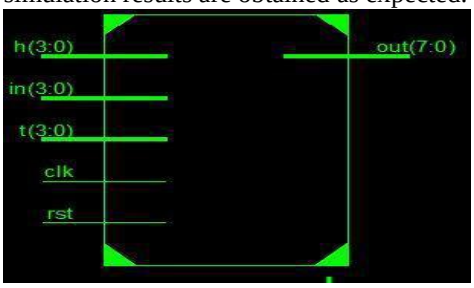

Fig.5: Block diagram of fully PRESTO

Fig 6 shows the output waveforms of the PRESTO module. By using multiple sic vector scheme, only single bit is going to change such that we can reduce the power consumption in generating scan chains because only one flip-flop is in active at a time.

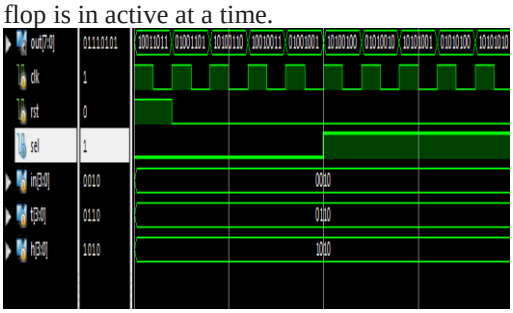

Fig.6: Simulation Results for fully PRESTO

V. CONCLUSION

This paper has proposed test vector generation for power optimization as we are using one bit change test vectors to reduce the switching power dissipation. By using multiple SIC vector scheme, only single bit is going to change such that we can reduce the power consumption in generating scan chains. Because only one flip flop is in active at a time. For a test-per-clock scheme, the MSIC-TPG uses its one bit change vectors as inputs to the CUT with the SRAM-like grid. This paper presents the novel implementation of all the one- bit change approach based test vector generator by using verilog language. Synthesizing and simulation of the code is carried out on Xilinx - Project Navigator, ISE suite.

REFERENCES

[1]. MichałFilipek, GrzegorzMrugalski, Nilanjan Mukherjee, Benoit Nadeau-Dostie, JanuszRajski, Je˛drzejSolecki, and Jerzy Tyszer, "Low-Power Programmable PRPG With Test Compression Capabilities" in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 6, JUNE 2015

[2]. Feng Liang, Luwen Zhang, Shaochong Lei, Guohe Zhang, KaileGao, and Bin Liang "Test Patterns of Multiple SIC Vectors: TheoryandApplication in BIST Schemes" in IEEE transactions on very large scale integration (vlsi) systems, Vol. 21, No. 4, April 2013

[3]. Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in 11th Annu. IEEE VLSI Test Symp. Dig. Papers, Apr. 1993,pp. 4–9.

[4]. J. Rajski, J. Tyszer, G. Mrugalski, and B. Nadeau-Dostie, "Test generator with preselected toggling for low power built-in self-test," in *Proc. IEEE 30th VLSI TestSymp. (VTS)*, Apr. 2012, pp. 1–6.

[5]. A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 28, no. 5, pp. 755–759, May 2009.

[6]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras,S. Manich, P. Teixeira, and M. Santos, "Low-energy BIST design: Impact of the LFSR TPG parameters on the weighted switching activity,"in Proc. IEEE Int. Symp. Circuits Syst.,vol. 1.Jul. 1999, pp.110–113.

[7]. S. Wang and S. K. Gupta, "LT-RTPG: A new test-per-scan BIST TPG for low switching activity," IEEE Trans. Comput.-Aided Design Integr. ircuits Syst., vol. 25, no.8, pp. 1565–1574, Aug. 2006.

[8]. F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante,"Low power BIST via non-linear hybrid cellular automata,"in Proc. 18th IEEE VLSI Test Symp., Apr.–May 2000, pp.29–34.

[9]. B. Cowan, O. Fransworth, P. Jakobsen, S. Oakland, M. R. Ouellette, and D. L. Wheater, "Onchip repair and an ATE independent fusing methodology," in Proc. Int. Test Conf. (ITC), Oct. 2002, pp. 178 -186.

[10]. MichałFilipek, GrzegorzMrugalski, Nilanjan Mukherjee, Benoit Nadeau-Dostie, JanuszRajski, Je˛drzejSolecki, and Jerzy Tyszer, "Low-Power Programmable PRPG With TestCompression Capabilities" in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 6, JUNE 2015