Design and Simulation of Charge Transport in Single Electron Transistor Using Tcad Numerical Simulator

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Abstract- The ability to control the flow of electron of a MOSFET is decreased due to quantum mechanical effect when scaled down below 50 nm .To compete this challenge a new field of device research is needed. One such area is devices based on tunneling phenomena called as single electron devices. In this paper a most fundamental single electron device, single electron transistor (SET) is designed using visual TCAD with gate length of 2nm and gate width of 2nm. The channel is ultra thin with length of 2nm and width of .005 nm and channel thickness is .3nm.Then a Si quantum dot of size .5*1.6nm2 is used between the island and gate. Both the Devices are simulated using Genius Simulator successfully. It is found that at room temperature the device with Si dot is more promising. Device with Si dot have less capacitance and higher charging energy than device without Quantum dot.

Keywords- Quantum tunneling, Coulomb blockade (CB), quantum dot (QD), single electron transistor (SET).

I. INTRODUCTION

The manipulation of single electrons was demonstrated by Millikan in the beginning of 20th century by Millikan. In the late 1980s it was implemented for solid state circuits because its reproducible fabrication is required for small size conducting particles, and their exact place averse to external electrodes. The growth in techniques of nanofabrication in the last three decades facilitates a new branch of solid state physics called single-electronics [1].

SET is essential in single electronics where the device operation depends on the effect of Coulomb blockade and can be designed at very small scale. However, the voltage gain provided by SET is low, input impedances is high and it is sensitive to background charges [1].

SETs can take the electronics industry to the theoretical limit of electrons for computing applications. It allows representation of logic state by using single electron [2]. The SET can be used for the metrology and memory applications. It can be used as supersensitive electrometers and primary thermometers [2].

II. SINGLE ELECTRON TRANSISTOR(SET)

SET have been designed with small dimensions of few nanometers using semiconductors, metals and individual molecules. It made up of a tiny conducting island which is coupled with source and drain guided by tunnel junctions and coupled capacitively to gates.

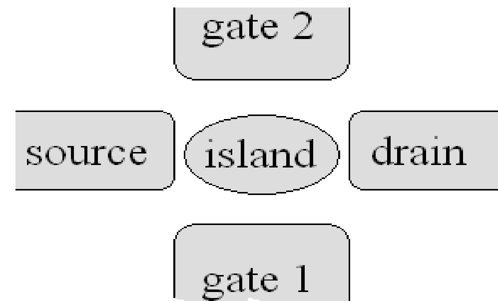

Fig.1: Geometry of SET [3].

a. SET Operation

The addition or withdrawal of only one electron can change the electrostatic or Coulomb energy in a mesoscopic system. A mesoscopic system is Quantum dot [QD] in which Coulomb energy is more than the thermal energy and can manage the transportation of electron inside and outside of the QD. This responsiveness to a single electron has open on to electronics which is based on individual electrons. As shown in figure 2.2 a nanoparticle of metal is placed between electrodes of metal. For separation of particle from electrodes insulation layer of oxide or vacuum can be used. This separation allows only tunneling of electron between them. The junctions between nanoparticles and electrodes can be modeled as a resistor and capacitor in parallel. The value of capacitance is dependent on particle size and value of resistance depends on tunneling of electrons. The capacitors and resistors are denoted by C_1, C_2, R_1 and R_2. The applied voltage between electrodes is denoted by V. Now it will be discussed that how the current, depends on applied voltage V.

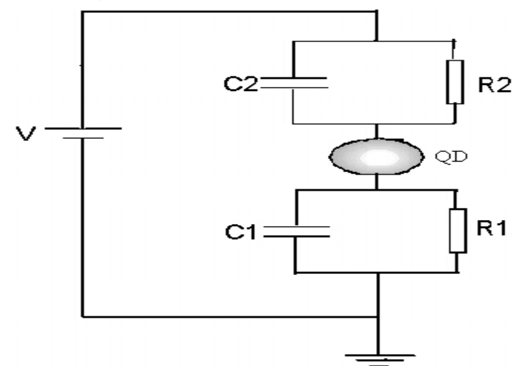

Fig.2: Quantum Dot structures [4].

When we increase applied voltage from zero, there is no current flow between two electrodes because for movement of

electron an amount of energy is required which is represented by equation 2.1.This quashing of flow of electron is represented as Coulomb blockade. The movement of electron will start between electrodes if applied voltage is enough to establish a voltage at the nanoparticles such as

$$e\varphi \geq E = \frac{e^2}{2C} \qquad (2.1)$$

This voltage is denoted by V_{th} and called as threshold voltage.

III. PHYSICAL MODEL USED FOR NUMERICAL SIMULATION

The physical models which are used in simulations are specified by models statements while the exception is impact ionization in which specification is done by IMPACT statements. The selection of models is based on the physical phenomenon occurs in the device for which models to be used. We can classify the models in five categories that are carrier statistics models, mobility models, recombination models, impact ionization models and tunnelling and carrier injection models.

IV. DEVICE STRUCTURE

The device is fabricated on p-type, separated by oxide layer called Silicon On insulator wafer of length 10nm.The structure of device is shown in figure 4.1.

The dimensions for substrate is 10×7 nm^2,for buried oxide 10×2 nm^2,for gate 2×1 nm^2,for wall spacers 2×4 nm^2,for source and drain are 4×1 nm^2 and a channel of 2×0.3 nm^2 is used. The device mesh structure and material used for different regions are shown in figure 4.2.

Substrate region and channel are doped with boron with concentration of 1×10^{15}cm^{-3} and 1×10^{17}cm^{-3}. The source and drain regions are doped with phosphorous with concentration of 1×10^{19}cm^{-3}.

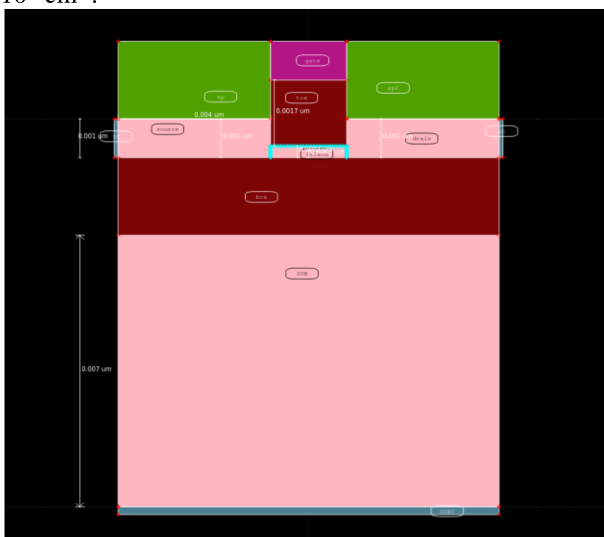

Fig.3: Cross Section View of designed single electron transistor

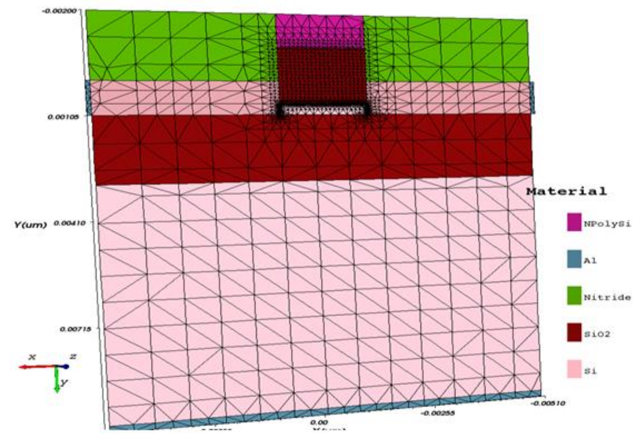

Fig.4: Device mesh structure

To improve the performance of designed device a Si quantum dot of size $.5 \times 1.6$nm^2 is used between gate and island. The structure of the device with Si dot is shown in figure 4.3.

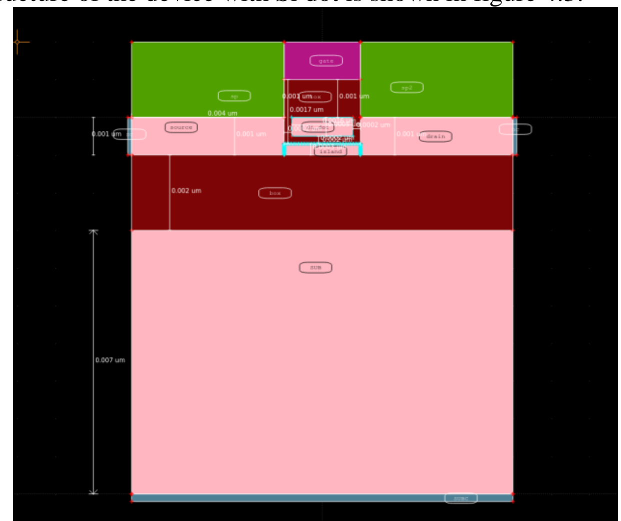

Fig.5: Device structure with Si dot

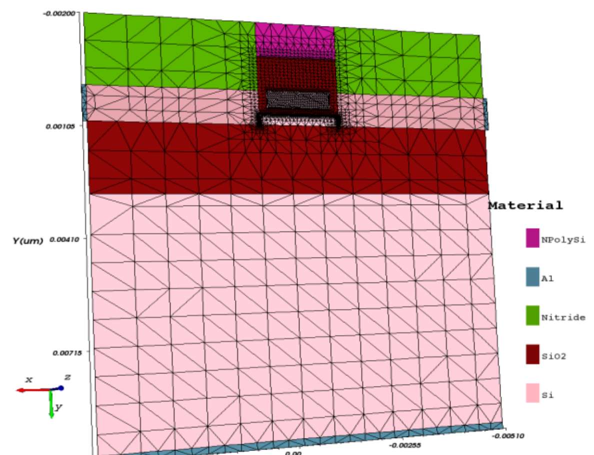

Fig.6: mesh structure with Si dot

V. RESULT & DISCUSSION

Device simulation is done using TCAD genius simulator. Figure 5.1 shows the comparison of I_D Vs V_G characteristics of both the devices. It is clear from the characteristics that the device with Si dot between gate and island exhibit better characteristic than the device without Si dot.

The device with Si dot has a small threshold voltage of .64V compare to .7V of device without Si dot. A high drain current is also observed in device with Si dot between gate and island.

Figure 5.2 shows the comparison of characteristics at logarithmic scale.

The minimum voltage requirement for tunnelling is Vth, called threshold voltage given by

$$Vth = e/C \quad (5.1)$$

So from equation 5.1 the value of capacitance C will be for device with Si dot. From the figure 5.1, Vth = .64V and value of e = 1.602×10^{-19} so,

$$C=1.602 \times 10^{-19}/.64=.250*10^{-18} \text{ F or } .250\text{aF} \quad (5.2)$$

The value of capacitance C_{wd} will be for device without Si dot. From the figure 5.1, Vth = .7V and value of e = 1.602×10^{-19} so, C_{wd} =.473aF (5.3)

Ec, charging energy for SET is given by,

$$Ec= e^2/2C \quad (5.4)$$

From equation 5.4 it is clear that the device having low value of capacitance will have high charging energy .So the device with Si dot will have high charging energy so it will behave better at room temperature.

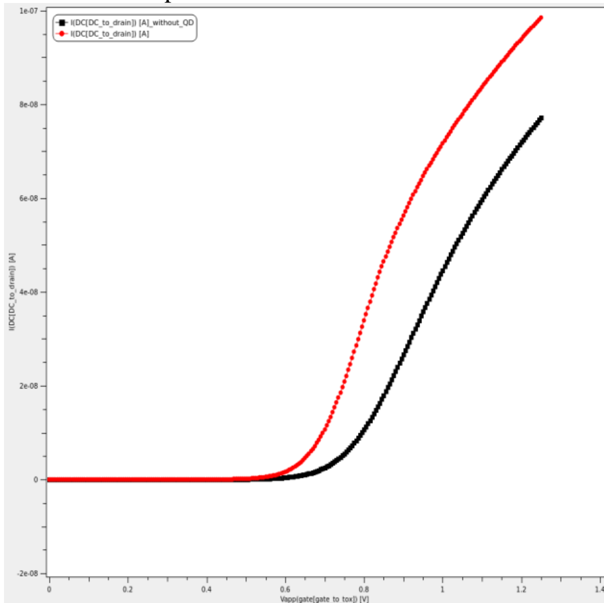

Fig.7: Comparison of I_D Vs V_G for device with and without Si dot

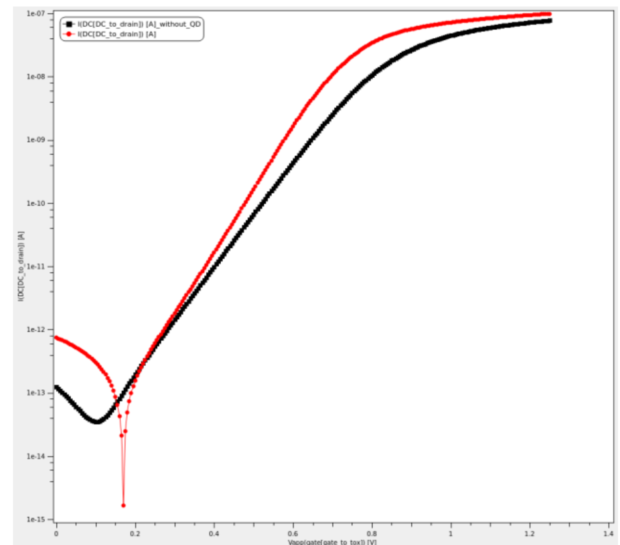

Fig.8: Comparison of I_D Vs V_G for device with and without Si dot at logarithmic scale

To study the charge transport in device designed with single electron transistor electric field and electron density are also plotted. Figure 5.3 shows the contour and cut line view of electric field inside the device. When no gate voltage is applied electric field is very small only inbuilt potential appear. Due to small electric field no electron will be attracted and no channel will be formed. When gate voltage of 1.2V is applied a sufficient electric field is generated and channel gets formed and conduction takes place.

The concentrations of electrons in various regions are shown in figure 5.4.The electron density plot shows that sufficient numbers of electrons are available to form the channel.

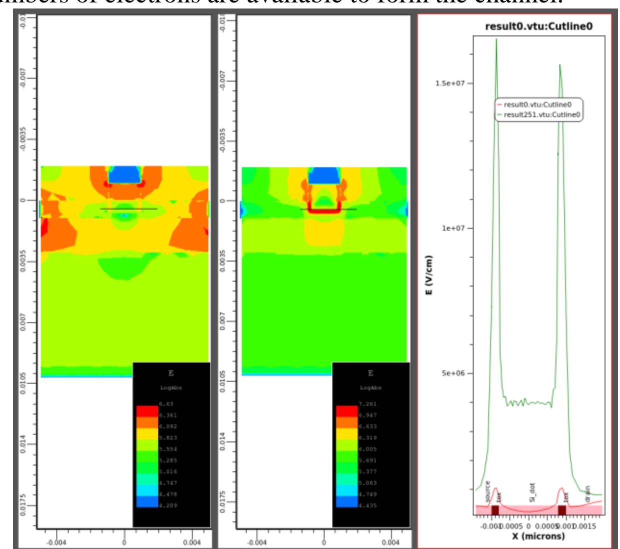

Fig.9: Electric field contour and cut line view

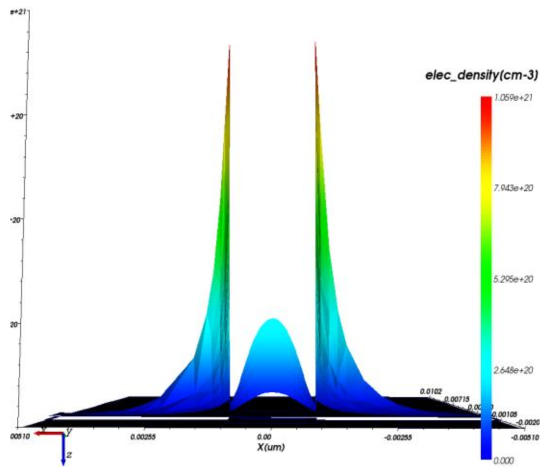

Fig.10: Electron density

As it is clear that device with Si dot having more charging energy than the device without dot at room temperature so it is more promising to work at room temperature operation. Figure 3.9 shows the comparison of I_D Vs V_G at different temperatures.

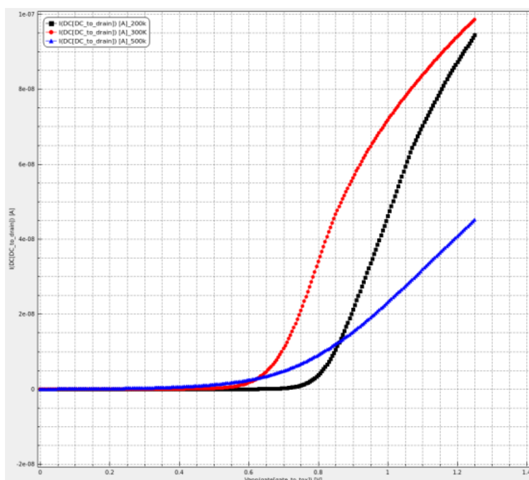

FIG.11: DRAIN CURRENT VERSUS GATE VOLTAGE CHARACTERISTICS FOR VARIOUS TEMPERATURES

VI. CONCLUSION

The single-electron transistor (SET) is most fundamental among single-electron devices. The two SET structures are simulated successfully using TCAD tools. From the simulation, when the length of channel is 2 nm, the threshold voltage for SET device with Si dot between gate and island is 0.64 V and for other is .7V. The SET devices are operated at room temperature (300K).The calculation shows that the charging energy, E_C of single electron transistor with Si dot found more than the device without quantum dot. The value of capacitance calculated is smaller for device without Si dot. So at room temperature the device having Si dot between gate and island is more promising.

VII. REFERENCES

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Author's Biographies

Tarun Singhal have done m.tech in ece.he is pursuing his phd from mdu, rohtak.his area of intrest is single electron devices.he has 12 international and 5 national publications.