Design and Synthesis of Combinational Circuits using Reversible Logic Gates

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***Abstract*—**Reversible logic gates has ability to reduce the power dissipation which is the main requirement in low power VLSI design. A circuit is said to be reversible, if number of inputs are equal to number of outputs and there is one to one mapping between the input and output vectors. Using outputs we can obtain full knowledge of inputs. This paper realizes the combinational circuits like comparator, full adder using reversible decoder. Reversible decoder is designed using reversible logic gates like Fredkin gate, Peres gate, TR gate and Feynman gate with minimum quantum cost.

Keywords*-Quantum Cost, Reversible Gates, Garbage Output.*

I. INTRODUCTION

Reversible logic is referred as a logic in which number of inputs and number of outputs are equal. In order to maintain reversibility, Garbage outputs are needed. Quantum cost, Garbage outputs, Number of gates are used to estimate performance of reversible circuits. Number of gates are the gates required to design the circuit.

i.Garbage outputs: Garbage outputs are extra outputs which maintain the reversibility. Every gate output is not used as input to other gates.

ii.Quantum Cost: The quantum cost of a reversible gate is the number of 1*1 and 2*2 reversible gates are used to design a circuit.

II. REVERSIBLE LOGIC GATES

The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

i.NOT GATE: The NOT GATE is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the Fig. 1. It is primitive gate to find quantum cost.

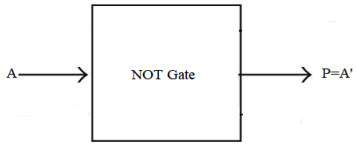

Fig. 1 NOT Gate

ii. FEYNMAN GATE (FG): Feynman gate is a 2×2 reversible gate as shown in Fig. 2. The Feynman gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate outputs. The Quantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.

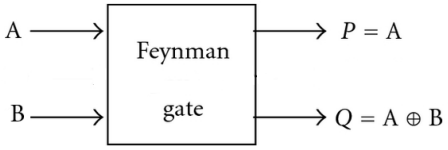

Fig. 2 Feynman Gate

iii.DOUBLE FEYNMAN GATE (DFG): Double Feynman Gate is a 3×3 reversible gate. The outputs are defined as shown in Fig. 3. The quantum cost of DFG is 2. This gate can also be used for duplicating outputs.

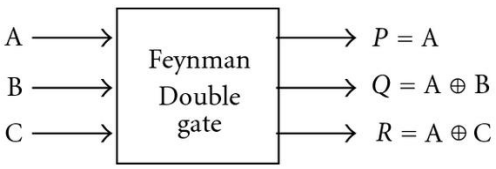

Fig. 3 Double Feynman Gate

iv.FREDKIN GATE (FDG): Fredkin Gate is a 3×3 reversible gate. The outputs are defined as shown in Fig. 4. The Quantum Cost of FDG is 5. This paper mainly surrounds around Fredkin gate.

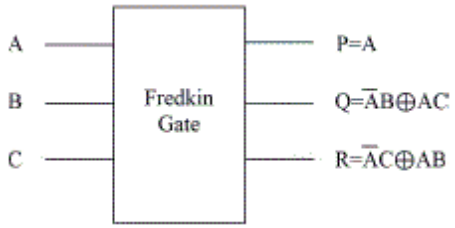

Fig. 4 Fredkin Gate

v.PERES GATE (PG): Peres Gate is a is a 3×3 reversible gate. The outputs are defined as shown in Fig. 5. The Quantum Cost of PG is 4.

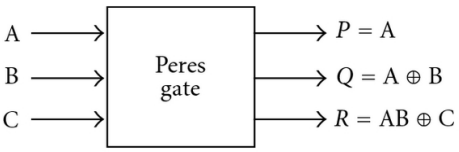

Fig. 5 Peres Gate

vi.TR GATE: TR Gate is a 3×3 reversible gate. The outputs are defined as shown in Fig. 6. The quantum cost of TRG gate is given by 4.

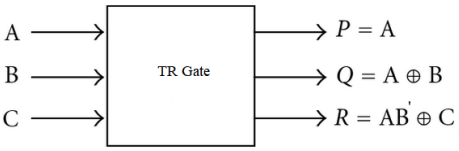

Fig. 6 TR Gate

III. BASIC GATES USING REVERSIBLE GATES

We can also design NOT gate, AND gate and OR gate using reversible gates. Here we used fredkin gate to design NOT, AND and OR gates as shown in Fig. 7. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing NOT, AND and OR gates.

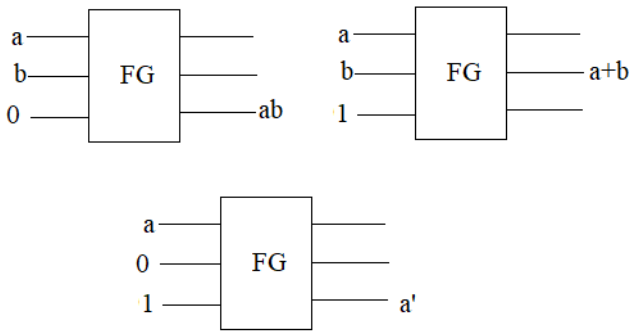

Fig. 7 AND, OR and NOT gates using Fredkin Gates

IV. EXISTING METHOD

The combinational circuits like binary comparator, full adder, full subtractor are designed using reversible decoder. A reversible decoder is designed using Fredkin gates. A 2*4 reversible decoder is designed using 3 Fredkin gates as shown in Fig. 8 and 3*8 reversible decoder is designed using one 2*4 decoder and 4 Fredkin gates i.e.,totally 7 Fredkin gates are used.Similarly a 4*16 decoder is designed using 3*8 decoder and 12 Fredkin gates.The quantum cost of 2*4 reversible decoder is 15 because quantum cost of Fredkin gate is 5 and we are using 3 Fredkin gates. The number of gates required to design 4*16 reversible decoder is 15 Fredkin gates. Therefore the quantum cost of 4*16 decoder is 75. In order to reduce the quantum cost, Fredkin gates are replaced by Peres gate, TR gate, Not gate, and CNOT gate.

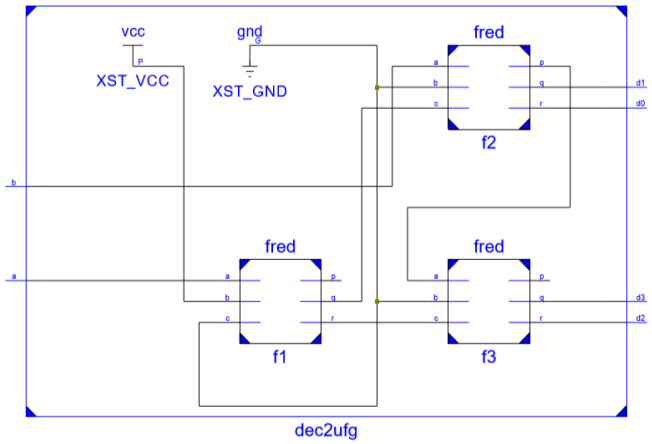

Fig. 8 circuit diagram of 2*4 Reversible decoder using Fredkin gates

V. PROPOSED METHOD

In proposed method, Fredkin gates for designing 2×4 decoder are replaced with reversible gates like Peres gate, TR gate, NOT gate and CNOT gate as shown in Fig. 9.

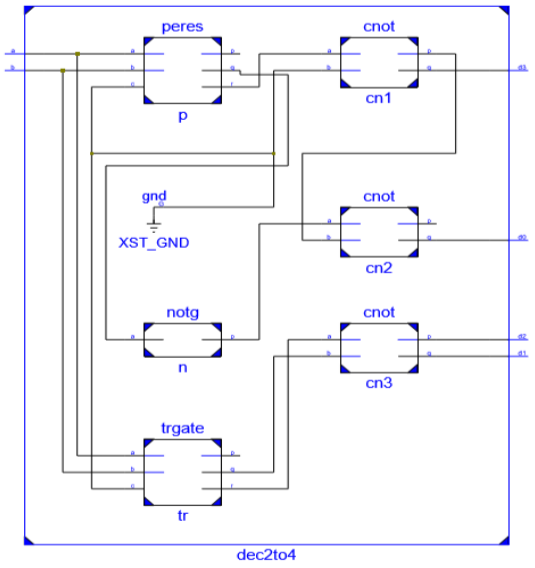

Fig. 9 Circuit diagram of 2*4 reversible decoder

The whole design is done using Fredkin, NOT gate, CNOT, Peres gate which reduces the quantum cost when compared to the existing method. The quantum cost of 2*4 decoder is 11.

VI. SIMULATION RESULTS OF PROPOSED CIRCUITS

a. 4*16 Reversible decoder

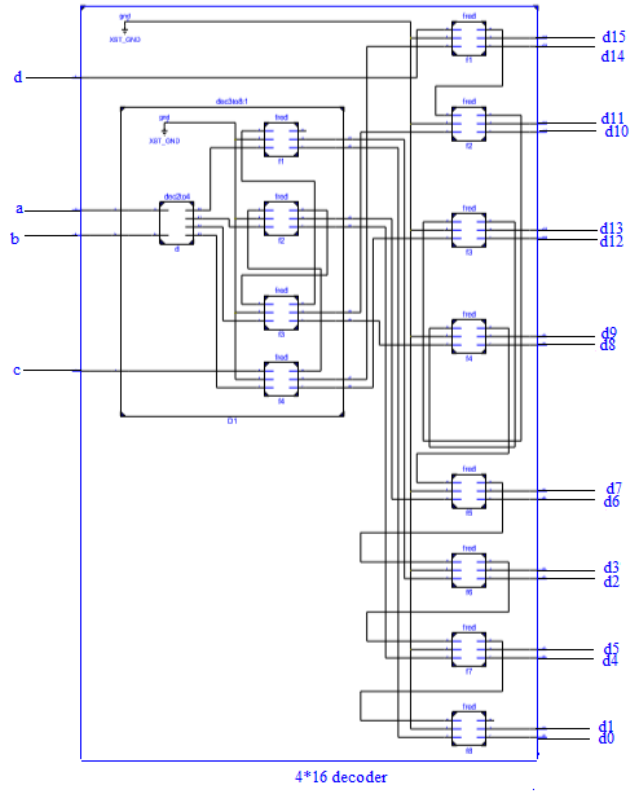

Fig. 10 RTL schematic of 4*16 reversible decoder

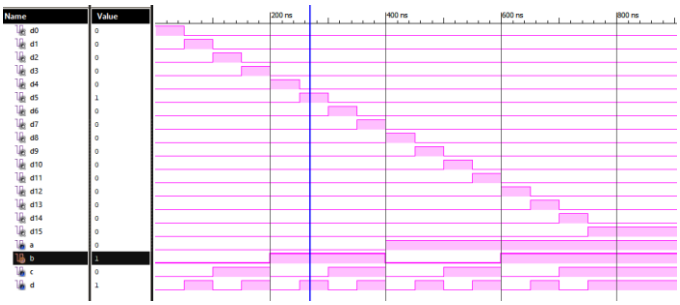

Fig. 11 Simulated output of 4*16 decoder

b. Binary Comparator:

Binary Comparator requires one 2*4 decoder and one OR gate as shown in Fig. 12. The output lines g, l, e represents greater, lesser and equal. The inputs are a, b. If a<b then l becomes high. If a>b then g becomes high. If a=b then e becomes high.

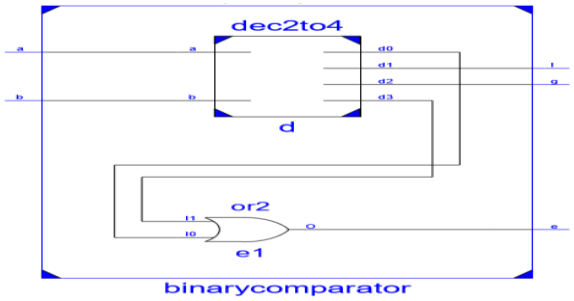

Fig. 12 RTL schematic of binary comparator

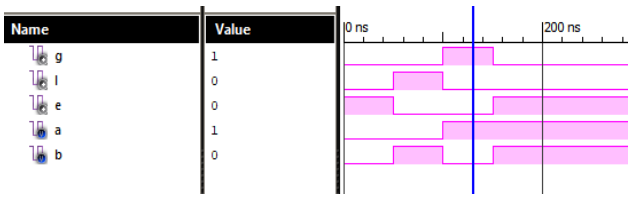

Fig. 13 Simulated output of binary comparator

c. Full Adder:

Full adder requires one 3*8 decoder and two four input OR gate as shown in Fig. 14.The min terms for sum and carry are derived from outputs of decoder.

Equation for sum S= ∑(1, 2, 4, 7)

Equation for carry C=□∑(3, 5, 6, 7)

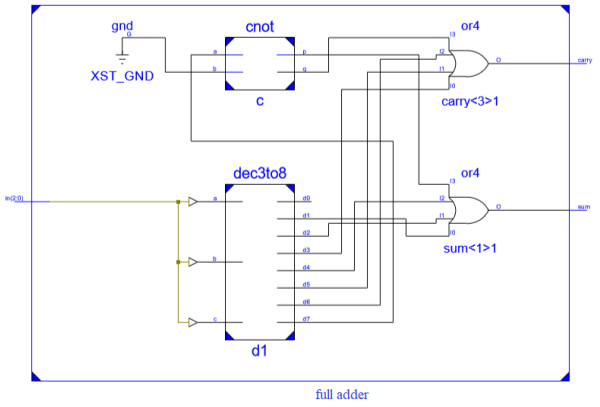

Fig. 14 RTL schematic of full adder

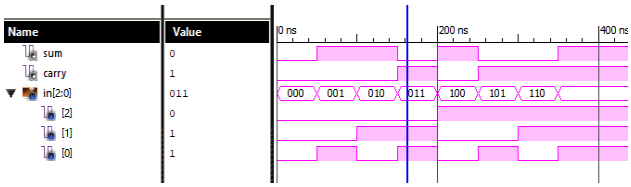

Fig. 15 Simulated output of full adder

d. Comparative Study:

CIRCUIT	QUANTUM COST	GARBAGE OUTPUTS
2*4 decoder	11	3
3*8decoder	31	4
4*16 decoder	71	5

e. Power calculations :

CIRCUIT	CONVENTIONAL (mw)	REVERSIBLE (mw)
2*4 decoder	1.28	1.21
Binary Comparator	1.17	0.90
Full Adder	1.27	1.18

The main advantage of using reversible logic gates is power dissipation. When compared to the conventional circuits, power dissipation is reduced by using reversible logic.

VII. CONCLUSION

The combinational circuits (decoder, binary comparator and full adder) are designed using reversible decoder. The proposed reversible decoder is designed with minimum quantum cost and garbage outputs. These combinational circuits are synthesized using Isim tools and power dissipation is calculated. The power calculations are compared with conventional circuits which concludes that power dissipation is reduced which is a major advantage of the reversible logic gates.

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