72-Mbit (2M x 36) SYNC SRAM

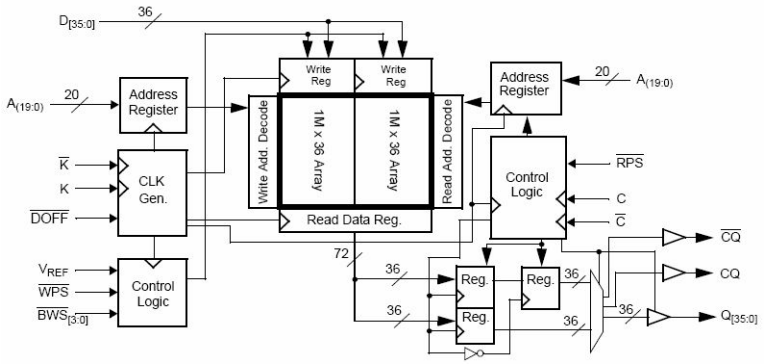
Part Number: DPA71514AV1802A

\ The DPA71514AV1802A is a 1.8V Synchronous Pipelined SRAM equipped with QDR™-II architecture. QDR-II architecture consists of two separate ports: the read port and the write port to access the memory array. The read port has dedicated Data Outputs to support read operations and the write port has dedicated Data Inputs to support write operations. QDR-II architecture has separate data inputs and data outputs to completely eliminate the need to "turn-around" the data bus required with common IO devices. Access to each port is accomplished through the common address bus. The read address is latched on the rising edge of the K clock and the write address is latched on the rising edge of the $\overline{K}$ clock**.** Accesses to the QDR-II read and write ports are completely independent of one another. To maximums data throughput, both read and write ports are equipped with Double Data Rate (DDR) interfaces. Each address location is associated with two 36-bit words that burst sequentially into or out of the device. Since data is transferred into and out of the device on every rising edge of both input clocks (K and $\overline{K}$ and C and $\overline{C}$), memory bandwidth is maximized while simplifying system design by eliminating bus "turn-arounds."

Depth Expansion is accomplished with port selects which enables each port to operate independently.

All synchronous inputs pass through input registers controlled by the K and $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ (or K and $\overline{K}$ in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write

Logic Block Diagram



- **-55˚ to +125˚C operating temperature**
- **Hermetically sealed ceramic package**
- **Separate Independent read and write data ports**
  - **Supports concurrent transactions**
- **250 MHz clock for high bandwidth**
- **2-Word Burst on all accesses**
- **Double Data Rate (DDR) interfaces on both read and write ports (data transferred at 500 MHz) @ 250 MHz**
- **Two input clocks (K and $\overline{K}$) for precise DDR timing**
  - **SRAM uses rising edges only**
- **Two input clocks for output data (C and $\overline{C}$) to minimize clock skew and flight time mismatches**
- **Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems**
- **Single multiplexed address input bus latches address inputs for both read and write ports**
- **Separate port selects for depth expansion**
- **Synchronous internally self-timed writes**
- **QDR™-II operates with 1.5 cycle read latency when Delay Lock Loop (DLL) is enabled**
- **Operates as a QDR-I device with 1 cycle read latency in DLL off mode**
- **Full data coherency, providing most current data**
- **Core V_{DD}= 1.8 (±0.1V0); I/O V_{DDQ}=1.4V to V_{DD}**
- **Variable drive HSTL output buffers**
- **JTAG 1149.1 compatible test access port**
- **Delay Lock Loop (DLL) for accurate data placement**
- **This product uses Cypress CY7C1514AV18 die and is tested to meet military and space operational environment requirements.**