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Research Article

Design and Simulation of FIR Filter using Multiple Constant Multiplication

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Abstract

Finite impulse response (FIR) digital filters have potential for high-speed and low-power realization through parallel processing. In this paper, we suggest an efficient implementation of FIR filters using Pipelined Multiple Constant Multiplication (PMCM) technique. MCM methods are widely used for reducing computational complexity of FIR filters. The concept of pipelining has been incorporated that results in reducing the delay of the FIR filter, thereby enhancing the speed and reducing the power dissipation as compared to the non-pipelined techniques. The speed of the multipliers can be increased by reducing the number of partial products. Parallel multipliers are fastest among all multipliers. Booth multiplier is one of the parallel multiplier that operate on signed operands in two's complement form and have high performance, low power consumption Experimentation on block filters for 16 bits of different block lengths indicates that, compared to sample-by-sample MCM based FIR Filters. The simulation of this design is done by using Modelsim 6.2c. The design synthesis and power analysis are carried out using Xilinx ISE 12.1v.

Keywords: Finite impulse response; Multiple Constant Multiplication; Booth's Muliplier; Filters.

Introduction

Filters are used in wide range of applications such as multimedia and DSP (Digital Signal Processing) etc. Most of DSP computations involve the use of multiply accumulate operations and therefore the design of fast and efficient multiplier and adder units are important [1]. More ever, the demand for portable applications of DSP architectures has dictated the need for low power designs. Digital Finite Impulse Response filter (FIR) has performs lot of arithmetic and logical operations. In general, arithmetic and logic operation modules such as adder and multiplier modules, consume more chip area and delay for each operation is more. The resource utilization and power of digital FIR filter circuit is reduced by optimization of taps and bit width of input signal and filters coefficients. The adders and multipliers are applied for filters to eliminate power consumption due to unwanted data transitions. A multipliers technique is presented based upon add and shift operation and multiple constant multiplication technique for low area and high speed implementation of FIR filters [2].

A multiplication dominates the complexity of many digital signal processing systems. On the other hand, digit-serial architectures offer alternative low-complexity designs since digit-serial operators occupy less area and are independent of the data word length [3]. Also, it is mentioned that the full flexibility of a multiplier is not necessary for the constant multiplications, since filter coefficients are fixed and determined beforehand by the DSP algorithms. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift adds architecture [4]. One of the important implementation of the Multiplication of a variable with a set of constants also known as the MCM operation, is a central operation and achieves performance bottleneck in many DSP applications such as, error correcting codes, linear DSP transforms, and Finite Impulse Response filters.

Research methodology

Multiple Constant Multiplication

Multiple constant multiplication (MCM) has been shown to be an efficient way to reduce the number of additions and subtractions in FIR filter implementations [5]. However, for

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polyphase decomposed FIR filters and filter banks, the problem can be formulated in three different ways. Either as one MCM block with all coefficients, one MCM block for each subfilter, or as a matrix MCM block in figure 1. In this work we compare the approaches in terms of complexity, both for the MCM blocks and for the remaining hardware, such as structural additions and delay elements.

The multiple constant multiplication (MCM) problem, i.e., multiplying one data with several coefficients has received consideration over the years. By expressing the multiplication using shifts, additions, and subtractions a realization without general multipliers is obtained. The number of additions and subtractions can then be significantly reduced by using common partial results. As additions and subtractions have similar complexity we will from now on only refer to them as additions [6]. The development of efficient algorithms has to a high extent been motivated by the use of MCM blocks in FIR filters. For direct transposed form FIR filters the input is multiplied with the filter coefficients where the MCM block is marked with a dashed box in figure 2. Using transposition, a direct form FIR filter is obtained where the sum-of-product computation is marked with a dashed box. Hence, MCM is also efficient for sum-of-product computations. We will from now on refer to MCM block for both multiple constant multiplication and for the sum-of-products computation [7]. Sometimes the term multiplier block is used for MCM block. But as that may indicate the algorithm used, we use the more general term MCM block.

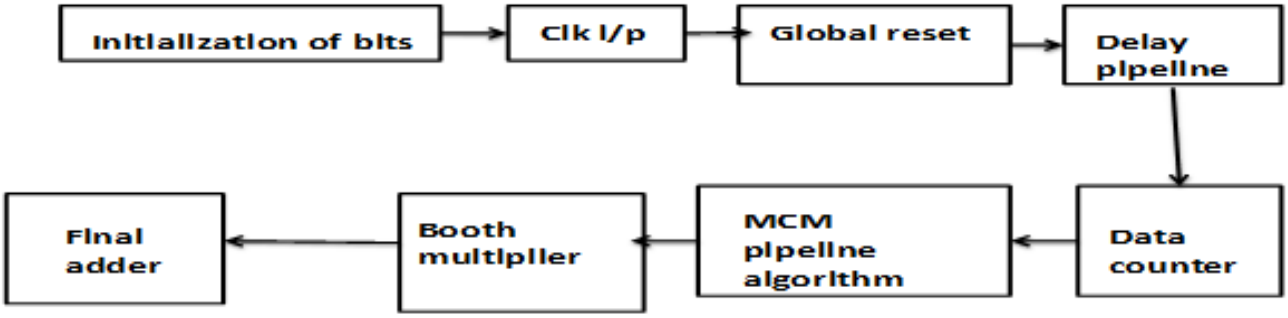

Figure 1. Block diagram of proposed system

However, in some applications, more than one FIR filter is operating on the same data stream. This is the case for, e.g., FIR filters and filter banks using poly phase representation. In figure 2 shown that by using transposed form FIR filters only one MCM block. However, this leads to that more delay elements and structural additions are required as shown in figure 3, as each filter has its own delay line. For direct form FIR filters, one must apply MCM to each subfilter. With the recent advances of algorithms for matrix MCM this gives us a third alternative.

Complexity

The complexity of the resulting realization will be dependent of three factors. First, the size numbers, and type of MCM blocks. Second, the number of delay elements and finally the number of structural additions, i.e., the additions that are not part of the MCM block (additions outside of the dashed box. Here, we focus the discussion on polyphase decomposed interpolation and decimation filters, but identical results can be derived for the filter bank case [8]. We assume that the filter order of the total filter is N and that the number of sub filters are M. Hence, each sub filter has a filter order (N + 1)/M – 1).

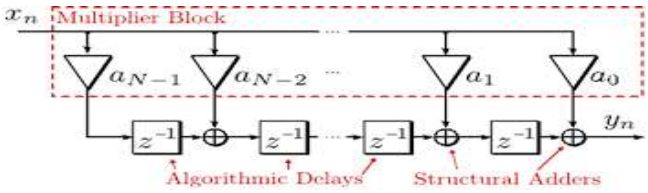

Figure 2. Structure of a fir filter in transposed form

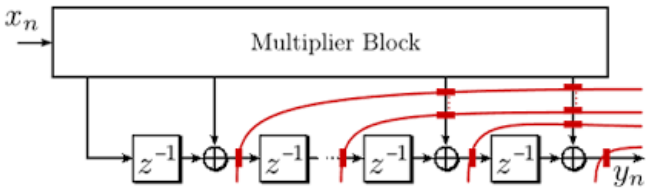

Figure 3. Pipelining the structural adders

Mixed integer linear programming (MILP) is a powerful representation often used to formulate decision-making problems under

uncertainty. However, it lacks a natural mechanism to reason about objects, classes of objects, and relations. First-order logic, on the other hand, excels at reasoning about classes of objects, but lacks a rich representation of uncertainty [9].

While representing propositional logic in MILP has been extensively explored, no theory exists yet for fully combining First Order Logic with MILP. We propose a new representation, called first-order programming, which subsumes both First Order Logic and MILP. We establish formal methods for reasoning about first order programs, including a sound and complete lifted inference procedure for integer first order programs. Since First Order Programming can offer exponential savings in representation and proof size compared to First Order Logics, and since representations and proofs are never significantly longer in First Order Programming than in First Order Logic, we anticipate that inference in First Order Programming will be more tractable than inference in First Order Logic for corresponding problems.

Booth Multiplier

Booth's algorithm can be implemented by repeatedly adding (with ordinary unsigned binary addition) one of two predetermined values A and S to a product P, then performing a rightward arithmetic shift on P [10]. Let m and r be the multiplicand and multiplier, respectively; and let x and y represent the number of bits in m and r.

A: Fill the most significant (leftmost) bits with the value of m. Fill the remaining (y + 1) bits with zeros. S: Fill the most significant bits with the value of (−m) in two's complement notation. Fill the remaining (y + 1) bits with zeros.

P: Fill the most significant x bits with zeros. To the right of this, append the value of r. Fill the least significant (rightmost) bit with a zero.

Results and discussions

Figure 4 shows the internal wave form structure of the given input that is the reprsentation of the input in the form of the 16 bit structure it mainly describes the internal structure of the given input frequency module.

The above figure 5 represents band filter which represents in the analog form whereas in the previous diagram represents in the digital here it represents in the analog form other than that it has the pass bands and attenuation band life structure and figure 6 shows the corresponding digital representation of analog form.

The figure 7 shows the RTL logical structure of the given input form as it mentions the data flow line of the given filter input form.

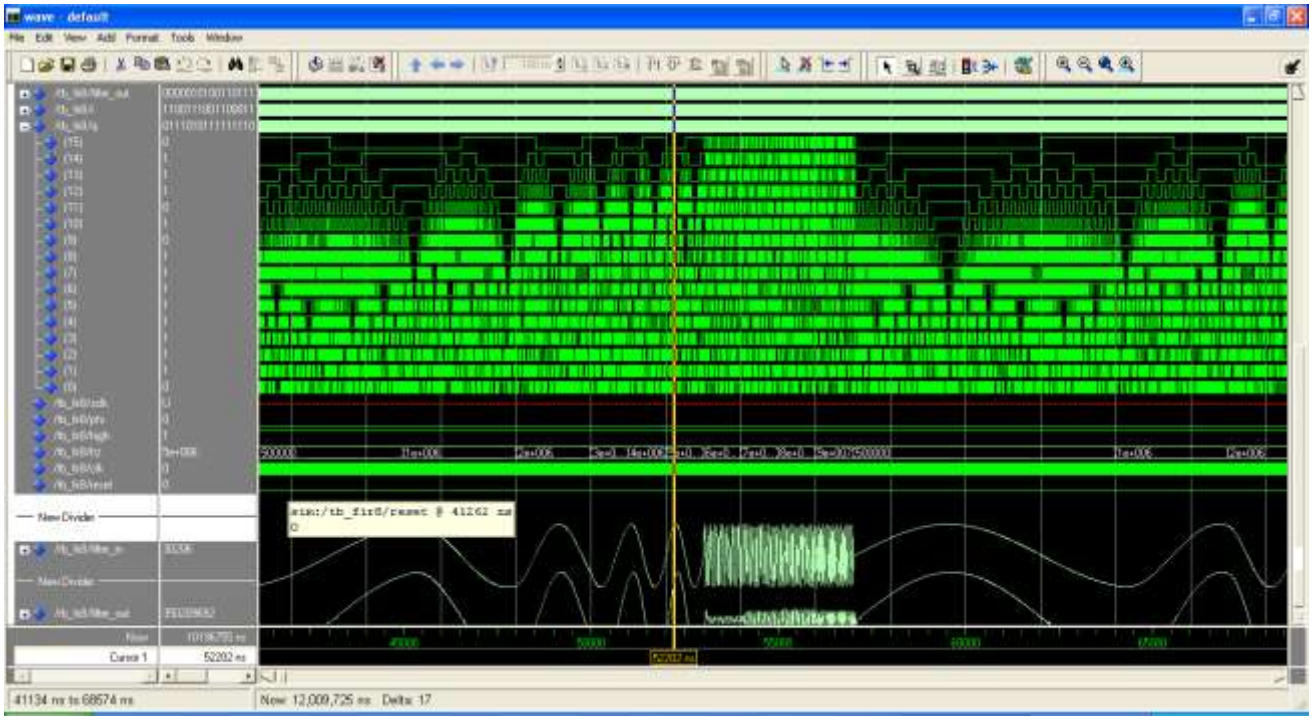

Figure 4. Internal waveform structure

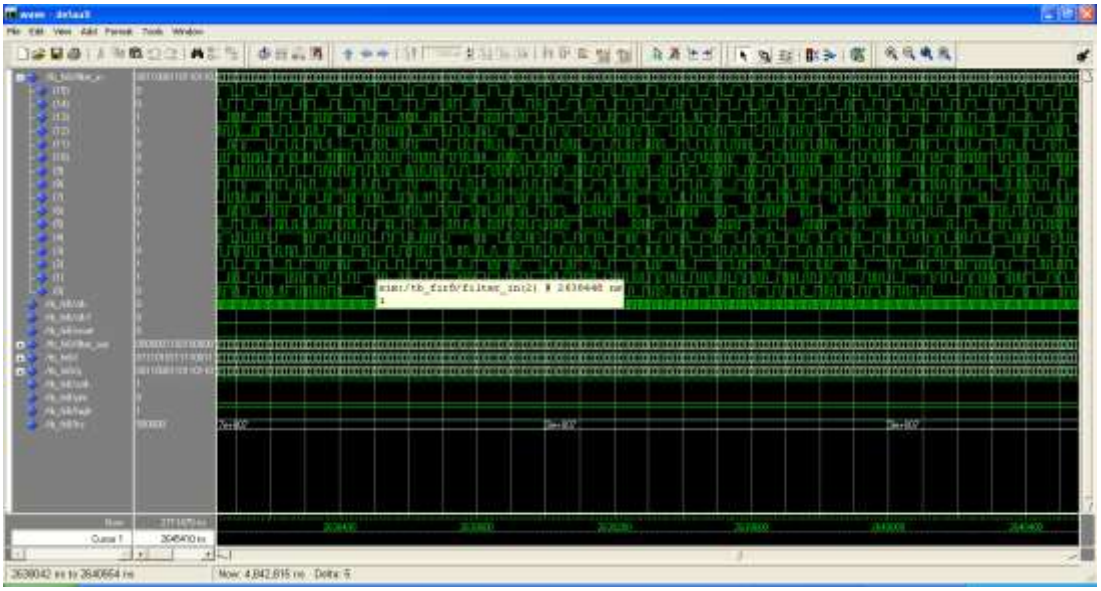

Figure 5. Analog form of filter

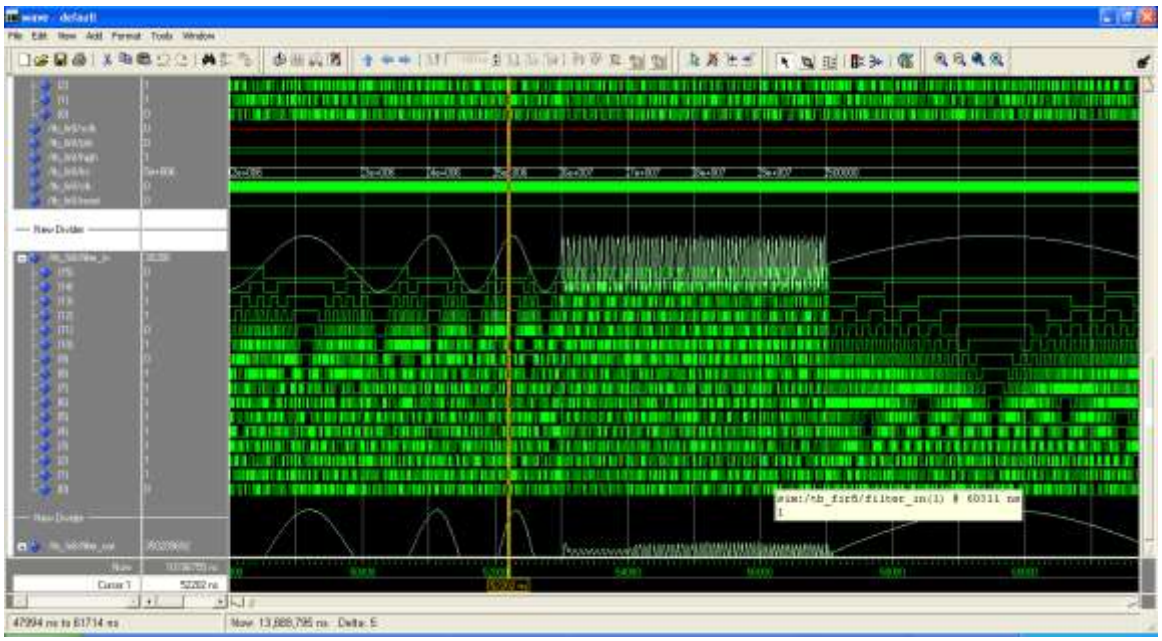

Figure 6. Digital representation

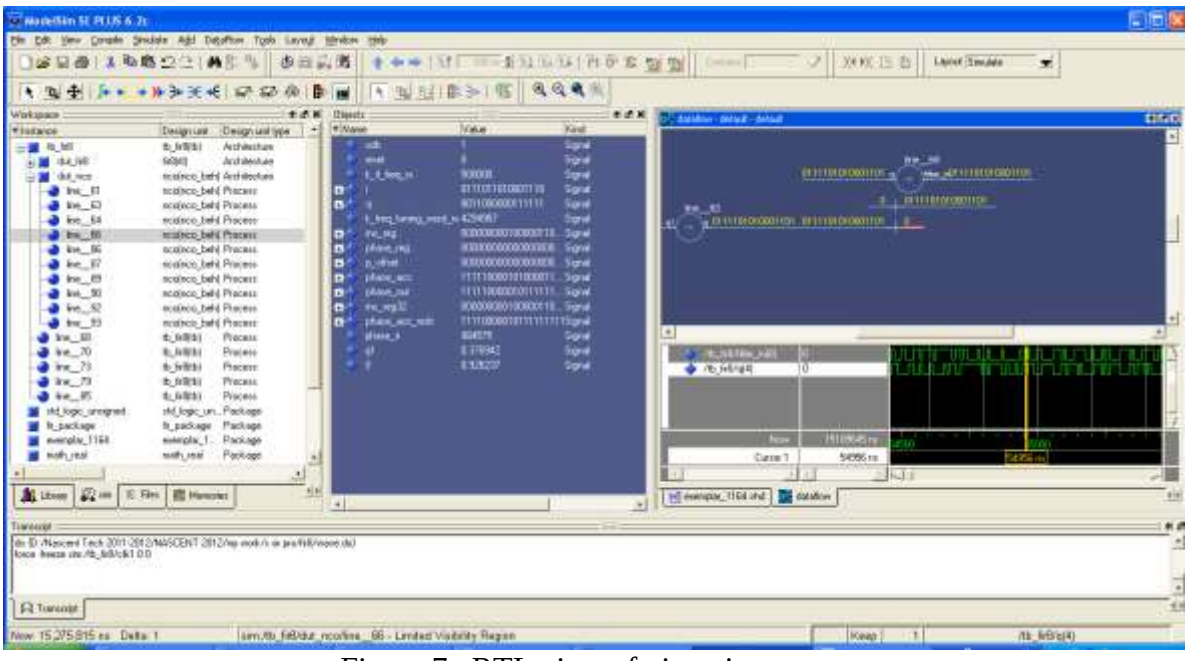

Figure 7. RTL view of given input

Conclusions

The FIR Filter based on Pipelined MCM operation is designed and total power consumption is reduced. The Booth multiplier with Pipelined MCM operation will significantly reduce the computational complexity of digital FIR filter and may reduce the noise signal. The proposed filter is used by Booth multiplier for their multiplication. In future, various high speed parallel multipliers can be implemented by using FPGA. The simulation of this proposed design was performed by Modelsim 6.2c. The design synthesis and the power result were done by Xilinx 12.1v.

Conflict of interest

Authors declare there are no conflicts of interest.

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