Performance analysis of a 127-micron pixel large-area TFT/photodiode array with boosted fill factor

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ABSTRACT

Sensor fill factor is one of the key pixel design requirements for high performance imaging arrays. In our conventional imaging pixel architecture with a TFT and a photodiode deposited in the same plane, the maximum area that the photodiode can occupy is limited by the size of the TFT and the surrounding metal lines. A full fill factor array design was previously proposed using a continuous sensor layer[1]. Despite the benefits of 100% fill factor, when applied to large-area applications, this array design suffers from high parasitic line capacitances and, thus, high line noise. We have designed and fabricated an alternative pixel structure in which the photodiode is deposited and patterned over the TFT, but does not overlap with the lines underneath. Separating the diode from the TFT plane allows extra space for an additional TFT which can be used for pixel reset and clipping excessive charge in the photodiode developed under high illumination. This reduces memory effect by 250%. The yield and the reliability are expected to improve as well since the TFTs and lines are buried underneath the diode. With the increased fill factor, we collect 50% more electrons per pixel, thereby improving the signal to noise ratio. The maximum signal to noise ratio is achieved when the increased signal and the undesirable parasitic capacitance on the data line are best optimized. Linearity, sensitivity, leakage, and MTF characteristics of a prototype X-ray imager based on this architecture are presented.

Keywords: X-ray detector, image sensor, a-Si, TFT, *nip* photodiode, fill factor, clamping circuit, large-area array

1. INTRODUCTION

Large-area arrays incorporating amorphous Silicon (a-Si) thin-film transistors (TFTs) and *nip* photodiodes have now become well-established in the field of medical imaging.[1-10] This technology, based on the similar manufacturing processes developed for active matrix TFT panels used to make liquid crystal displays, takes advantage of the ability to coat glass substrates with a-Si over large areas. This material is also well known for its excellent photoconductive properties, which is utilized in image sensors to form *nip* photodiodes[3] or *mis* devices.[9] *nip* photodiodes are particularly useful because under reverse bias, they operate with submicrosecond response times and thus are well-suited to dynamic applications. The low dark currents of a-Si *nip* photodiodes make it possible to operate sensors at very low exposure levels without substantial cooling. These devices have near unity quantum efficiency in the visible spectrum. Coupled with high efficiency CsI:Tl or other scintillators, a-Si sensor arrays have proven very effective as X-ray image sensors. Through appropriate optimization of the optical stack, their quantum efficiency can be tuned to match the output spectrum of the scintillator to provide maximum x-ray sensitivity.

Recent medical imaging applications of a-Si image sensor arrays include radiography, mammography, oncology, cardiology, and fluoroscopy. This range of applications requires image sensors with high sensitivity, large dynamic range, low noise, and high frame rate capability. The same sensor is often used in various modes of operation, where it needs to switch from high dose radiographs or diagnostic image sequences to low dose fluoroscopic sequences. Under high exposure conditions, image quality is paramount. For example, image cross-talk along each data line is controlled by the degree to which the TFT switches can hold their charges on each pixel prior to readout. This requirement is well satisfied by the low off-currents of a-Si TFTs. Another imaging concern is memory effect due to charge trapping in the *nip* photodiodes after each high dose image. This has largely been resolved through software adaptation[4] or back light compensation.[7]

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The fluoroscopic application[6,7] is extremely demanding, as it requires the viewing of very low dose, dynamic images where signal levels and electronic noise limit the contrast of images at dose levels below ~1 μR/frame. Electronic noise generated from the array is dominated by switching noise from the photodiode capacitance (√kTC noise), noise from charge trapped in the TFT switch, and parasitic noise generated from high data line capacitance. In order to minimize these noise effects, the diodes are made relatively thick (~1.5 μm) to reduce their capacitance and the sizes of the TFT switches used to connect them to each data line. However, thickening the diodes increases their propensity to trap charge after light exposure and thus enhances image lag. To minimize this effect, large reverse bias voltages, as much as -10 V, are applied to limit image lag, particularly under saturated exposure conditions. This voltage is more negative than the typical gate off-voltages detector designers would like to apply to the TFTs, leading to increased cross-talk at high exposure when the TFTs begin to leak photocharge onto the data lines. One of the purposes of this paper is to demonstrate the interplay between memory effect and cross-talk as a function of light exposure and reverse bias in standard image sensors through an imaging experiment, and the role an additional clamping TFT would play to minimize these effects.

Another way to improve performance of image sensors under low dose conditions is to boost pixel fill-factor. Conventional image sensors utilize a manufacturing process in which the photodiode is embedded in the same plane as the TFT and the gate and data lines. This limits the fill-factor to approximately 57% for currently produced 127 μm x 127 μm pixel arrays. Previous high fill-factor designs utilized a continuous photodiode layer deposited over the TFT matrix which offers effectively 100% fill-factor. This approach, however, suffers from higher line capacitances due to the overlap of the photodiode layer over the gate and data lines, and image blooming effects due to the nonisolated structure of the pixels. In this paper, we investigate pixel designs which utilize fully isolated photodiodes built on top of the TFT matrix, with pixel fill-factors of between 80 and 87% while minimizing excessive gate and data line capacitances. This approach allows for new circuitry to be placed next to the TFT switch, such as an additional clamping TFT, TFT amplifiers, or dose sensing circuitry. Recent results with arrays made under these conditions are reported in this paper.

2. PROCESS ARCHITECTURE

In the baseline (BL) sensor array architecture, the *nip* photodiode is built on top of a chromium layer which serves both as the bottom (floating node) electrode of the photodiode and the source-drain (SD) metal for the TFT. A separate 1 μm thick aluminum layer separated by an interlayer dielectric (ILD) is used to form bias and data lines. Because of the dual role played by the chromium layer, the photodiode competes directly with the TFT for space within the pixel. As pixel size decreases below 100 μm, the decrease in fill factor is so severe that a new pixel architecture is warranted.

Full fill factor array (FF) architecture using a continuous *nip* sensor layer has previously been proposed[11] to address fill factor at high resolution. However, we have found that this array architecture has a number of manufacturability drawbacks. With a continuous, intrinsic a-Si layer, control of crosstalk between adjacent pixels is key to good array performance. To provide pixel isolation, the bottom *n*+ a-Si layer must be separately deposited and patterned to eliminate lateral conduction between pixels. Also, the bottom metal contacts should be fully covered by the *n*+ layer in order to suppress hole injection from the back metal, which requires an additional masking step. Moreover, the intrinsic and *p*+ a-Si layers need to be deposited in a separate PECVD deposition cycle to form the *nip* diode. In production, one must ensure a consistent *n*+ surface, free of any organic residues and native oxide, if good, uniform sensor performance is to be maintained. By contrast, when the *nip* layers are deposited successively within the same pumpdown, consistent sensor performance is readily assured.

In the new MaxFill™ sensor array (MF) architecture, we have retained the segmented photodiodes of the baseline architecture, building the *nip* devices on top of the TFT switching matrix. By moving the *nip* sensor out of the plane of the TFTs, the fill factor can be greatly increased. For example, the fill factor of the 127μm pixel used in this study was increased from 57% with the BL architecture to 85% with the MF architecture (see Figure 1). In the new architecture, the TFT SD metal and data lines share a single mask. For the new architecture to succeed, the TFT channel length must

not increase from the current architecture, if the TFT contribution to the pixel capacitance and noise is to be maintained. To enable this, we have developed an anisotropic dry etch process for the data line and TFT SD patterning process.

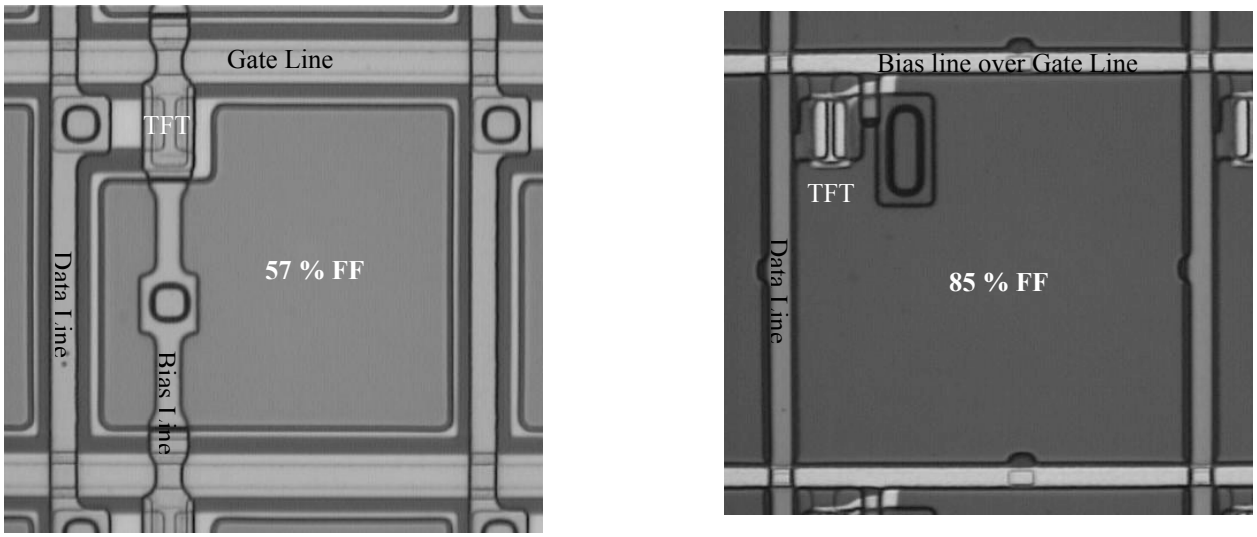


Figure 1. Comparison between 57% FF baseline and 85% FF MaxFill™ 127 µm pixel designs.

In consolidating the SD and data metals, we have found that it is possible to pattern the *nip* diodes and the back contact metal in one masking sequence without degrading leakage. In BL arrays, the Cr back contact metal is patterned separately from the *nip* sensor. The sensor is recessed from the Cr edges to protect the sensor sidewalls from chemical attack and contamination during the TFT SD formation. Eliminating this Cr "skirt" improves the fill factor by 7%.

The MF architecture is accomplished with seven photomasks, in contrast to eight photomasks for the baseline architecture. We have taken advantage of earlier work done at Xerox on a five mask process for AMLCD flat panel display architecture.[12] This architecture uses a single level gate structure to eliminate separate masking of a cladding layer used for hillock control. There is an overcoating to passivate the bias layer and protect against mechanical abrasion. We have not included this in the mask count, as shadow masking is used, and precise alignment by photomasking is not required.

Because the bias metal runs over the *nip* diodes, it can reduce the optical fill factor. Three different approaches are shown in Figure 2 representing different tradeoffs between optical fill factor, bias resistance, and coupling capacitance.

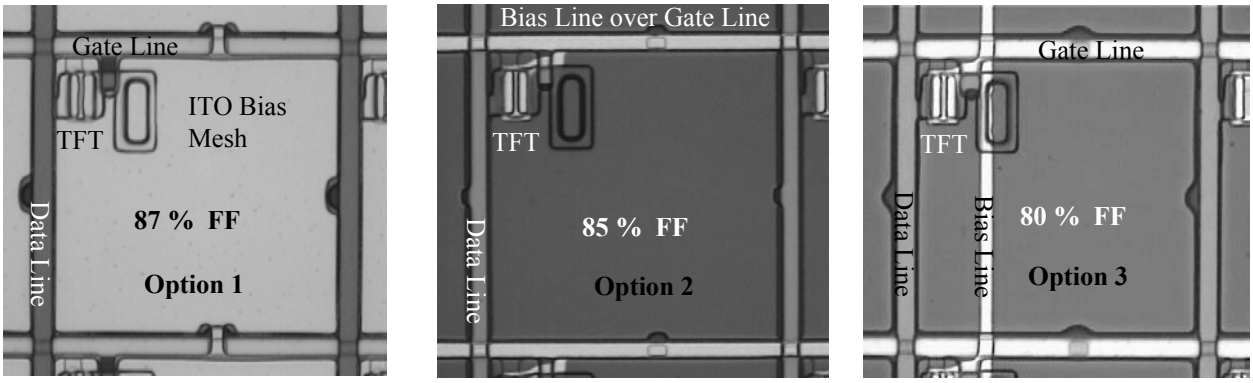


Figure 2. Different connection schemes for connecting bias to each photodiode: Option 1: ITO bias mesh; Option 2: bias line running over gate line; and Option 3: bias line running parallel to data line.

Option 1 uses a second layer of indium tin oxide (ITO) to provide bias to the array. Because of its high transparency, ITO is an ideal candidate for the bias metal. However, due to its relatively high sheet resistance, a continuous or mesh design is essential to keep bias voltage variation across the array at a minimum. Data line coupling and optical losses must be carefully optimized. Because of these reasons, we have chosen not to implement this option in the first arrays, as it is not viewed as critical to demonstrate the main advantage of the MF architecture. Option 2, which is what we used in this study, runs the Bias over the gate lines (B/G). Aluminum bias lines run over the gate lines to minimize capacitive coupling to the data lines. In this design, the bias to gate coupling is increased, but modeling shows that the RC time constant of the gate line can be kept below 1μs. In this design, shadowing is limited to the bias tap to the individual pixel. There is a 1.7% reduction in the optical fill factor in the current design, because we have chosen to have the bias contact serve cover the TFT as a secondary light shield for a separate investigation involving thin *nip* sensors. In an optimized design, a reduction in optical fill factor of less than 1% is achievable. Option 3 runs the bias lines parallel to the data lines (B‖D). This option produces the least data line coupling, but reduces the fill factor by about 5% reduction. It has the advantage that it provides a direct one-to-one comparison of the array performance between the MF and BL architectures. In all three designs, added redundancy is provided by turning the bias line into a two dimensional mesh by crosslinking between the long bias lines. The crosslinks are in a stair-step pattern running diagonally across the array repeating every 16 pixels to reduce the effective bias line resistance at the center of the array below 100 Ohms. Placing the bias on top, a feature of all three designs, eliminates data-to-bias shorts, which are common defects in the BL architecture.

In the FF architecture, the ITO layer on the continuous sensor provides the sensor bias. By segmenting the sensors, a separate bias metal layer must be added for the sensor bias. This increase in mask count is offset by the improvement in manufacturability, as it allows provisions to be made for repair. In the FF architecture, the continuous sensor layer covers and obscures the underlying switching matrix, making it difficult to diagnose or repair at the pixel level. In the MF architecture, it is straightforward to make provisions for pixel level repair using methodologies established with the current architecture. The lack of a practical repair strategy makes the full fill factor architecture incompatible with the current state of maturity of large-area sensor array manufacturing.

In the BL architecture, the *nip* diode is a flat structure with no underlying topography. In the MF structure, the *nip* diode runs over the TFT and makes a back contact to the data metal through a via in 1.5 μm of interlayer dielectric. To minimize any topography-related degradation in sensor characteristics, a tapered via etch profile has been achieved. Figure 3a shows a cross-sectional SEM image of the pixel, and 3b indicates the area where the cross-section was made.

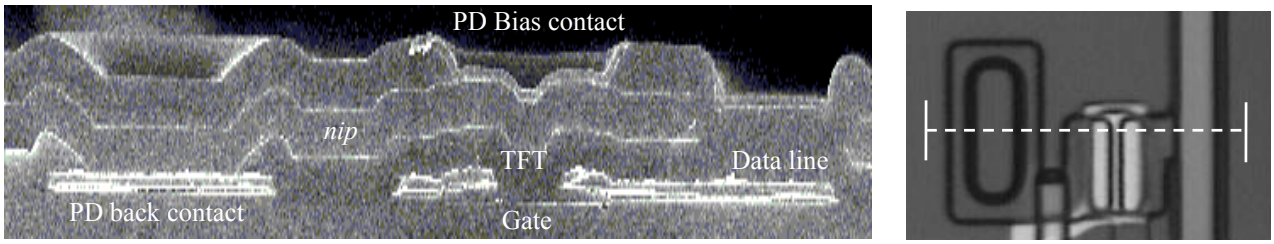


Figure 3. (a) SEM cross-section of the MF pixel. (b) Line across pixel where the cross-section was made.

Figures 4a and 4b show a comparison of the photodiode I(V) characteristics between the BL and MF architectures in the dark and under green LED illumination, respectively. The room temperature data are measured with an electrometer on approximately 100 photodiodes connected in parallel. By optimizing the MF process, we have been able to achieve low sensor dark currents of about 10^{-13} A mm^{-2}, equivalent to the performance of the BL architecture. The very flat photoresponse vs. bias is also independent of process, with 91.4% internal collection efficiency obtained at 0 V bias.

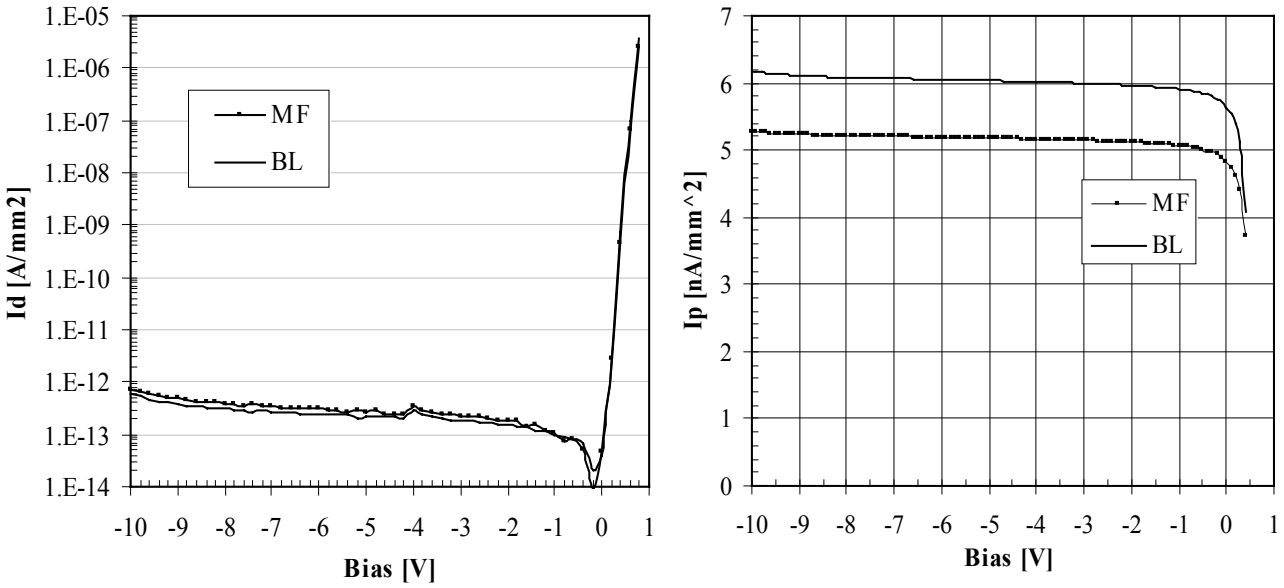


Figure 4. (a) Id(V) for BL and MF photodiodes in the dark. (b) Ip(V) for BL and MF photodiodes under green (565 nm) LED illumination.

3. CLAMP TFT CIRCUIT

By moving the pixel sensor on top of the TFT array matrix, the area within each pixel has been opened up for additional electronic amplification or compensation circuitry. With the present design, we have taken advantage of this freedom to add an extra clamp TFT whose function is to prevent the sensor from going into forward bias at high dose and thus reduce memory effect. For the clamp TFT, a compact, low-leakage TFT structure is added, as indicated in Figure 5.

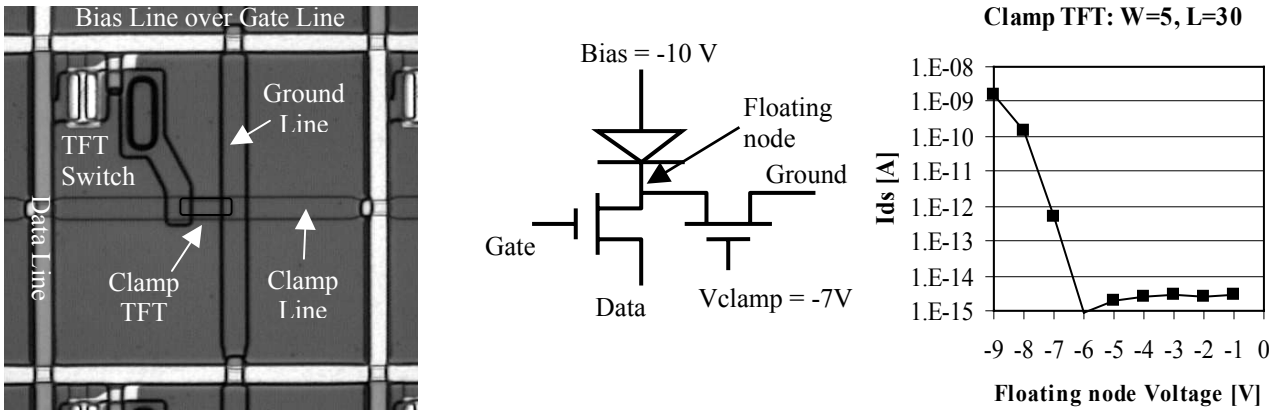
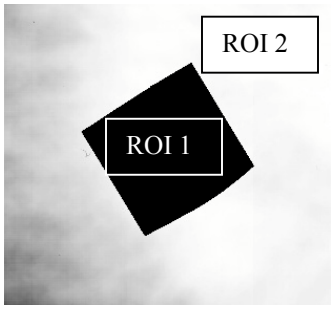


Figure 5. (a) 127 µm clamped pixel layout. (b) Clamped pixel schematic. (c) Clamp TFT I(V) characteristic.

The gate voltage of the clamp TFT is chosen to be 3V higher than the bias voltage and the common line is at ground. Under normal operation at low dose, the internal mode of the pixel is near virtual ground and the clamp TFT is turned off. In normal operation, the clamp TFT off current adds to the pixel noise so the clamp TFT is chosen to be a long channel (25 µm) minimum width (4 µm) TFT to minimize its leakage current. At high dose, the reverse bias across the *nip* diode is reduced. As the voltage on the floating node drops below –6 V, the clamp TFT starts to turn on, bleeding away the excess photo charge and preventing the pixel from going into saturation. The current handling requirement for the clamp TFT under saturation is estimated to be 0.5 nA, which is well within its capability.

In order to illustrate the potential benefit of a clamping TFT, we took images from a conventional a-Si sensor array which has no clamping circuitry. We placed an opaque piece of tape on the surface of the array, and illuminated it with a 10 cd green LED held at a height of 25 cm above the array surface. The LED was used to approximate an ideal point source. We acquired flat-field gain and offset images for various bias voltages from –4 to –10 V, and then imaged the object and its surrounding area as a function of increasing exposure time and bias voltage. We measured the LED dose as a function of LED exposure time using the known sensitivity of the array. The 20 nJ/cm^2 flat-field gain exposure is estimated to be equivalent to a 70 kVp X-ray exposure of 7.8 μGy coupled to a CsI:Tl scintillator.



The image of the tape is shown in Figure 6. We evaluated the image in two regions of interest (ROI's). One ROI was the area beneath the tape, where we observed the image lighten as a function of exposure due to the tape's optical transparency of ~0.1%. We also observed cross-talk from the exposed areas of the array bleeding into the dark area beneath the opaque object at high exposure and large negative bias conditions. This crosstalk, defined as the signal in ROI 1 divided by the flat-field signal, is caused by TFT leakage when the pixel floating node drops below the gate-off voltage (-7 V in this case). The second ROI was outside the opaque object, where we measured the signal integrated between 10 and 20 seconds after each LED pulse (which gives the memory effect, defined as the signal in ROI 2 divided by the flat field signal).

Figure 6. Image of tape and ROI's 1 and 2.

The results are shown in Figure 7.

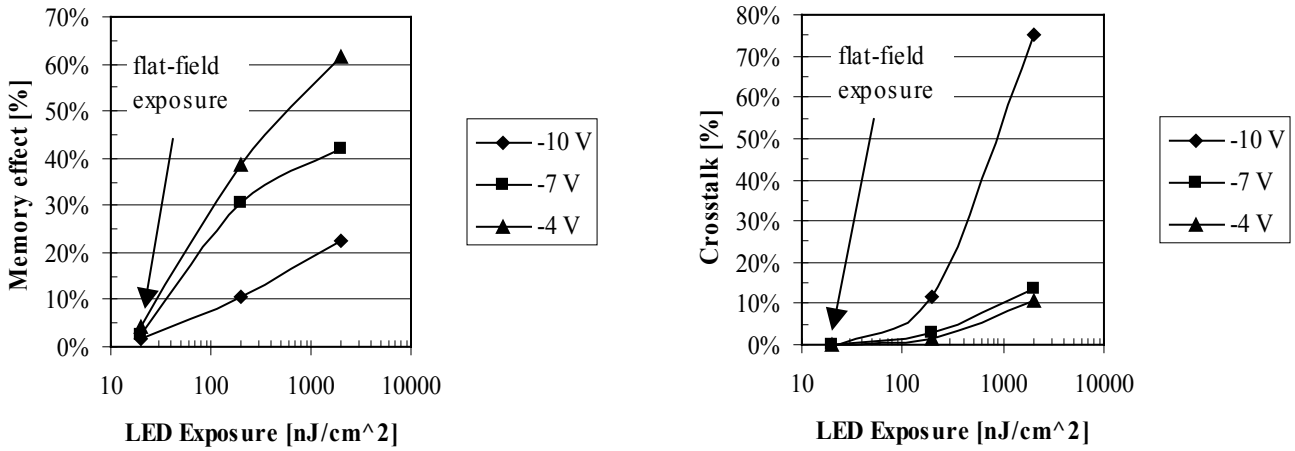


Figure 7. The memory effect and crosstalk as a function of LED exposure and array bias.

We note two major effects: at the flat-field exposure level, the memory effect is small and weakly dependent on bias voltage. As the LED exposure increases above the saturation dose of the pixel, the memory effect increases dramatically, but is diminished as the magnitude of the bias voltage across the photodiode increases. We observed a 2.5X reduction in memory effect in changing the bias from –4V to –10 V. However, the image contrast degrades as a function of increasing bias. The object we used showed a signal level of 10% of the flat-field signal at –4 V bias under the highest exposure used. At this same exposure, the signal at –10 V bias increased to 76%. This 7X loss in contrast is caused by TFT leakage where the photocurrent in the photodiode directly leaks on to the data lines, increasing the signal level under the opaque object. This TFT leakage occurs because the drain of the TFT (connected to the photodiode floating node) drops 3 volts below the off-voltage of the TFT (-7 V), thus allowing the TFT to turn on.

This is what motivated us to introduce a second clamping TFT connected to the floating node, with a second set of gate and source lines. This TFT can be set to leak off excess charge which builds up on the photodiode onto a nonimaging ground line, thus preventing overexposure from degrading the image contrast as described previously. We have

designed and fabricated clamp pixel test structures using the MF architecture, but to date, we have only fabricated and characterized MF arrays made using the conventional, single pass-transistor circuit. The design optimization of these arrays will be the subject of the next section.

4. DESIGN OPTIMIZATION

In order to maximize the fill-factor of the pixel and minimize parasitic coupling of the bias line to the data and gate lines, we put together a model which calculates the data line and gate line capacitance for the idealized pixel structure shown in Figure 8. We used the MIT FastCap model[13] to estimate the parasitic capacitance between the lines and the common bias potential of each photodiode. In this model, we fix the data line width at 6 μm and thickness at 1 μm and varied the separation of the diode collection electrodes from each line. We assumed two 100 μm square, 1.5 μm thick photodiodes (of dielectric constant k=12.0) on each side of a given line, and neglected fringing field capacitances beyond nearest neighbor pixels. The photodiodes are separated from the glass substrate by a 0.5 μm thick SiN layer and a 1.5μm thick SiON interlayer dielectric (ILD) layer, and covered with a 1.5 μm thick layer of passivation. For ease of calculation, we assumed the entire array is immersed in an insulating half-space of dielectric (k=5.7) beneath a half-space of air (k=1.0) situated 1.5 μm above the plane of each photodiode. We used the FastCap model to calculate the capacitance of each line to bias, by summing the capacitance from each line to the adjoining collection electrodes of each diode and to the top surface of each adjoining diode, which are connected to the common bias potential.

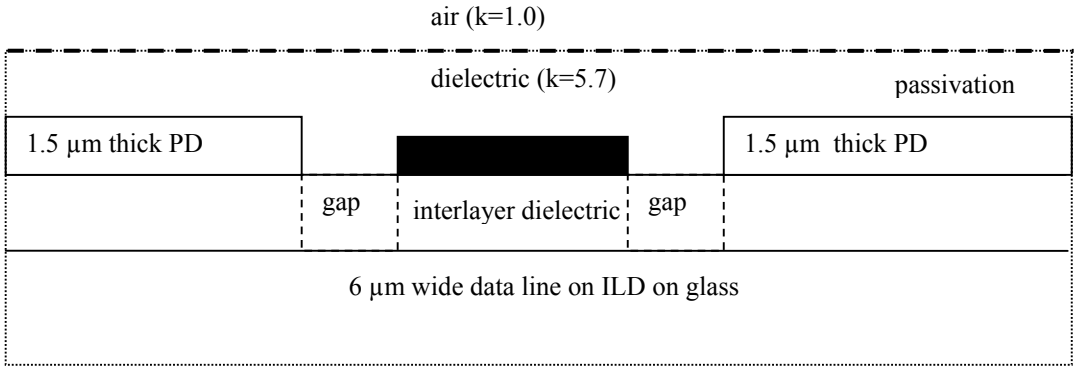


Figure 8. The top of each photodiode (PD) is held at constant bias potential; the bottom of each photodiode forms a floating collection electrode which is strongly coupled to bias potential through the capacitance of each photodiode.

In Figure 9a we show the results of the model calculations for data to bias capacitance Cdb. The model indicates the capacitance Cdb increasing very strongly when the diode overlaps the data line, as would be the case for a 100% full-fill factor architecture. We also show in Figure 9a experimental results measured on test arrays of 127 μm pixels with different gaps between the data line and the photodiodes. We used the experimental results to predict the actual array capacitances.

The model trends and experimental results agree, in that the data line capacitance increases significantly when the line and photodiode begin to overlap and that the capacitance tends to drop off more slowly as the gap becomes small compared to the thickness of the ILD separating the diode from the data line. The numerical model we constructed overestimates the capacitance contribution from the bias to data coupling by as much as 50%, particularly when the diodes overlap the data lines significantly.

Part of the reason for this discrepancy comes from inspection of SEM photomicrographs of the gap between the data line and adjacent photodiode, as shown in Figure 9b. When the photodiode overlaps the data line, the photodiode and the ILD conformally coat the edge of the line, so the spacing between line and diode is maintained at a minimum of the ILD thickness. This reduces the photodiode contribution in capacitance when the overlap is reduced significantly. The model also overestimates the contribution of the direct coupling from data line to the top of the photodiode. The actual diode has a taper to it, whereas the model assumes a vertical structure. Clearly, a more realistic model is needed.

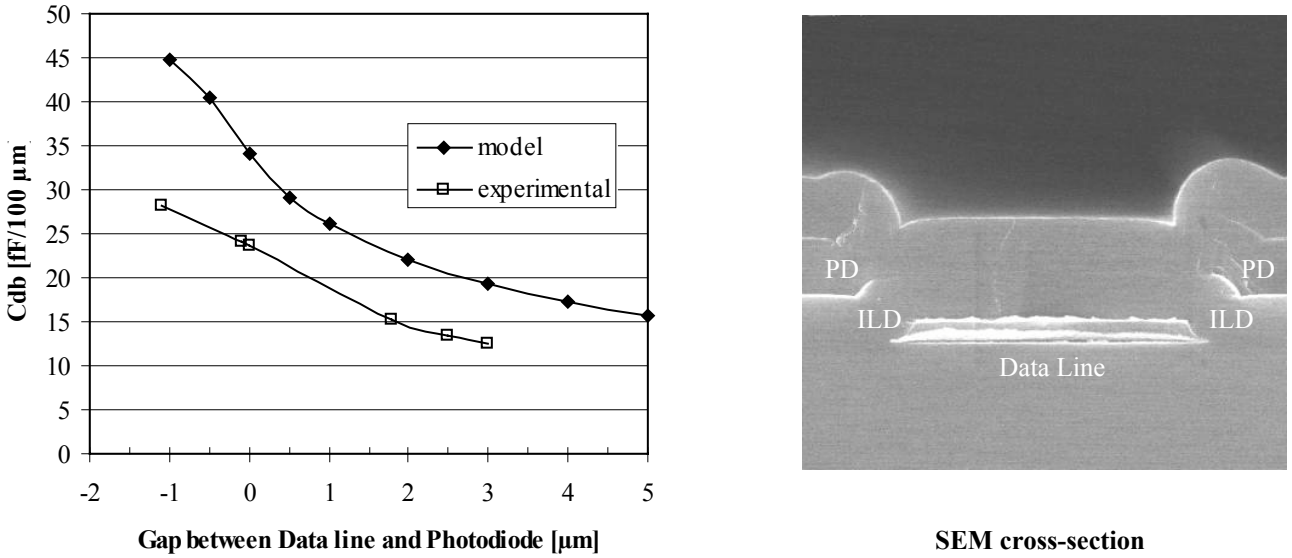


Figure 9. (a) Data line to bias capacitance as a function of gap between the data line and photodiodes, modeled with FastCap and measured on test arrays of 127 µm pixels. (b) SEM cross-section of photodiodes and ILD near a data line.

With the 127 µm size pixel format, we have designed two test arrays of 93x93 and 130x130 mm^2 dimensions. With the bias running over the gate lines, we achieve a fill-factor of 85% and a photodiode capacitance of 1.0 pF. In the following section, we describe some of the measured array characteristics.

5. ARRAY RESULTS

A prototype 768 x 768 pixel "M10" array was assembled with a standard Gd_2O_2S:Tb phosphor screen. The array was operated at 15 fps. The signal was measured in low-gain mode to evaluate the array saturation under room light exposure as a function of bias applied to the photodiodes. The saturated response is shown in Figure 10a below. The curve for bias voltages between –6 V and 0 V is linear and shows the measured photodiode capacitance of 1.0 pF. The x-intercept indicates the 1.6 V virtual ground of the data line, which is set by the readout amplifier. At bias voltages below –6 V, the signal increases strongly. This occurs at the point where the TFTs are no longer fully turned off, so that charge generated during continuous exposure leaks on to the data lines. The signal linearity vs. X-ray dose is shown in Figure 10b. The signal is linear within 0.1% up to 70% of pixel saturation. We measure an X-ray sensitivity of 1.72 Me/mR at -4 V bias, dropping by 10% at 0 V bias. We compared the sensitivity of the detector to a detector with 57% fill factor and the same screen, and determined that the sensitivity of the MaxFill™ array is 55.5% higher.

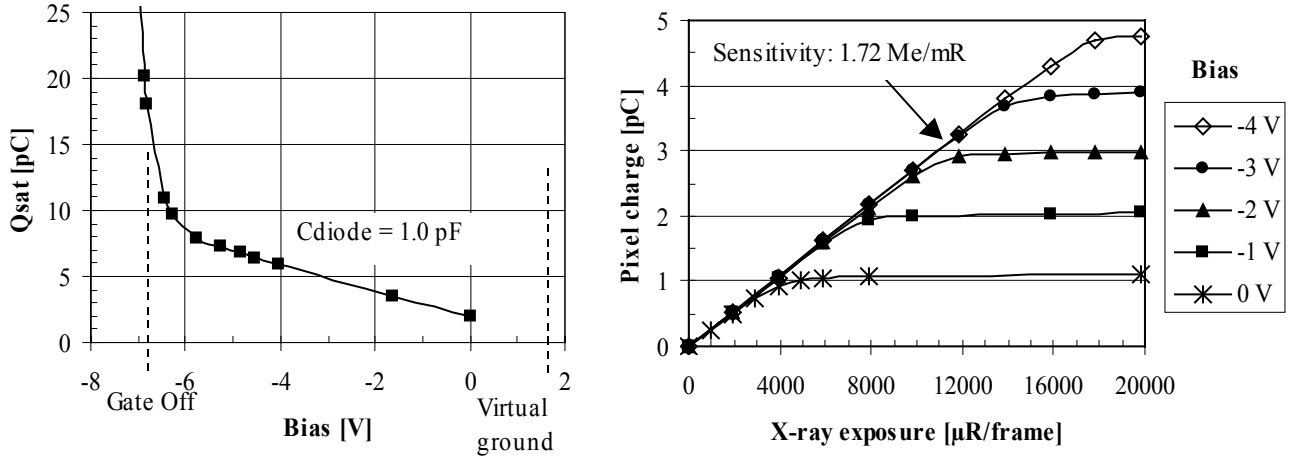


Figure 10. (a) Saturation charge measured vs. bias. (b) Signal linearity vs. X-ray dose at 70 kVp with 4 mm of Al.

Leakage currents were determined by subtracting fast frame-rate offset images (15 fps) from longer 1 fps offset images. A histogram of dark leakage currents for -5V bias is shown in Figure 11a. The peak values of leakage current and full widths at half maximum are shown vs. bias voltage in Figure 11b. For bias voltages below –5 V, the dark currents increase rather strongly and broaden in their distribution. This dispersion in leakage currents correlates with anomalously high photodiode dark currents, and has been corrected in more recent arrays (see Figure 4a). The leakage changes sign at small bias voltage, where the TFT off-current dominates over the PD leakage.

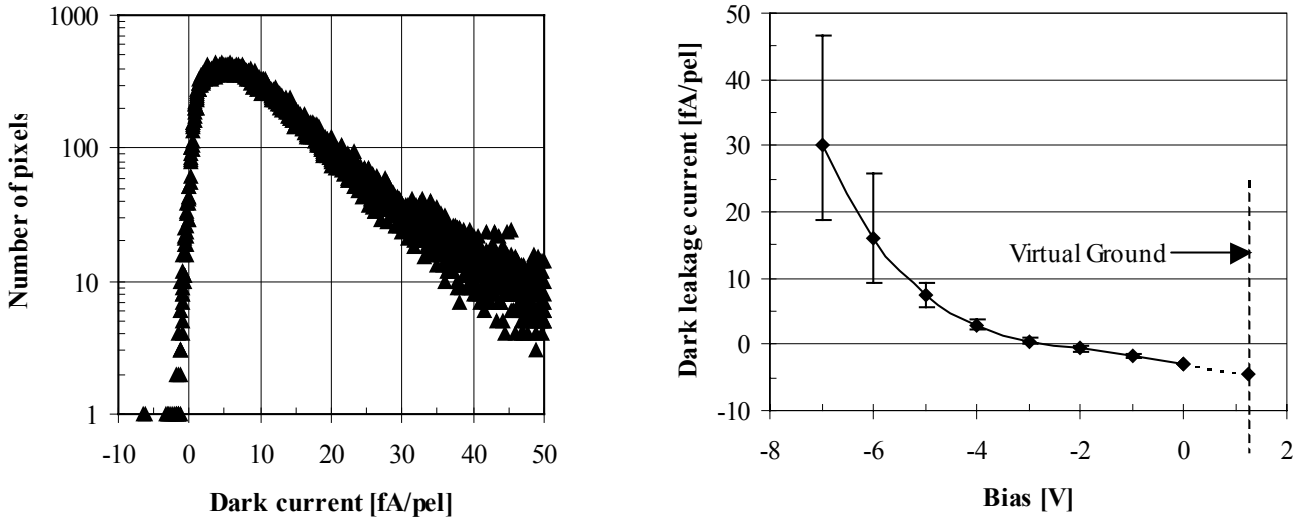


Figure 11. (a) Histogram of dark leakage for Bias = -5 V. (b) Dark leakage current vs. bias voltage.

By subtracting 15 fps offset-corrected X-ray flat-field images from corresponding images taken at 1 fps, we can directly measure the TFT leakage currents in the array. These images were taken at 80 kVp with 4 mm filtration and 10 ms pulse width. The X-rays induce a charge in the photodiodes, which develop a voltage drop Vds across each TFT. In Figure 11a, we show the distribution of TFT leakage currents at 50 mA, or 967 μR/frame. We estimate the Vds across the TFT is –0.26 V. The peak values of off-current are plotted vs. Vds for different levels of X-ray dose. The measurements indicate a TFT off-resistance of approximately $7.8 \cdot 10^{13}$ Ω. This value is about 2 orders of magnitude lower than the DC value of off-resistance, because it takes several seconds for the TFTs to fully turn off, whereas the array is operating here at 15 fps. Note that the leakage extrapolates to 0 at +0.20 V. This is very close to the estimated feedthrough voltage of 0.24 V we expect from the 20V gate swing capacitively coupling to the TFT floating node.

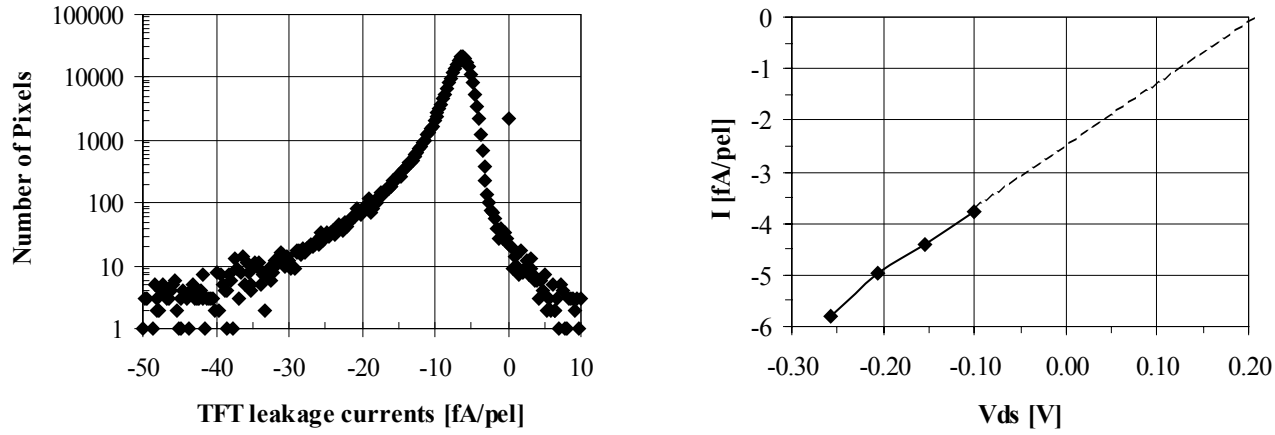
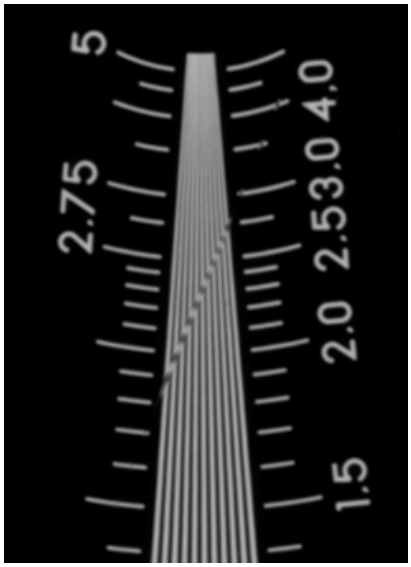


Figure 12. (a) Histogram of TFT leakage currents at 967μR/frame. (b) Peak TFT leakage current vs. estimated Vds.

Images of a resolution target taken at 65 kVp filtered with 1 mm of Cu are shown in Figure 13 taken with two screens, (a) the standard screen used for sensitivity measurements and (b) with a Lanex® fine screen.

(a) Standard screen 

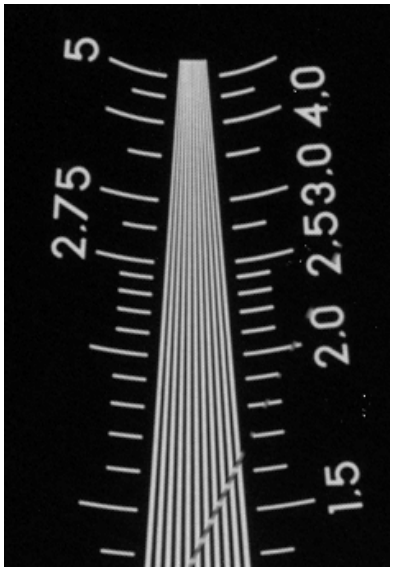
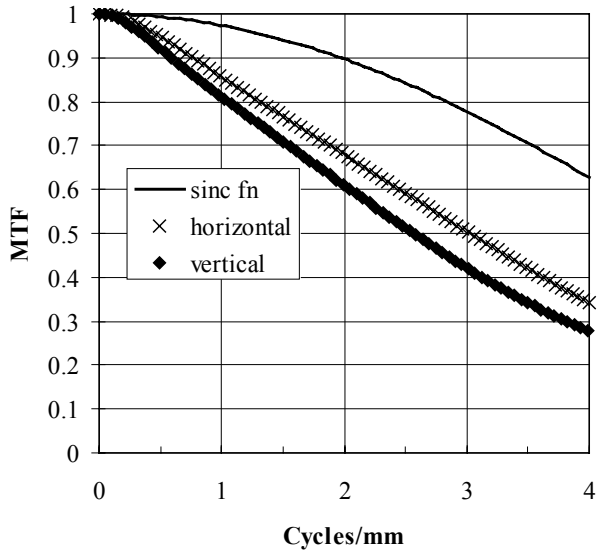
(b) Fine screen 

Figure 13. Images taken from the detector with (a) the standard screen, and (b) a fine screen. The line-pair patterns are fully resolved out to the Nyquist limit of 3.94 LP/mm in both cases, although the resolution is much better with the fine screen.



Images of a slit were taken at 65 kVp and 1 mm Cu filtration. The resulting MTF for the detector using the fine screen is shown in Figure 14. We compare the resolution taken in the horizontal and the vertical directions with the limiting sinc function. We find that the resolution is very comparable to the resolution of 65% at 2 LPM and 28% at 4 LPM reported earlier[14] for the base-line pixel design, using a Lanex® fine screen. The vertical MTF is approximately 8% lower than the horizontal MTF over much of the spatial frequency range due to high-frequency roll-off in the temporal response of the detector electronics. This data suggests that the resolution is limited by that of the fine screen. We plan to check this in the near future by evaluating the array's MTF response with optical resolution techniques.

Figure 14. MTF comparisons between the detector with the fine screen in the vertical and horizontal directions, against theoretical sinc function response.

6. CONCLUSIONS

We have successfully developed a new high fill-factor sensor array designed with manufacturability in mind. The first arrays demonstrate basic feasibility, and results agree with device measurements. Clamped pixel test structures have been designed and fabricated using the MF process architecture. Future plans include further evaluation of standard and clamped pixel arrays made with the MaxFill™ process.

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