Design and Implementation of a Low-Voltage Low-Power Double-Tail Comparator

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Abstract-
In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18μm CMOS technology confirm the analysis results.

Keywords - Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.

I. INTRODUCTION
Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. The designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods, techniques employing body-driven transistors current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures.

Furthermore, based on the double-tail structure proposed in , a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator. Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise offset and random decision errors, and kick-back noise dynamic comparator and double-tail comparator.

II. BLOCK DIAGRAM

![Fig.1: conventional double-tail dynamic comparator](image)

Fig.1: conventional double-tail dynamic comparator
III. DESIGN AND IMPLEMENTATION

A conventional double-tail comparator. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset. The operation of this comparator is as follows (see Fig. 4). During reset phase (CL = 0, Mtail1 and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CL = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by /Mtail1/Cfn(p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes _Vfn(p) to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tLatch.

**Feature Detection using FAST**

**Operation of the proposed comparator**. During reset phase (CL = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CL = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1).

**SYSTEM SOFTWARE**

**Tanner Software:**

Today’s semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.
IV. IMPLEMENTATION RESULT

The presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. The modification is power saving when compared to the conventional dynamic comparator and dual tail comparator.

VI. REFERENCE


