Design and Synthesis of High Speed Low Power Combinational and Sequential Circuits Using Reversible Logic

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Abstract: Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research did in this project aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realize Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as N-bit Ripple-carry Adder/subtractor, comparator D-flip flop and ring counter using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient.

Index Terms— Reversible logic, quantum cost, garbage ouputs.

I. INTRODUCTION

Reversible rationale is broadly utilized in low power VLSI. Reversible circuits are fit for back-calculation and eduction in scattered power, as there is no loss of data [1]. Fundamental reversible gates are utilized to accomplish the required usefulness of a reversible circuit. The uniqueness of reversible rationale is that, there is no loss of data since there is balanced correspondence amongst information sources and yields. This empowers the framework to run in reverse and keeping in mind that doing as such, any middle of the road configuration stage can be altogether inspected. The fan-out of each square in the circuit must be one. This examination paper centers around execution of reversible rationale circuits in which fundamental point is to upgrade speed of the plan. A Reversible adder is outlined utilizing essential reversible gates. Utilizing this adder, a 8-bit reversible swell convey viper is concocted and afterward contrasted and the traditional 8-bit adder as far as speed, basic ways, equipment utilized. At that point utilizing a similar reversible adder, a Wallace tree multiplier has been executed, and contrasted and the traditional Wallace tree multiplier. With the well established actuality that successive circuits are the core of computerized outlining, the plan for the control unit of a reversible GCD processor has been proposed utilizing Reversible rationale gates.

II. REVERSIBLE LOGIC

Boolean rationale is said to be reversible if the arrangement of information sources mapped have an equivalent number of yields mapped i.e. they have balanced correspondence. This is acknowledged utilizing reversible gates in the plans. Any circuit having just reversible gates is equipped for disseminating no power . Objectives of Reversible Logic:

A. Quantum Cost: Quantum cost of a circuit is the proportion of execution cost of quantum circuits. All the more preecisely, quantum cost is characterized as the quantity of rudimentary quantum activities expected to understand an gate.

B. Speed of Computation: The time postponement of the circuits ought to be as low as conceivable as there are various calculations that must be done in a framework including a quantum processor; subsequently speed of calculation is a critical parameter while looking at such frameworks.

C. Garbage Outputs: Garbage yields are those yield signals which don't contribute in driving further squares in the outline. These yields wind up repetitive as they are not required for calculation at a later stage. The trash yields make the framework slower; henceforth for better effectiveness it is important to limit the quantity of waste yields.

D. Feedback: Looping is entirely restricted when planning reversible circuits.

E. Fan-out: The yield of a specific square in the plan can just drive at most one square in the outline. Subsequently it very well may be said that the Fan-out is confined to 1.

III. MAJOR SEVERAL REVERSIBLE LOGIC

3.1 Feynman Gate

It is a 2*2 Feynman gate [13]. The information vector is I (A, B) and the yield vector is O(P, Q). The yields are characterized y P=A, Q=AÅB. Quantum cost of a Feynman gate is 1. Figure 1 demonstrates a 2*2 Feynman gate.

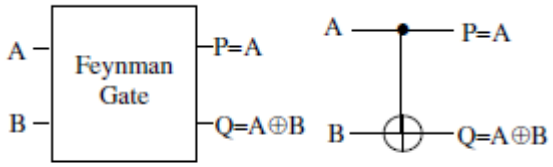

Figure 1: Feynman gate

3.2 Double Feynman Gate (F2G)

It is a 3*3 Double Feynman gate [14].The input vector is I (A, B, C) and the yield vector is O (P, Q, R). The yields are characterized by P = A, Q=AÅB, R=AÅC. Quantum cost of twofold Feynman gate is 2. Figure 2 demonstrates a 3*3 Double Feynman gate.

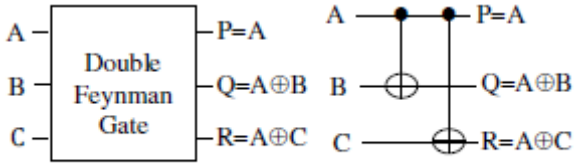

Figure 2: Double Feynman gate

3.3 Toffoli Gate

It is a 3*3 Toffoli gate [6] The info vector is I(A, B, C) and the yield vector is O(P,Q,R). The yields are characterized by P=A, Q=B, R=ABÅC. Quantum cost of a Toffoli gate is 5. Figure 3 demonstrates a 3*3 Toffoli gate.

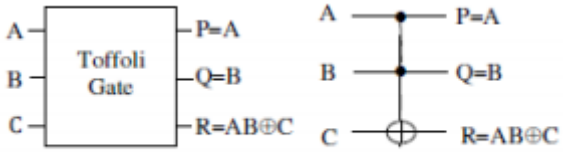

Figure 3: Toffoli gate

3.4 Fredkin Gate

It is a 3*3 Fredkin gate [7]. The information vector is I (A, B, C) and the yield vector is O(P, Q, R). The yield is characterized by P=A, Q= A_ BÅAC and R= A_ CÅAB. Quantum cost of a Fredkin gate is 5. Figure 4 demonstrates a 3*3 Fredkin gate.

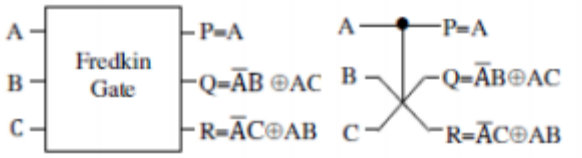

Figure 4: Fredkin gate

3.5 Peres Gate

It is a 3*3 Peres gate [15]. The info vector is I (A, B, C) and the yield vector is O (P, Q, R). The yield is characterized by P = A, Q = AÅB and R=ABÅC. Quantum cost of a Peres gate is 4. Figure 5 demonstrates a 3*3 Peres gate.

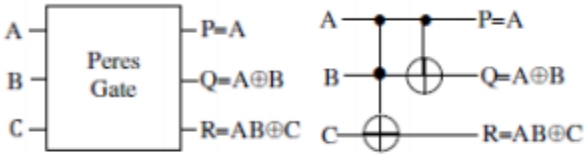

Figure 5: Peres gates

3.6 Double Peres gate

It is a 3*3 Peres gate [15]. The info vector is I (A, B, C) and the yield vector is O (P, Q, R). The yield is characterized by P = A, Q = AÅB and R=ABÅC. Quantum cost of a Peres gate is 4. Figure 5 demonstrates a 3*3 Peres gate.

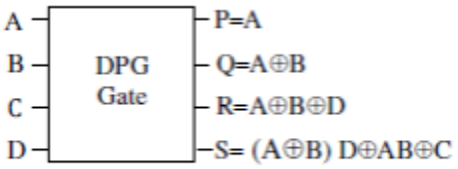

Figure 6: DPG gate

IV. REVERSIBLE N- BIT FULL ADDER/SUBTRACTOR

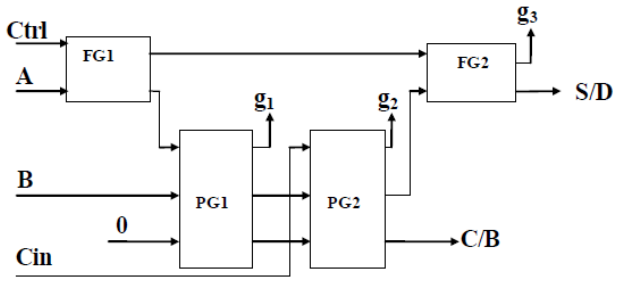

Figure 7. Reversible Full Adder/Subtractor

The Reversible Full Adder/Subtractor Design comprises of two FG, two PG gates, and their interconnections are appeared in the Figure 7. The three information sources are A, B, and Cin, The yields are S/D and C/B. For Ctrl esteem zero the circuit performs addition and Subtraction for Ctrl esteem one. The quantities of Garbage inputs are 1 spoken to by consistent zero. The Garbage yields are 3 spoken to by g1 to g3. The Quantum Cost for the outline is 10. A Quantum Cost preferred standpoint of 11 is gotten when contrasted with Adder/Subtractor utilizing fundamental gates and of 4 when contrasted with Adder/Subtractor utilizing cmos rationale. Quantum Cost advantage is because of the acknowledgment of Arithmetic squares utilizing two PG gates as against two F and one TR gate for Design I and two TR gate.

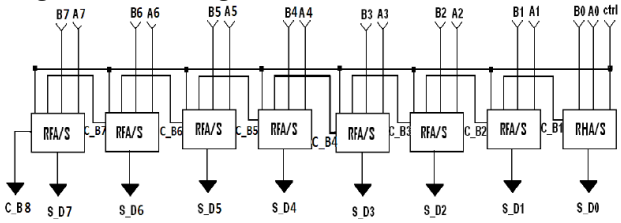

Figure 8. Reversible N-bit Adder/Subtractor

The tasks of both expansion and subtraction can be performed by a one basic double viper. Such twofold circuit can be outlined by including a faymen gate with each full adder as appeared in underneath figure. The figure above demonstrates the 4 bit parallel twofold viper/subtractor which has two 4 bit contributions as A3A2A1A0 and B3B2B1B0.The mode input control line M is associated with convey contribution of the minimum note worthy piece of the full adder. This control line chooses the sort of task, regardless of whether expansion or subtraction. At the point when M= 1, the circuit is a subtractor and when M=0, the circuit moves toward becoming adder. The Ex-OR gate comprises of two contributions to which one is associated with the B and other to enter M. At the point when M = 0, B Ex-OR of 0 deliver B. At that point full adders include the B with A with convey input zero and thus an expansion task is performed. At the point when M = 1, B Ex-OR of 0 create B supplement and furthermore convey input is 1. Consequently the supplemented B inputs are added to An and 1 is included through the info convey, only a 2's supplement task. In this manner, the subtraction activity is performed.

V. PROPOSED REVERSIBLE NUMERICAL COMPARATOR

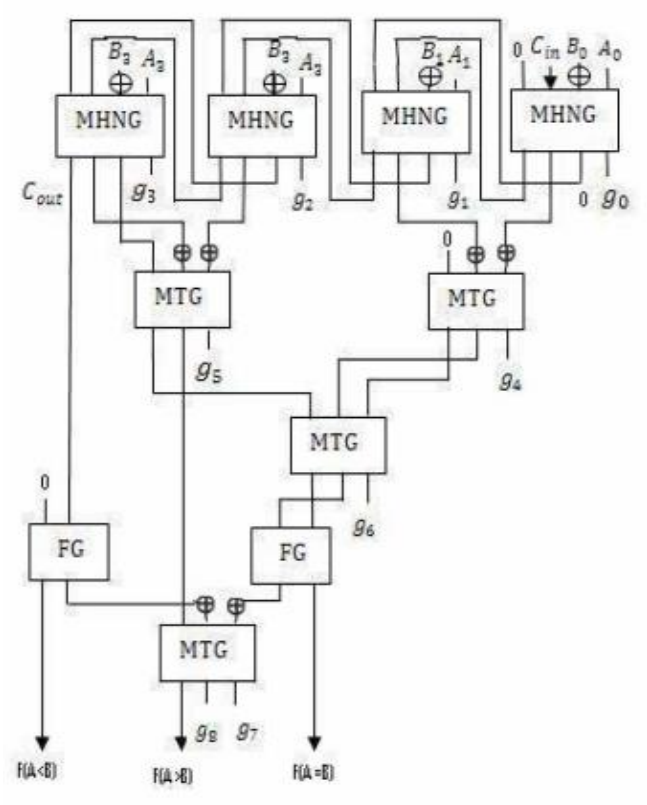

Fig. 9 Proposed reversible comparator

Our proposed 4-bit reversible numerical comparator essentially contains 4 MHNG gate as full adder , and 4 three info MTG and two FG for fan-out and some not gate. It can look at the estimation of two paired numbers An and B by utilizing A-B. We have demonstrated our proposed reversible numerical comparator in Fig.9.

VI. REVERSIBLE D FLIP-FLOP

In this plan reversible edge-activated D Flip-slump is utilized for state advances. Two D-locks are associated in Master-Slave mode to go about as an edge-activated D Flip-tumble. Reversible D-lock is outlined utilizing Feynman and Fredkin gates.

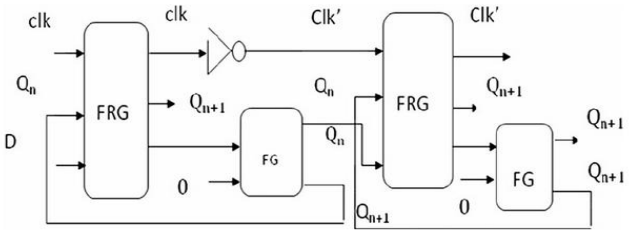

Fig.10 Proposed D Flip-Flop

The D Flip-Flop can be mapped with two FRG and two FG gate. The FRG gate needs D, CLK, 1 and 0 inputs individually in first, second, third and fourth info. The yield D. CLK and D. CLK are acknowledged by one BME in the second and fourth yields. Presently, the second yield D. CLK that is can be utilized as second contribution of one Peres gate.

VII. REVERSIBLE RING COUNTER

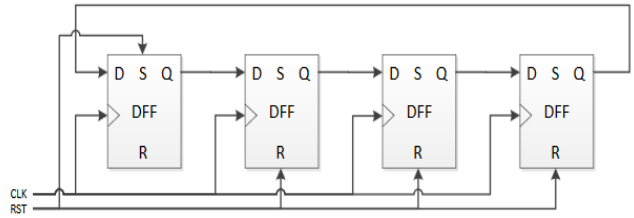

Fig.12 Proposed Ring Counter

The fourth yield D. CLK that is R can be utilized as second contribution of another Peres gate. Along these lines, our plan needs just 3 reversible rationale gates with 4 junk yields to outline of D Flip-Flip. The proposed outline of D Flip-Flip is appeared in Figure 10.

VIII. SIMULATION RESULTS

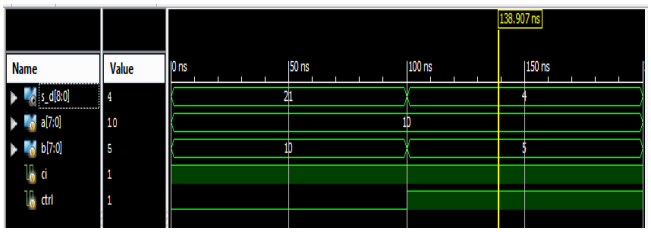

Fig.13 Adder/Subtractor

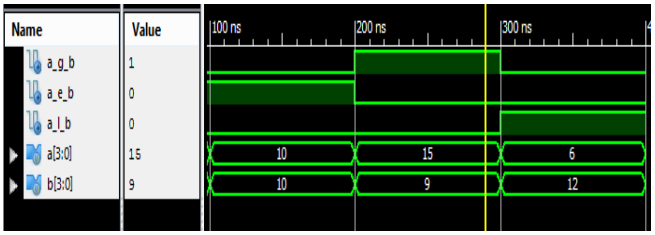

Fig.14 comparator

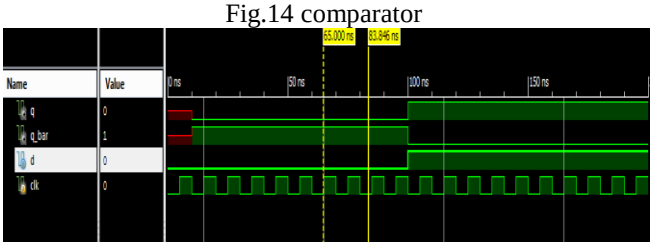

Fig.15 D Flip-Flop

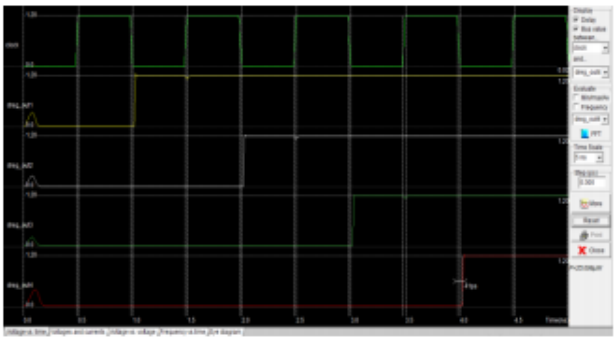

Fig.16 Ring Counter

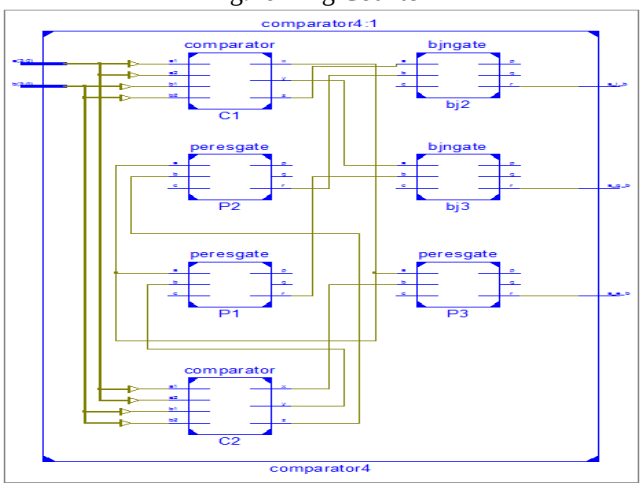

Fig.17 RTL SCHEMATIC of Comparator

IX. CONCLUSION

It can be seen that the performance of digital circuits can be enhanced using reversible gates and have compared N-bit ripple carry reversible adder, Comparators, D Flip-Flop and Ring counter with an irreversible design styles in terms of speed and power; thereby concluding that reversible designs are faster and power efficient. Furthermore, this concept is extended to combinational circuits such as a Wallace tree multiplier using reversible gates, which were simulated and respective results validate prior inferences.

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