



4-Mbit (1M x 4) Static RAM

Part Number: DPA71046D02A

The DPA71046D02A is a high-performance CMOS static RAM organized as 1M words by 4 bits.

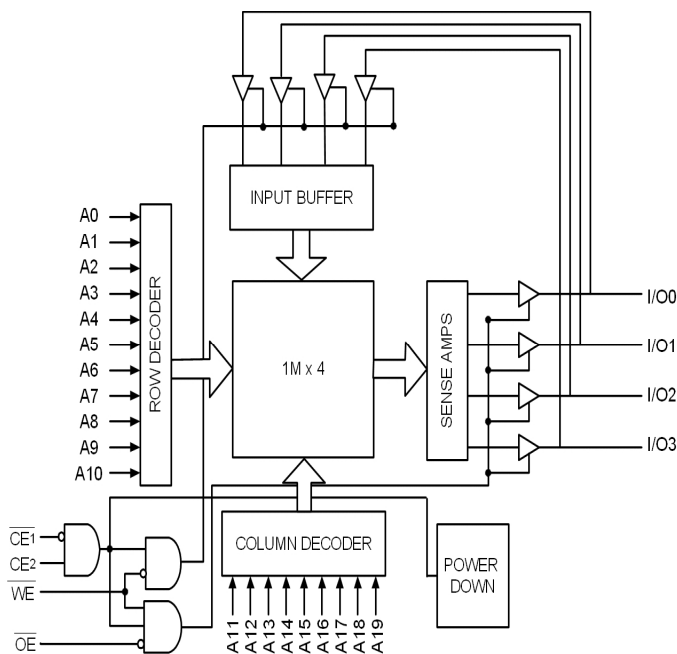
Writing to the device is accomplished by enabling the chip (by taking \overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW.

Reading from the device is accomplished by enabling the chip (\overline{CE}_1 LOW and CE_2 HIGH) as well as forcing the Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH.

The Input/Output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 LOW or CE_2 HIGH), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

- -55° to +125° operating temperature
- High speed
 - $t_{AA} = 12 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA @ } 12 \text{ ns}$
- Low CMOS Standby Power
 - $I_{SB2} = 10 \text{ mA}$
- Supply voltage
 - 5.0 V dc
- Data Retention at 2.0 V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- 54-pin SO ceramic flatpack, same footprint as 54-pin TSOP II
- Custom packaging available
- This product uses Cypress CY1C1046D die and is tested to meet military and space operational environment requirements.

Logic Block Diagram



Pin Configuration

