NAND Technology Improvement Technique

Priyanka Sahu

Asst. Prof., Electronics and Telecommunication Engineering Department, Kalinga University, Raipur, India

Abstract - A digital delay line is a discrete element in digital filter theory, which allows a signal to be delayed by a number of samples. If the delay is an integer multiple of samples digital delay lines are often implemented as circular buffers. This means that integer delays can be computed very efficiently. Digital delay lines are widely used building blocks in methods to simulate room acoustics, musical instruments and digital audio effects. The DCDL are designed glitch free and it is implemented in the application for the better performance. A necessary condition to avoid glitching is designing a DCDL which have no-glitch in presence of a delay control code switching.

Keywords - Digit delay Lines, NAND-based DCDL, CMOS

I. INTRODUCTION

A glitch is a short-lived fault in a system. It is often used to describe a transient fault that corrects itself, and is therefore difficult to troubleshoot. The term is particularly common in the computing and electronics industries, and in circuit bending, as well as among players of video games, although it is applied to all types of systems including human organizations and nature. An electronics glitch is an undesired transition that occurs before the signal settles to its intended value. In other words, glitch is an electrical pulse of short duration that is usually the result of a fault or design error, particularly in a digital circuit. For example, many electronic components, such as flip-flops, are triggered by a pulse that must not be shorter than a specified minimum duration; otherwise, the component may malfunction. A pulse shorter than the specified minimum is called a glitch. A related concept is the runt pulse, a pulse whose amplitude is smaller than the minimum level specified for correct operation, and a spike, a short pulse similar to a glitch but often caused by ringing or crosstalk. A glitch can occur in the presence of race condition in a poorly designed digital logic circuit.

In recent deep-submicrometer CMOS processes, time-domain resolution of a digital signal is becoming higher than voltage resolution of analog signals. This claim is nowadays pushing toward a new circuit design paradigm in which the traditional analog signal processing is expected to be progressively substituted by the processing of times in the digital domain. Within this novel paradigm, digitally controlled delay lines (DCDL) should play the role of digital-to-analog converters in traditional, analog-intensive, circuits. From a more practical point of view, nowadays, DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), alldigital spread-spectrum clock generators (SSCGs).

II. LITERATURE REVIEW

The recently proposed NAND-based digitally controlled delay- lines (DCDL) present a glitching problem which may limit their employ in many applications. This paper presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications. The proposed NAND based DCDL maintains the same resolution and minimum delay of previously proposed NAND-based DCDL. This paper gives two contributions to the design of NAND-based DCDLs. First it is shown and analyzed the glitching problem of the NAND-based DCDL.

III. METHODOLOGY

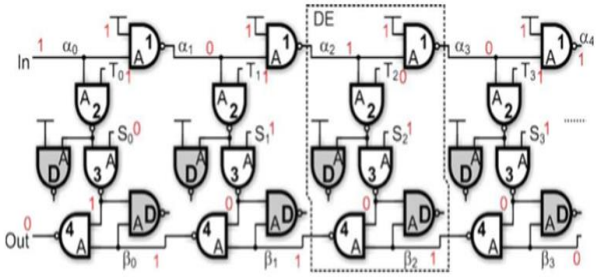

Figure 1: Proposed glitch free NAND-based DCDL (inverting topology).

The structure of proposed DCDL is shown in Fig. 1. In this figure "A" denotes the fast input of each NAND gate. Gates marked with "D", represents dummy cells added for load balancing. Two sets of control-bits, Si and Ti, control the DCDL. The Si bits encode the control-code by using a thermometric code: Si =0, for i<c and Si =1 for i ≥ c. The Ti bits encode again by using a one-cold code: Tc+1.=0, Ti =1 for i ≠ c+1. The Fig. 1 shows the state of all signals in the case, in =1, c=1. According to the chosen control-bits encoding, each delay-element (DE) can be in one of three possible states.

The DEs with i<c are in pass-state (Si=0, Ti=1) . In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state (Si=Ti=1) . In this state the upper input of the DE is passed to the output of NAND "3". The next DE i=c+1 is in post-turn-state (Si=1, Ti=0). In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining DEs are again in turn-state.

IV. RESULTS

In order to verify the effectiveness of proposed solution, the circuits of have been designed for a 90-nm CMOS

technology, with 1.0Vsupply voltage and using standard-Vt devices. The considered length, for all DCDLs, is 64 elements. All NAND based DCDLs have been sized in order to optimize tR. All NAND gates present a ratio , 2WP/WN =1.5 where WP and WN represent the widths of PMOS and NMOS, respectively. In proposed DCDL the INL is improved by slightly changing the ratio WP/WN of NAND "3" in each DE. This NAND gate, in fact, presents opposite switching for odd and even delay control-codes and is, therefore, responsible for an asymmetry in the minimum delay between these two conditions. This asymmetry is the major contribution to the INL of NAND-based DCDL.

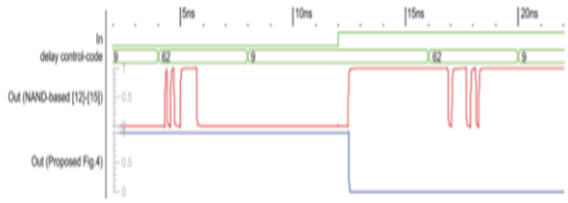

Figure 2: Transient simulations highlighting glitching problems of the NAND-based DCDL of [1]–[2] and the glitch-free operation of proposed DCDL.

V. CONCLUSION

A NAND-based DCDL which avoids the glitching problem of previous circuit [1]–[2] has been presented. A timing model of the novel DCDL structure has been developed to demonstrate the glitch-free property of the proposed circuit. As an additional result, the developed model provides also the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. Two different driving circuits for the DCDL control-bits, which verify the given timing constraints, have been also proposed in the paper. The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches.

VI. REFERENCES

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