*International Journal of Modern Science and Technology* *Vol. 2, No. S1, 2017. Page 20-25.*
***http://www.ijmst.co/*** ***ISSN: 2456-0235.***

***Research Article***

# Three phase grid connected transformer less mosfet Inverter for photovoltaic system

**V. Suriyakala, V. Mohan, B. Amalore Naveen Antony**

Department of Electrical and Electronics Engineering, E.G.S. Pillay Engineering College, Nagapattinam, India.
Corresponding author's e-mail: kala.suriya.suriya47@gmail.com

**Abstract**

The unipolar sinusoidal pulse width modulation (SPWM) full-bridge transformer less photovoltaic (PV) inverter can achieve high efficiency by using latest super-junction metal oxide semiconductor field effect transistor (MOSFET) together with silicon carbide (Sic) diodes. However, the MOSFETs are limited to use in transformer less PV inverter due to the low reverse recovery characteristics of the body diode. In this paper, a family of new transformer less PV inverter topology for single-phase grid-tied operation is proposed using super-junction MOSFETs and Sic diodes as no reverse recovery issues are required for the main power switches for unity power operation. In addition, dead time is not necessary for main power switches at both the high frequency commutation and the grid zero crossing instant, results low current distortion at output. The dc operating principles of the proposed inverter and the voltage balancing method of the multilevel inverter is controlled with Sinusoidal Pulse-Width Modulation (SPWM). This paper contains theoretical analysis and simulation result of this novel multilevel inverter. Finally, a 1kw prototype is built and tested to verify the theoretical analysis. The experimental results show 98.5% maximum efficiency and 98.32% European efficiency. Furthermore, to show the effectiveness, the proposed topology is compared with the other transformer less topologies.

**Keywords:** DC–AC Inverter; Digital Signal Processor; Maximum Power Point Tracking; Multi Level Inverter; Sinusoidal Pulse With Modulation.

## Introduction

Recently, transformer less inverter has been found a one of the excellent solution for grid-tied PV application because of its higher conversion efficiency, lower cost, smaller size, and light weight [1]. Due to the loss of galvanic isolation between the PV module and the grid, a direct path is formed to flow leakage current which generally depends on the non-negligible parasitic capacitance between the PV module and the ground [2], and the amplitude of fluctuating CM voltage. Another important concern of transformer less inverter is the efficiency that can be improved by optimal design. These two issues (efficiency and leakage current) are the major force in pushing progressive development of transformer less grid-tied PV inverter [3]. Voltage sag is defined by the IEEE 1159 as the decrease in the RMS voltage level to 10%-90% of nominal, at the power frequency for duration of half to one minute.

Voltage swell is defined by IEEE 1159 as the increase in the RMS voltage level to 110%-180% of nominal, at the power frequency for duration of half cycles to one minute. Voltage fluctuations, often in the form of voltage sags/swells, can cause severe process disruptions and result in substantial economic loss. So, cost effective solutions which can help such sensitive loads ride through momentary power supply disturbances have attracted much research attention [4]. In order to reduce the leakage current, a lot of in-depth researches have been conducted in the literature, where a new freewheeling path has been introduced to decouple the PV module from the grid during freewheeling period. However, due to poor reverse recovery of MOSFETs slow body-diode, it is limited to use in transformer less inverter

*Received: 10.04.2017; Received after Revision: 05.05.2017; Accepted: 06.05.2017; Published: 07.05.2017*

[5]. In the MOSFET based transformer less topologies for grid-tied PV application will be reviewed and discussed based on their circuit structure, efficiency and CM voltage clamping capability. Some studies have been implemented to simplify the circuit and improve the balance speed by multistage equalization [6,7]. Some zero voltage and zero current switching techniques are also used to reduce the loss of the equalization circuit [8].

A fluctuating CM voltage could also be observed because the freewheeling path potential is not clamped at the mid-point of dc link. An extension of H5 topology is presented in [9] called optimized H5 (oH5) topology, where an extra switch (S6) has been added with the H5 topology to clamp the CM voltage at the half of input voltage as demonstrated [10]. As a result of leakage current flowing through the system, the grid current harmonics and system losses are increases, strong conducted and radiated electromagnetic interference are created, and more significantly, gives rise to safety issues [11].

The CM characteristics of this topology are better than other topologies because of the bi-directional clamping branch. During freewheeling mode, either diode D1 or D2 can be conducted based on whether the freewheeling path potential (VAN≈VBN) is higher or lower than half of the dc link voltage [12]. Another explicit transformer less topology proposed in [13] called H5 topology, made up by adding an extra switch in the dc side of FB inverter. In this topology, the freewheeling current flows through S1 and body diode of S3 during positive half cycle, and S3 and body diode of S1 during negative half cycle.

## Proposed System

### *Control Method of Mosfet*

The H-bridge is just used to alternate the direction of the dc bus voltage, so the reference voltage of the dc bus is the absolute value of the ac reference voltage, just like a half-sinusoidal-wave at a steady state. It means that not all the battery cells are needed to supply the load at the same time. As the output current is the same for all cells connected in the Fig. 1, the charged or discharged energy of each cell is determined by the period of this cell connected into the circuit, which can be used for the voltage or energy equalization (Fig. 1).

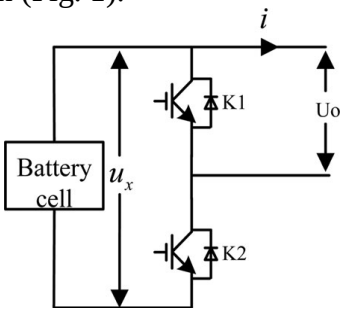


Fig. 1. Output voltage current of the battery and cell

For the cascaded multilevel converters, generally there are two kinds modulation method: phase-shift PWM and carrier cascaded PWM. As the terminal voltage or SOC balance control must be realized by the PWM, so the carrier-cascaded PWM is suitable as the modulation ratio difference between different cells can be used for the balance control. In the proposed PWM method, the carrier arranged by terminal voltage can realize the terminal voltage balance, while the carrier arranged by SOC can realize the SOC balance. Since the SOC is difficult to be estimated in the batteries in practice, the terminal voltage balance is usually used. Normally, the cut-off voltage during charge and discharge will not change in spite of the variation of manufacturing variability, cell architecture, and degradation with use (Fig. 2, 3 and 4). So the overcharge and over discharge can also be eliminated even the terminal voltages are used instead of the SOC for the carrier-wave arrangement.

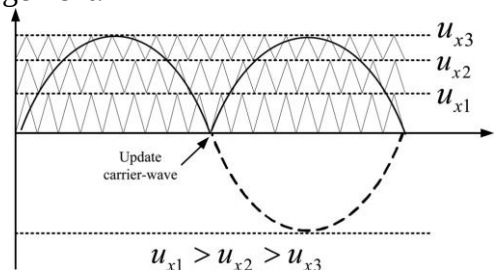


Fig. 2. Carrier wave during discharging

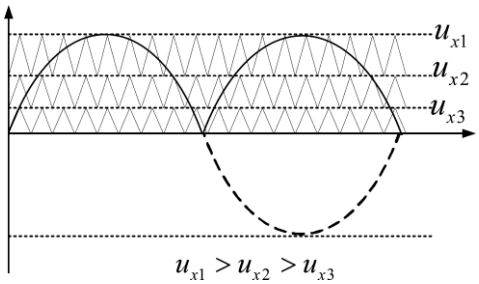


Fig. 3. Carrier wave during charging

 

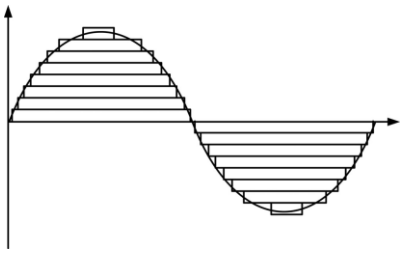

Fig. 4. Base frequency modulation

### *Charging method*

In the system using the proposed circuit a dc voltage source is needed for the battery charging. The charging current and voltage can be controlled by the proposed converter itself according to the necessity of the battery cells. The charging circuit is shown in Fig. 5, 6 and 7. Proposed system for simulation is shown in Fig. 8.

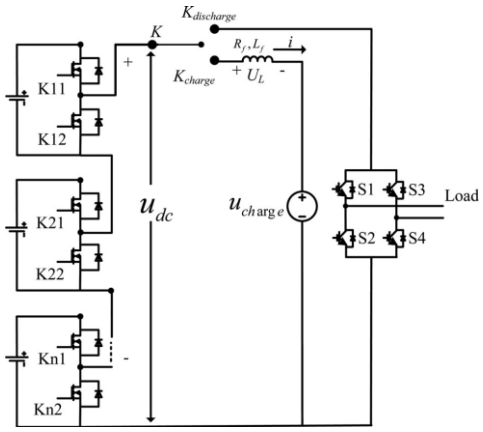


Fig. 5. Charging circuit of battery with dc source

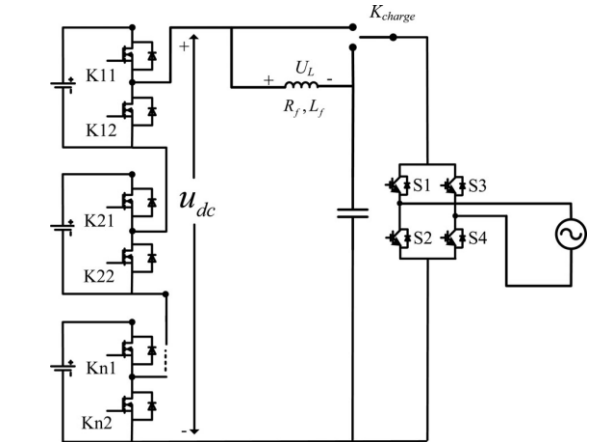


Fig. 6: Charging circuit of battery with ac source

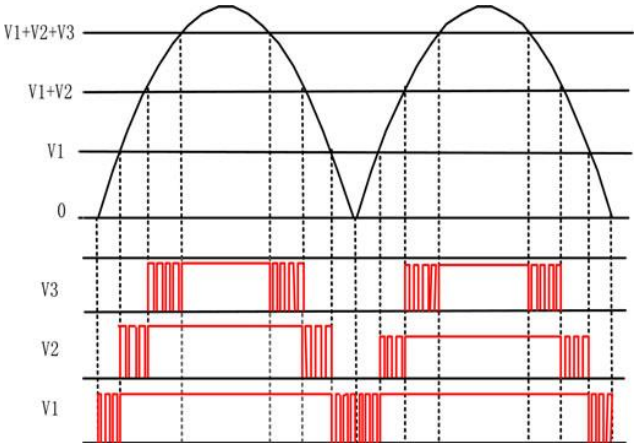


Fig. 7. Intermittent charging current of battery cell

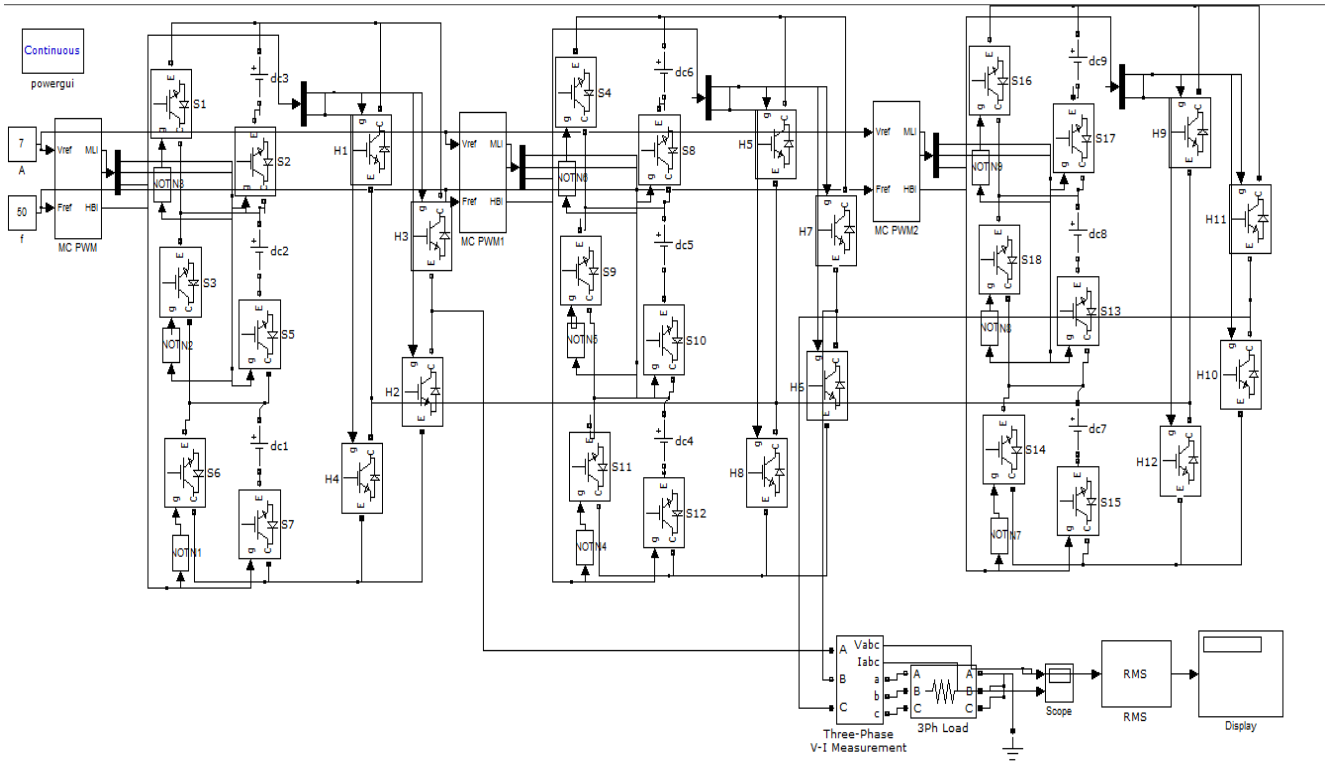


Fig. 8. Proposed system for simulation

 

### *Output waveforms*

The output voltage, current waveforms are shown in Fig. 9.

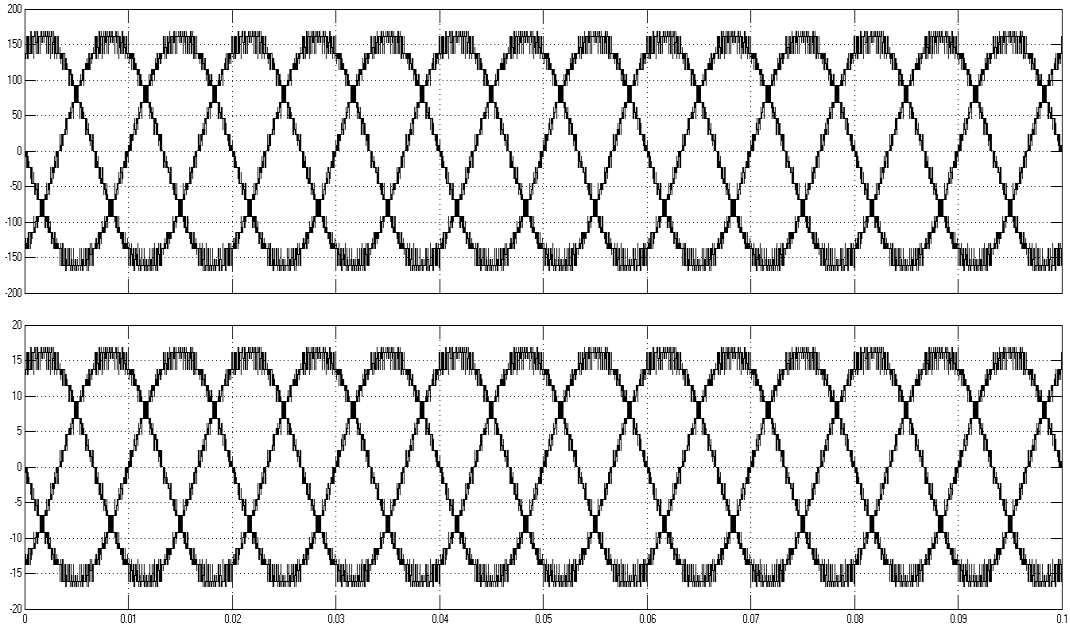

Fig. 9. Output voltage and current waveform

### Simulation Results

To verify the proposed scheme in Fig.10, MATLAB/SIMULINK software was implemented. The experimental results are presented for different levels of using sinusoidal PWM technique. In SPWM control the pulse widths are generated by comparing a triangular reference signal with carrier sinusoidal signal.

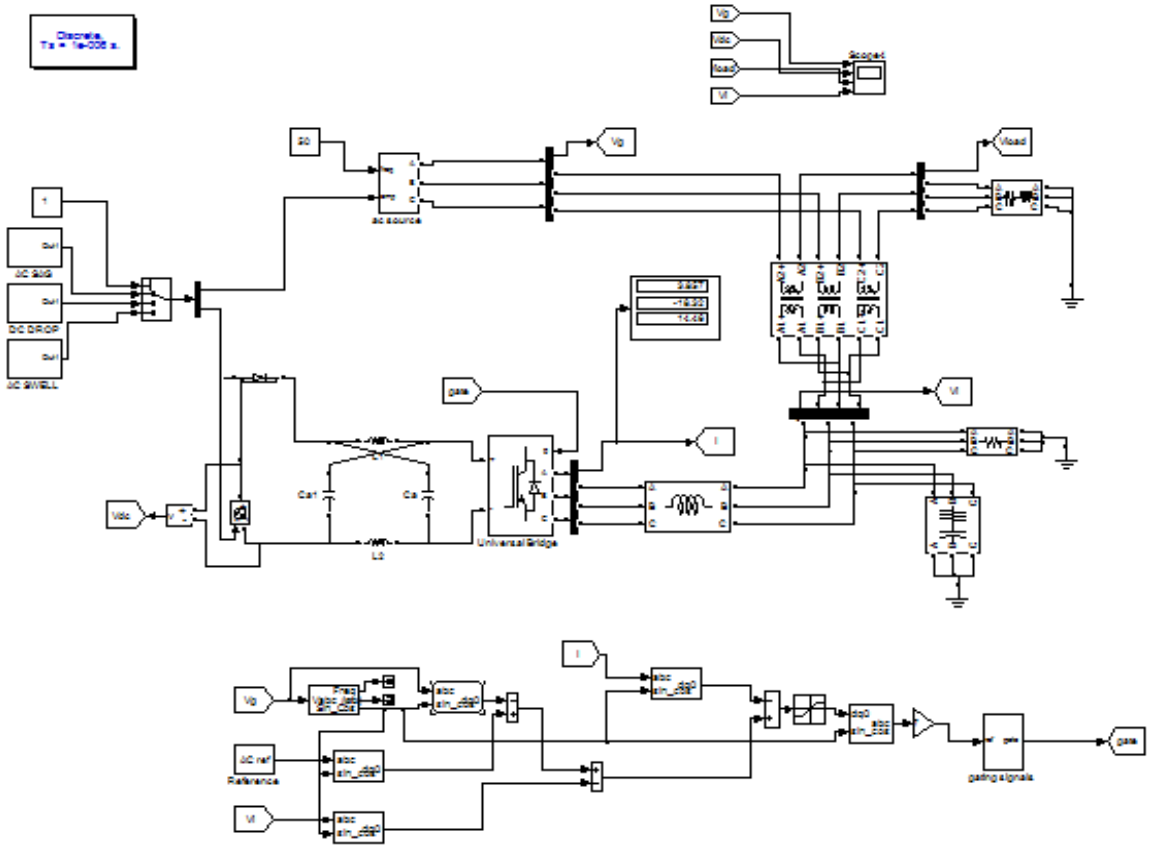

Fig. 10. Simulation Model of transformer less mosfet photovoltaic system

### *Voltage Swell*

The three phase voltage swell is simulated for 0.5 m sec from t=0msec to t=0.5 m sec as shown in Fig. 11. The DVR regulate the load voltage to the reference voltage by injecting appropriate voltage component (negative voltage magnitude).

### *Voltage Sag*

The three phase voltage sag is simulated for 0.5 m sec from t= 1.5 m sec to t=2 m sec as shown in Fig. 11. As in the case of voltage swell, the DVR injects appropriate voltage to regulate the load voltage to reference voltage.

The simulation results illustrates that the proposed Z-Source inverter control scheme restoring the DC voltage across the DC-link during the voltage is very effectively. The voltage swell and sag mitigation is performed with a smooth, stable and rapid DVR response.

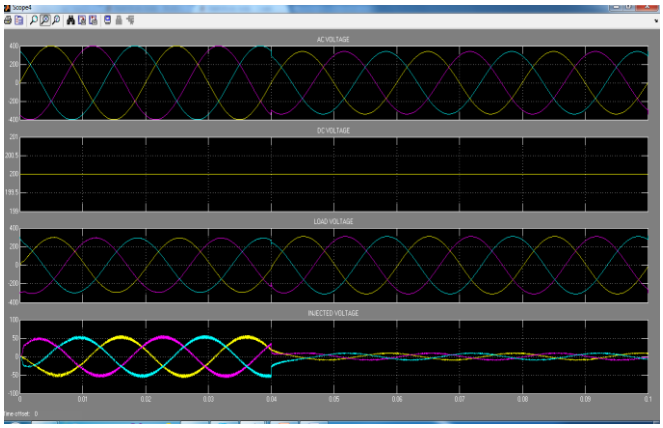


Fig. 11. Simulation Result for Voltage Swell and DVR Compensation

In Fig.12 shows the FFT analysis of Existing system. Magnitude is taken in the y-axis and Frequency in the x-axis. Here Fundamental frequency (50Hz)=161 THD=6.72.It shows that the harmonics is little compared to the base-frequency component in Fig. 13.

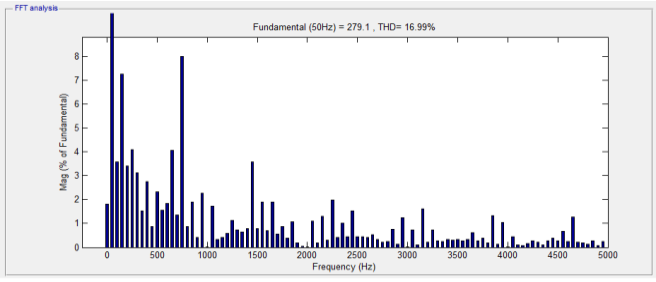


Fig. 12. FFT Analysis Voltage THD Response 16.99%

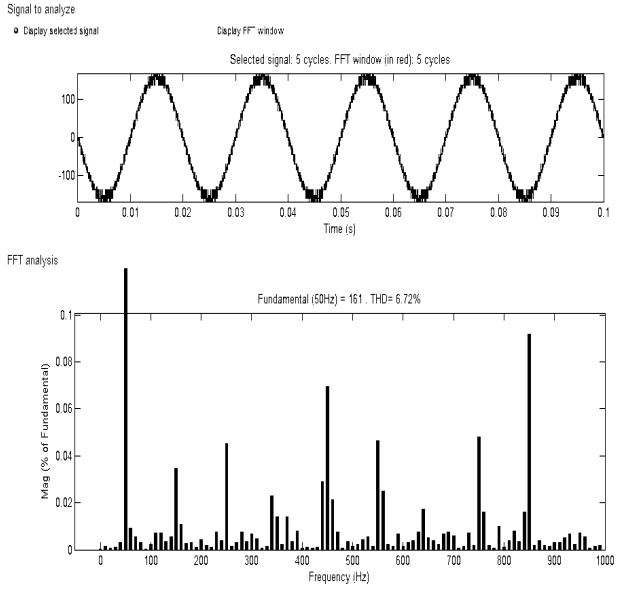


Fig. 13. FFT Analysis of Proposed system

A complete analysis of both bipolar (for two-level inverters) and unipolar (for three-level inverters) methods has been widely. We now develop an analysis of the MCPWM method for multilevel inverters. We refer to the system outlined in Fig.14. For the proposed multilevel generalization of the PWM method; we take as a starting point the unipolar technique. The idea we follow is to use several triangular carrier signals, keeping only one modulating sinusoidal signal.

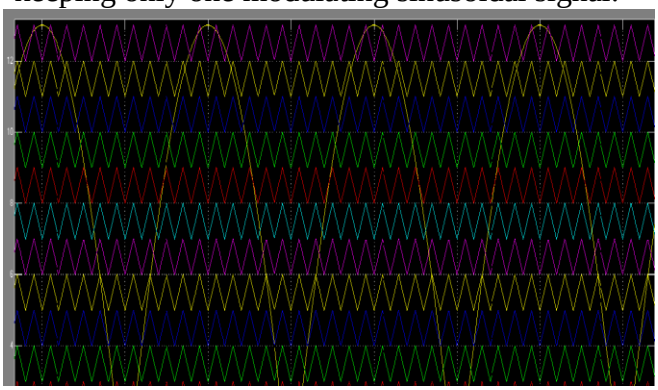

Fig. 14. Output waveform for pulse generation circuit

In order to verify the performance of the proposed topology and to compare with other topologies, a universal prototype is built and tested. The photograph of the laboratory prototype is given in Fig. 15 and the specifications are listed in TABLE III. The capacitance between the PV module and the ground is emulated using a thin film capacitor of 75nF.

 

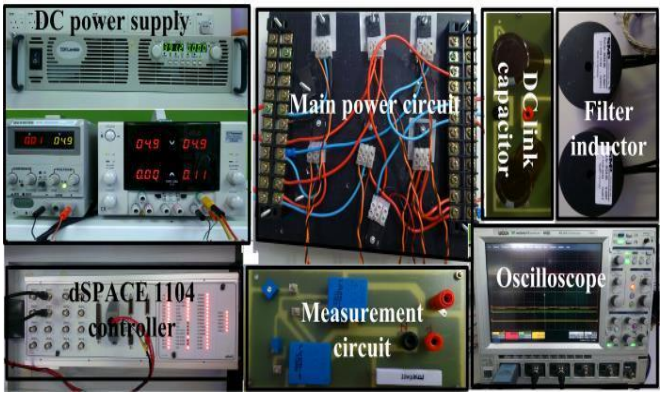


Fig. 15. Hardware prototype

## Conclusions

In this paper, a family of new efficient transformer less inverter for grid-tied photovoltaic power generation system is presented using super-junction MOSFETs as main power switches. The main advantages of the proposed topology are as follows: High efficiency over a wide load range is achieved by using MOSFETs and Sic diodes.CM voltage remains constant during all operation modes due to the added clamping branch, results low leakage current, Like as isolated full-bridge inverter, excellent DM characteristics are achieved with unipolar SPWM, PWM dead time is not required for main power switches, results low distortion at output.

## Conflict of interest

Authors declare there are no conflicts of interest.

## References

[1] Fitzer C, Barnes M, Green P. Voltage Sag Detection Technique for a Dynamic Voltage Restorer. IEEE Trans Ind Applicat. 2004;40:203-212.

[2] Manmadha Rao S, Lakshmi Kumari SVR, Srinivasa Rao B. Compensation of Unbalanced Sags/ Swells by Single Phase Dynamic Voltage Restorer. International Electrical Engineering Journal. 2015;6:1743-1748.

[3] Woodley NH, Morgan L, Sundaram A. Experience with an inverter based dynamic voltage restore. IEEE Trans Power Deliv. 1999;14(3):549-557.

[4] Mishra SK, Mangaraj M. Dynamic Voltage Restorer incorporating dqo Transformation Enhancing Power Quality, International Journal of Computer Applications. 2012;iC3S:19-22.

[5] Vijay Kumar D, Trinadha B, Prameela K. Z-Source Inverter based Dynamic Voltage Restorer for the Mitigation of Voltage Sag /Swell. International Journal of Scientific Engineering and Technology Research. 2015;04:7178-7182.

[6] Peng FZ, Akagi H, Nabae A. Compensation characteristics of the combined system of shunt passive and series active filters. IEEE Trans Ind Applicat. 1993;29:144-151.

[7] Fitzer C, Barnes M, Green P. Voltage Sag Detection for a Dynamic Voltage Restorer. IEEE Trans Power Deliv. 2004;40:203-212.

[8] Boonchiam P, Mithulananthan N. Understanding of Dynamic Voltage Restorer through MATLAB simulation, Thammasat International Journal of Scence and Technology. 2005;11:126-132.

[9] Deepa S, Rajapandian S. Voltage Sag Mitigation Using Dynamic Voltage Restorer System by Modified Z-Source Inverter. International Conference on Electrical, Electronics and Civil Engineering, 2012. pp. 1-4.

[10] Rovai CH, Doorwar A. An overview of various control techniques of DVR. International Conference on Circuit Power and Computing Technologies, 2014. pp. 53-57.

[11] Nicolaescu Gh, Andrei H, Rädulescu D. Dynamic Voltage Restorer Response Analysis for Voltage Sags Mitigation in MV Networks with Secondary Distribution Configuration. Proceedings of the IEEE-EEEIC, 2014. pp. 10-12.

[12] Heine P, Matti L. Voltage Sag Distributions Cause by Power System Fault, IEEE Transsactions on PowerSystems, 2003;18:1367-1373.

[13] Rashid MH. Power Electronics, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1993.

*******

 