

SIMULATION OF FAULT CURRENT LIMITER (FCL) FOR VOLTAGE SAG MITIGATION

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Abstract:-Fault current levels in power grid is approaching, and may eventually exceed, the short-circuit current limits of existing protection devices. Fault Current limiters (FCL) provide more cost-effective solutions to prevent old protection devices and other equipment on the system from being damaged by excessive fault currents. Short circuit faults are often the origin of voltage sags at the point of common coupling (PCC) in a power network, the extent of the voltage sag is proportional to the short circuit current level, reducing the fault current level within the networks can reduce voltage sags during faults and protect sensitive loads that are connected to the same PCC. The proposed structure prevents voltage sag and phase-angle jump of the substation PCC, will have good power quality. In this paper the system implementing FCL is created and simulation in MATLAB SIMULINK. The simulation results show that FCL can limit the fault current effectively.

Keywords - - Fault current limiter (FCL), point of common coupling (PCC), power quality (PQ), semiconductor switch, and voltage sag.

1. INTRODUCTION

A fault is an unintentional short circuit, or partial short-circuit, in an electric circuit. A variety of factors such as lightning, downed power lines, or crossed power lines cause faults. During a fault, excessive current called fault current flows through the electrical system often resulting in a failure of one section of that system by causing a tripped circuit breaker or a blown fuse.

Power quality disturbance can be defined as the deviation of the voltage and the current from its ideal waveform. Faults at either the transmission or distribution level may cause voltage sag or swell in the entire system or a large part of it. Also, under heavy load conditions, a significant voltage drop may occur in the system. Voltage sag and swell can cause sensitive equipment to fail, shutdown and create a large current unbalance. These effects can incur a lot of expense from the customer and cause equipment damage. Power quality problems are becoming more and more important for electric utilities due to growing number of sensitive loads. Among all the problems, voltage sag and momentary outage are the most serious ones faced by industrial and commercial customers.

About 80–90% of customer's displeasure is due to voltage sags that mainly caused by short circuits in distribution network. The distribution network topology is one of the important factors for the determination of the fault current magnitude and voltage sag. In the parallel feeders, which are connected to the Point of Common Coupling (PCC), the downstream faults in one of feeders could result in large fault current flow that might damage the series equipments. This voltage drop can affect other loads on parallel feeders connected to PCC. But, some sensitive loads are expected to continue their parallel operation with utility network without tripping during the fault or momentary outage, in order to avoid frequent and unnecessary disconnection from utility power network. The sensitive loads can be protected from voltage sag by DVR and UPQC. These devices can only compensate the voltage sag of sensitive loads. But they cannot affect the fault current. Since the voltage sag during the fault is proportional to the short circuit current, an effective fault current limiter, connected to the beginning of feeders, not only limits the large fault current but also improves the reliability, stability, and the system power quality.

In recent years, various types of fault current limiter such as, solid state fault current limiter, resonant circuit and SFCL (Superconducting Fault Current Limiter) have been proposed and developed. The main aim of this work is to develop and design a Fault Current Limiter to compensate voltage sags, of three phase three wire distribution systems.

A proposed lossless FCL component should have the following characteristics:

- 1 At normal operation maintained as zero resistance/impedance
- 2 No power loss at fault conditions
- 3 Operated as large impedance way during fault conditions
- 4 Appearance of system impedance during fault is very responsible & quick
- 5 Fast reverse recovery after fault eradication
- 6 Reliable operation
- 8 Low maintenance cost.

2. PROPOSED FCL CONFIGURATIONS & ITS OPERATION

Below fig.1 shows the single line diagram of power system with FCL connected to it [1]. Distribution side of the power system is shown. The FCL is connected in series with the second feeder.

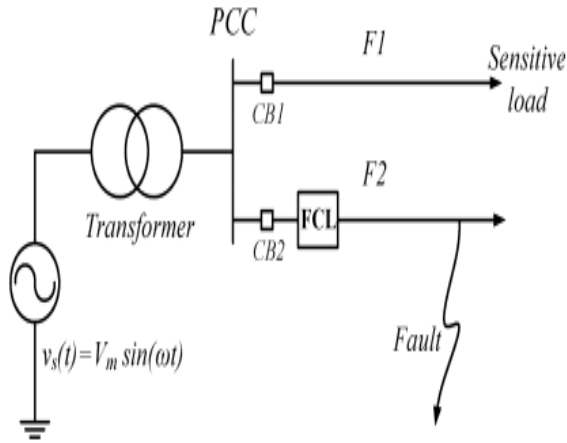


Fig.1 Single line diagram of power system with FCL

Fig. 2 shows the schematic diagram of proposed FCL topology which is comprised based on two following parts:

1 One is bridge part that contains a un-controlled rectifier form in bridge manner with diodes D1, D2, D3, D4 in coordination with small dc limiting reactor (Ldc) with internal resistance (Rdc), a power electronic switch (IGBT or GTO) with a supportive diode for freewheeling action (D5) in parallel with the dc limiting reactor.

2 Another component is shunt branch, acts as a limiter for enhancing the fault currents, it involves a shunt resistor (Rsh) and a shunt inductor (Lsh).

Every diode of the rectifier topology is ON for half period of a cycle. In normal operation, the IGBT switch remains ON and the line current for the positive half cycle passes through D1, Ldc, semiconductor switch and D4. For the negative half cycle, the line current passes through D3, semiconductor switch, Ldc and D2.

As a fault occurs, the line current begins to increase, but the Ldc limits its increasing rate and protects semiconductor switch against severe di/dt at the beginning of the fault occurrences. When the current reaches the maximum permissible fault current Im, control system of the semiconductor switch turns it OFF. So the bridge retreats from feeder and shunt impedance enters to the faulted line and limits fault current. At this moment, the free wheeling is used to provide free route for dc reactor current when the semiconductor switch is off. After fault the semiconductor switch is turned ON again and the proposed FCL returns to the normal state.

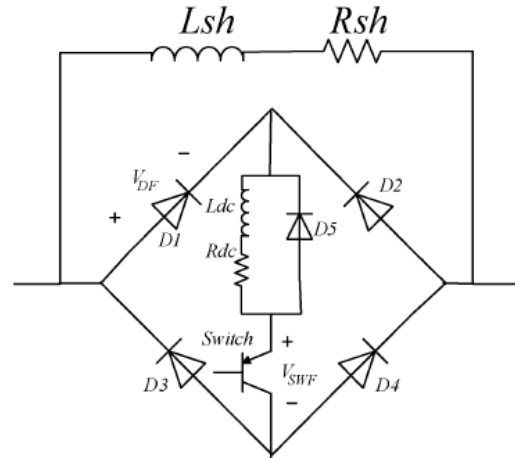


Fig.2 Schematic diagram of proposed FCL topology

For three phase system the FCLs are connected in all three phases separately. The power loss is calculated during the normal operation of the system. Total power losses should include loss FCLs in all the three phases:

$$P_{loss} = P_R + P_D + P_{SW} \tag{1}$$

$$3P_{loss} = 3(P_R + 4 P_D + P_{SW}) \tag{2}$$

Where

‘PR’ power loss in the resistor

‘PD’ power loss in the diode

‘PSW’ power loss in the switch.

Equation (1) shows the power loss in the bridge. Equation (2) shows the power loss in all the three FCLs connected in three phases.

Fault current is given by

$$I_{fault} = V_{pcc} / Z_{sh} \tag{3}$$

Where

‘Vpcc’ is voltage at PCC

‘Zsh’ is shunt impedance

Equation (3) shows the fault current due to the short circuit fault.

System parameters

Power Source	20kV, 50Hz, X/R ratio: 5
Three phase Transformer	20kV/6.6kV, 10MVA
FCL DC Side	Ldc = 0.01H, Rdc = 0.03 Ω Switch type: IGBT
FCL Shunt Branch	Lsh = 0.08H, Rsh = 5 Ω
Sensitive Load	10+j5.7 Ω
Load of F2	15+j31.4 Ω

3. SIMULATION RESULTS

The Fig.3 below is the model of three phase system of distribution side in Matlab. The simulation time is 0.3 sec. The Short circuit fault is created on second feeder. At 0.1 sec the fault occurs in the system and remains in the system for 0.1 sec. The system is without the Fault Current Limiter. The worst condition is considered with LLLG fault on the system to check the performance of the FCL. The fault current becomes very high about 3.6 kA.

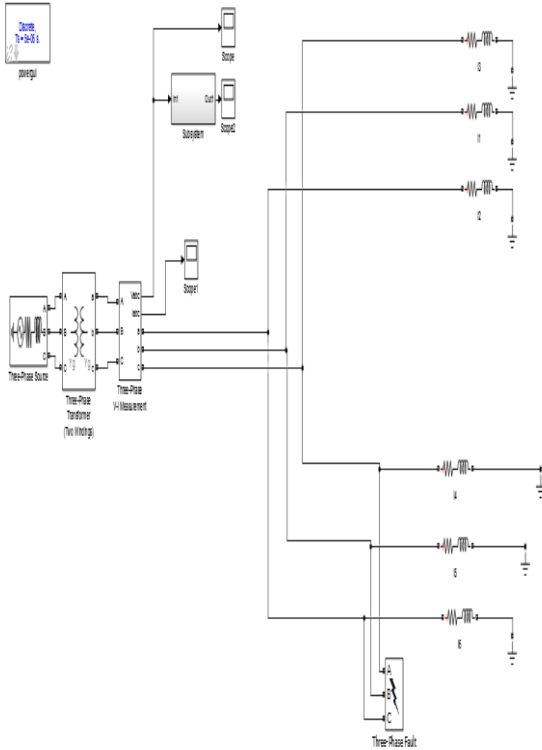


Fig. 3 Simulink Model of system without FCL

The fault due to LLLG fault that occurs at 0.1 sec and exists for 0.1 sec in the system. The fault current increases suddenly. After the 0.2 sec the current comes to its normal level. There occurs voltage sag in the system. The fig.4 shows the voltage dip. It is about 60%.

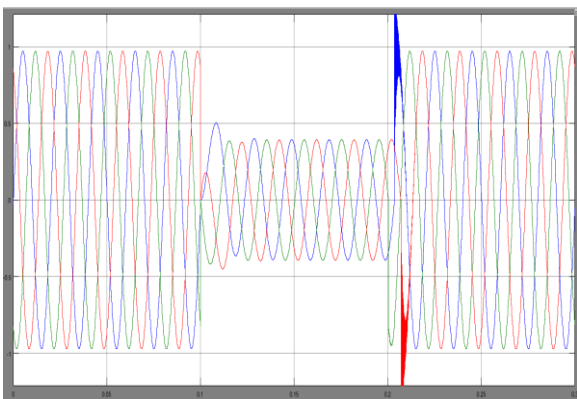


Fig.4 Three phase PCC voltage without FCL

The fig.5 below shows the model of the system connected with the FCL. The FCL is connected in series with the second feeder. The fault current is reduced from its high value to the acceptable level. The fig 6 depicts the waveform of three phase voltage at PCC with FCL. The waveform of three phase voltage at PCC with FCL. There is LLLG fault on the system, from 0.1 to 0.2 sec.

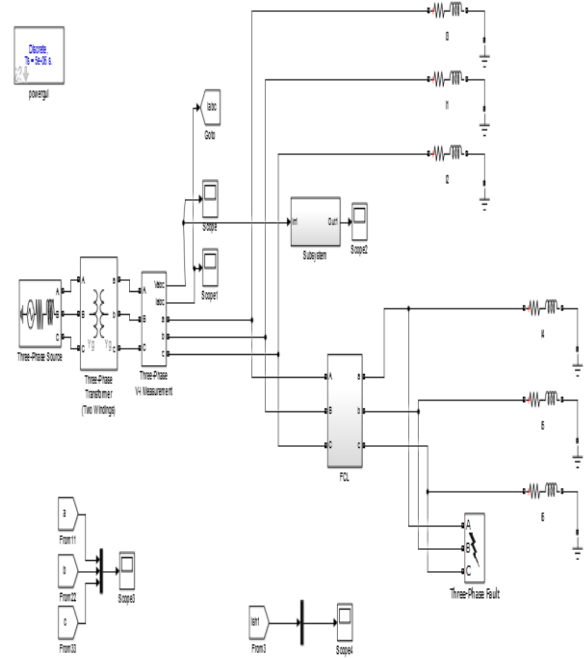


Fig. 5 Simulink Model of system with FCL

The fault current in the system is reduced and the voltage sag is mitigated. The waveform of three phase voltage at PCC with FCL.

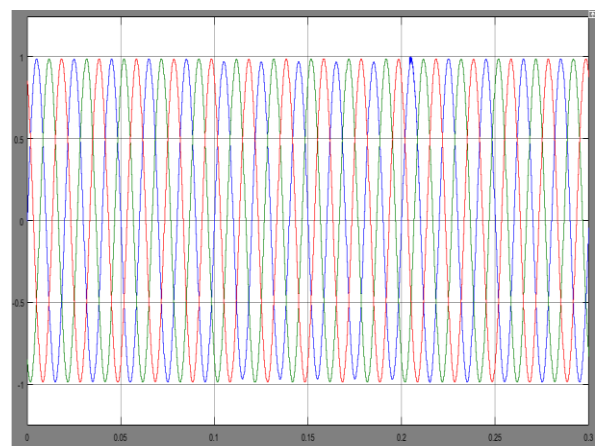


Fig 6 Three-phase PCC voltage for LLLG fault with FCL

4. CONCLUSION

The proposed FCL structure is presented for voltage sag compensation, a mitigation of large valued phase-angle jump and excavating the fault current operation due to the

proposed methodology were evaluated. In this design the diodes will be in conduction just when sag happens thus, in typical condition current directs through the switch by disposing of the diode loss in ordinary working conditions. Moreover, this sort of FCL, with the straight forward control circuit and ease is helpful for the enhancing the voltage-quality during fault conditions.

The models of three phase system without FCL and with FCL are observed by using Matlab /Simulink. When fault occurs on three phase system without FCL, the voltage sag is created at the point of common coupling. The power quality of the system is degraded. When the Fault Current limiter (FCL) is connected in series with the feeder where the fault occurs the voltage is mitigated. The power quality of the system is improve.

5. ACKNOWLEDGMENT

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