DESIGN AND ANALYSIS OF LOW-POWER FULL ADDER USING NOVEL 10-T XOR-XNOR CELL

Dr. K. Kalai Selvi[1], V.Pavithra[2]

[1]*Dean, Department of ECE, SNS college of Technology, Tamil Nadu,India*

[2]*PG Scholar, Department of ECE, SNS College of Technology, Tamil Nadu, India*

Abstract - Now a days, portable electronic gadgets, such as cellular phones, personal digital assistants (PDAs), and notebook, form the integral part of life. These electronic systems mostly comprise arithmetic circuits. An adder is a fundamental component of most of the arithmetic circuits such as multipliers. These arithmetic circuits are extensively used in the data paths consuming almost one-third of power in the high-performance microprocessors. Therefore, enhancing the performance of the adders improves the performance of the whole system significantly. Hybrid logic style is widely used to implement full adder (FA) circuits. Performance of hybrid FA in terms of delay, power, and driving capability is largely dependent on the performance of XOR–XNOR circuit. In this article, a high speed, low-power 10-T XOR–XNOR circuit is proposed, which provides full swing outputs simultaneously with improved delay performance. The performance of the proposed circuit is measured by simulating it Tanner EDA environment.

Keywords: Full voltage swing, Hybrid full adder (FA), XOR–XNOR circuit.

I. INTRODUCTION

For harnessing best out of these electronic systems, designers strive for small size, high speed, and energy-efficient circuits. These electronic systems mostly comprise arithmetic circuits. An adder is a fundamental component of most of the arithmetic circuits such as multipliers. These arithmetic circuits are extensively used in the data paths consuming almost one-third of power in the high-performance microprocessors. Therefore, enhancing the performance of the adders improves the performance of the whole system significantly. To realize a full adder (FA) circuit, several static CMOS logic styles have been presented. These logic styles can be broadly classified into two categories: classical design style and hybrid design style.

Classical Design:

The FA is designed in a single module using MOS transistors. The complementary CMOS (C-CMOS) FA is an example of this approach. This design uses 28-transistors to realize pull-up and pull-down networks of a FA. It provides full swing outputs and robustness against voltage scaling and transistor sizing. The main drawback of this circuit is high input capacitance as each of the input is connected to the gates having at least a pMOS and an nMOS transistor which degrades the speed of the adder.

Hybrid Design:

In hybrid design style, FA structure is divided into three modules as shown in Fig. 1. Module I generates full swing XOR and XNOR outputs of two input signals (A and B) simultaneously. These XOR–XNOR signals must have good driving capabilities as these signals have to drive other two modules. Module II and Module III are the sum and carry circuits which produce the sum and carry outputs (COUT), respectively, using the outputs of Module I and third input signal (CIN). The main advantage of hybrid style is that all the modules can be optimized at the individual level, and the number of transistors can be reduced, which reduces the internal power dissipating nodes.

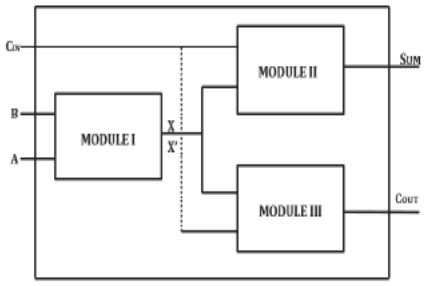

Fig1: Block diagram of hybrid logic FA circuit

II. PROPOSED XOR–XNOR CIRCUIT

The proposed XOR–XNOR circuit using ten transistors (10-T) is shown in Fig. 2.The proposed XOR–XNOR circuit is based on CPL and cross-coupled structure.

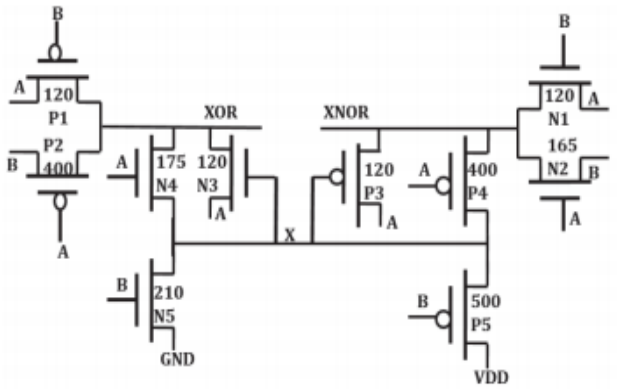

Fig 2: Proposed XOR–XNOR circuit

It uses two pMOS (P1 and P2) and three nMOS (N3, N4, and N5) transistors at the XOR output side and two nMOS (N1 and N2) and three pMOS (P3, P4, and P5) at the XNOR output side. At the XOR side, P1 and P2 are connected in parallel as PTL, N4, and N5 as a restorer to provide a full swing output and N3 as feedback transistor. Similarly, at the XNOR output side N1 and N2 transistors are connected in parallel as PTL, P4, and P5 as a restorer to provide a full swing output and the P3 as a feedback transistor. This circuit provides full swing XOR–XNOR outputs simultaneously. For understanding the operation of the proposed design, charging and discharging paths for XOR and XNOR outputs are shown in Table I.

Inputs AB	Path		Path	
	XOR (Full Swing)	XOR (Partial Swing)	XOR (Full Swing)	XNOR (Partial Swing)
00	N3	P1, P2	P4, P5	-
01	P2	-	N1	P4, P3
10	P1	N4, N3	N2	-
11	N4, N5	-	P3	N1,N2

Table 1: charging and discharging paths for XOR and XNOR outputs

It includes all the paths which provide partial swing and full swing at the output nodes. For the input AB: "01," the transistors P2, N1, and P4 turn on. Transistors P2 and N1 pass logic "1" and logic "0" at XOR and XNOR outputs, respectively, while transistor P4 turns on the transistor P3 to pass the weak logic "0" (-Vthp) at the XNOR output. Similarly, for the input AB: "10," transistors P1, N2, and N4 turn on. Transistors P1 and N2 pass logic "1" and logic "0" at XOR and XNOR outputs, respectively, and transistor N4 turns on the transistor N3 which passes the weak logic "1" (VDD–Vthn) at the XOR output. For these inputs (AB: "01" and "10"), the weak logic outputs will not affect the output swing as paths are available for full swing outputs. For the input AB: "00," the transistors P1, P2, P4, and P5 turn on. P1 and P2 pass weak logic "0" (-Vthp) at the XOR output, while P5 and P4 pass full logic "1" at XNOR output and the internal node X. Logic "1" at node X turns on the transistor N3 and a strong logic "0" is passed at the XOR output to make it full swing. Similarly, for input AB: "11," transistors N1, N2, N4, and N5 turn on. The transistors N1 and N2 pass weak logic "1" (VDD-Vthn) for the XNOR output, while the XOR node discharges completely through N4 and N5. Logic "0" also passes to the internal node X, which causes transistor P3 to be turned on and passes the full logic "1" at the XNOR output.

III. Hybrid Full Adder design

In hybrid logic design style, the FA is designed using XOR–XNOR circuit, sum circuit, and carry circuit. The performance of the FA depends upon all three modules.

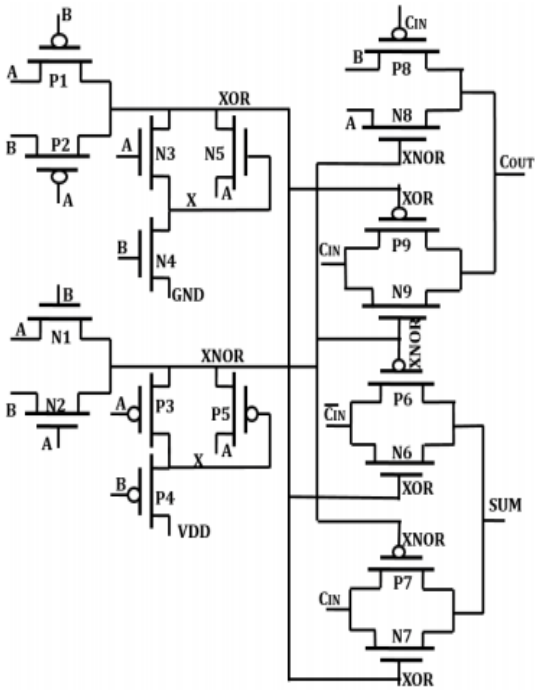

Fig 3: Proposed Full Adder Cell

SUM circuit: It can be implemented by considering CIN and the outputs of XOR–XNOR circuit as input signals. The most important prerequisite of this module is to provide enough driving power to the following gates:

$$\mathrm{SUM} = (A \oplus B) \oplus C'_{\mathrm{IN}} + (A \oplus B)' \oplus C_{\mathrm{IN}}.$$

The SUM circuit is implemented using TG as 2 to 1 multiplexer and employed using four transistors. In this circuit, XOR and XNOR signals are used as the inputs to the gate and CIN and CIN are used as the input to the sources of two TGs. This circuit provides low power consumption and high speed with full output swing.

Carry Circuit: The third module of the FA is a carry circuit (COUT). Output carry of the FA can be calculated using XOR and XNOR outputs of module I and previous carry CIN using (8). In cascading systems, delay of this module affects the overall delay most as the output of this module depends upon the output carry of the previous FA.

$$C_{\mathrm{OUT}} = (A \oplus B)'A + (A \oplus B)C_{\mathrm{IN}}.$$

The hybrid FA cell design (FA) designed using the proposed XOR–XNOR circuit as module I and TG-based module II and module III circuits. It consists of 20 transistors. This circuit gives the full output swing and high robustness; however, it has driving capability problems in the cascaded stages such as ripple carry adder.

IV. SIMULATION RESULTS AND DISCUSSION

The circuits are simulated using Tanner Eda in CMOS process technology. The supply voltage is taken as 5V for the estimation of power and area of the circuits in the real environment.

1). **10T Xor-Xnor Circuit:**

In the XOR–XNOR circuit, only two input A and input B are required which are taken as a pulse input signal. After passing the inputs through two inverters inputs A and B have glitches because of current feed-through effect. Due to this effect when the gate is turned off, charge under the gate moves toward either drain or source sides and distorted output finds out.

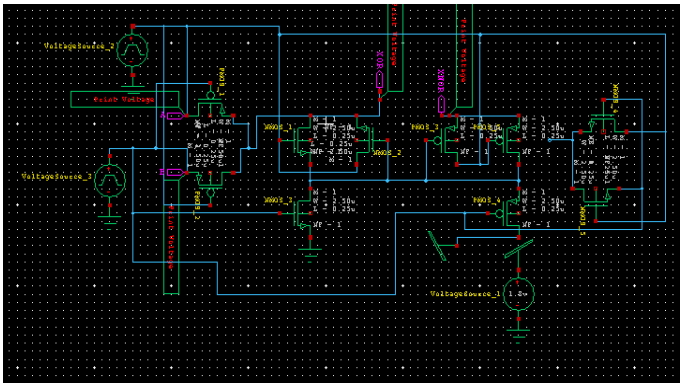

Fig 4: Schematic diagram of 10 T XOR-XNOR Circuit

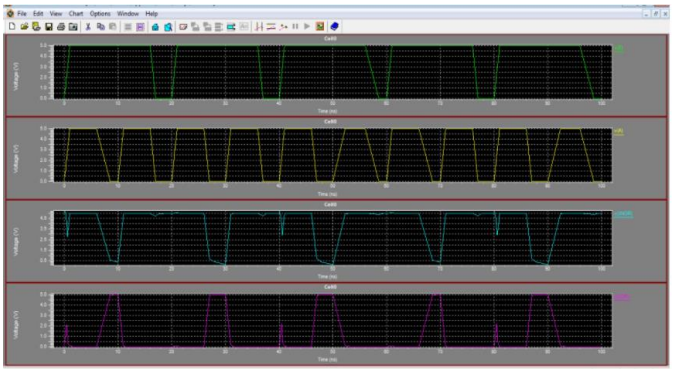

Fig 5: waveform of the 10T XOR-XNOR Circuit

2). **Full Adder Design:**

Existing System:

The existing full adder is designed with 22 transistors.

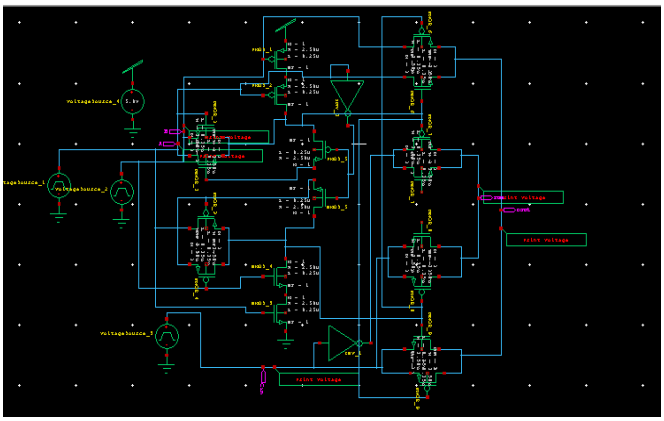

Fig 6: Schematic of FA with 22T Design

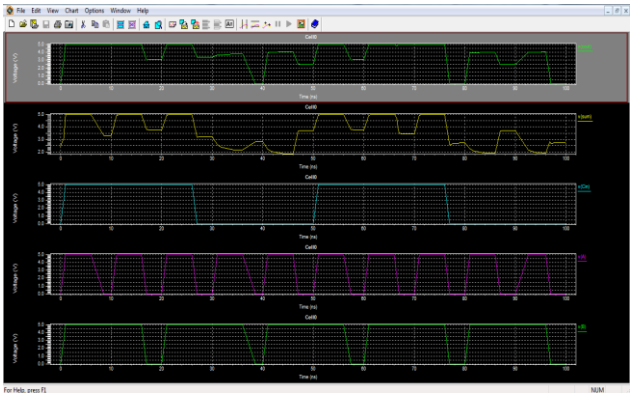

Fig 7: Waveform of FA 22T Design

Proposed System:

The proposed Full Adder is designed with 20 transistors based on 10T Xor-Xnor circuit.

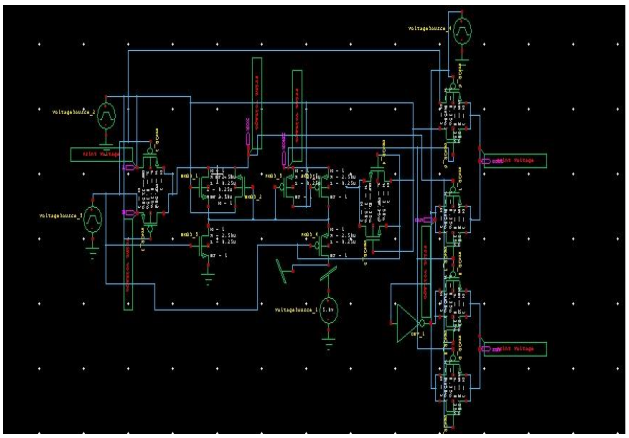

Fig 8: Schematic diagram of proposed FA Design

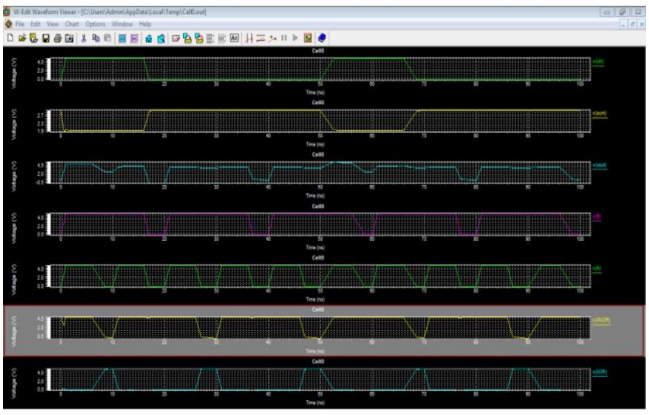

Fig 9: waveform of Proposed FA Design

Table II : Comparison between Proposed and Existing methods

Full Adder	Power	No.of Transistors
Existing	0.38mW	22
Proposed	0.22mW	20

V. CONCLUSION

A new 10-T XOR–XNOR circuit was proposed which provided full swing outputs simultaneously. Using the proposed XOR–XNOR circuit, FA cell based on hybrid logic design style were also proposed. The performance of the proposed XOR–XNOR circuit and the FA cells was tested by simulating them in tanner EDA tool.

VI. REFERENCES

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