18-Mbit (512K x 36) Pipelined SYNC SRAM

Part Number: DPA71370DV2502A

\ The DPA71370DV2502A is a 2.5V, 512K x 36 synchronous-pipelined Burst SRAM with No Bus Latency™ (NoBL™) logic. It is designed to support unlimited true back-to-back read/write operations with no wait states. The DPA71370DV2502A is equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The DPA71370DV2502A is pin compatible and functionally equivalent to ZBT devices.

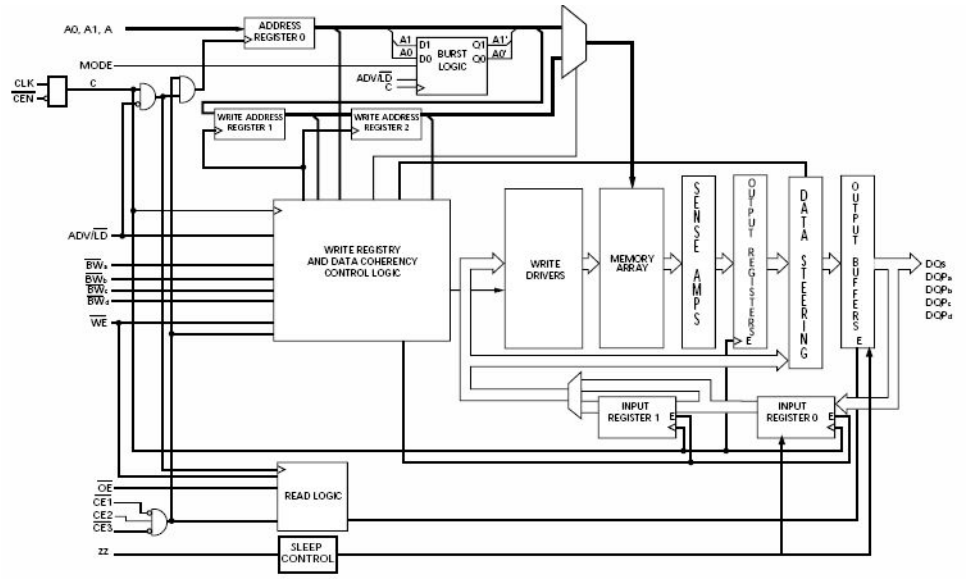
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal which, when deasserted, suspends operation and extends the previous clock cycle.

Write operations are controlled by the byte write selects ($\overline{BW}_A$-$\overline{BW}_D$) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drives are synchronously three-stated during the data portion of a write sequence.

- **-55˚ to +125˚C operating temperature**
- **Hermetically sealed ceramic package**
- **Pin-compatible and functionally equivalent to ZBT™**
- **Supports 250-MHz bus operations with zero wait states**
  - **Available speed grades are 250, 200 and 167 MHz**
- **Internally self-timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$**
- **Fully registered (inputs and outputs) for pipelined operation**
- **Byte Write capability**
- **Single 2.5V core power supply**
- **2.5V I/O power supply**
- **Fast clock-to-output times**
  - **2.6 ns (for 250-MHz device)**
- **Clock Enable ($\overline{CEN}$) pin to suspend operation**
- **Synchronous self-timed writes**
- **IEEE 1149.1 JTAG-Compatible Boundary Scan**
- **Burst capability-linear or interleaved burst order**
- **"ZZ" Sleep mode option and Stop Clock option**
- **This product uses Cypress CY7C1370DV25 die and is tested to meet military and space operational environment requirements.**

Logic Block Diagram



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