# nMOS Short Channel Device Characteristics After Soft Oxide Breakdown and Implications for Reliability Projections and Circuits

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***Abstract*— The currents in all N-channel field effect transistor device terminals can be severely degraded when a soft breakdown event occurs from gate-to-drain. These effects become more pronounced for shorter channel lengths. We present a methodology for separating the effects of mobility degradation and threshold voltage shift on post breakdown device characteristics. Using an accurate equivalent circuit model, we analyze the impact of these parameter shifts on post breakdown circuit performance and the implications for post breakdown reliability projections and circuit design.**

***Index Terms*— Breakdown, dielectric, oxide, reliability, SiON, time-dependent-dielectric-breakdown (TDDB).**

## I. Introduction

As TECHNOLOGY scaling becomes more aggressive, there is an increasing interest in reliability projection methods that extend the time to failure beyond the first soft breakdown (SBD) event [1]–[4]. This activity has been motivated by reports that in some circumstances, circuits remain operative after first SBD [5]–[10]. If the time to failure can be extended beyond first SBD, the corresponding relaxation in reliability requirements can enable higher safe operating voltage.

This paper focuses on dielectric breakdown from gate-to-drain because the degradation can be severe [11], even for SBD as shown in Fig. 1(a). For this device, the linear region drain current ($I_{\mathrm{DLIN}}$) changes polarity (from positive to negative) after SBD. This means that the post breakdown conductance between gate and drain has become sufficiently high that the net electron flow resulting in drain current is no longer from source-to-channel-to-drain, but is rather due to electrons entering the drain from the external circuit and flowing out the gate contact as shown in Fig. 1(b). In circuits, gate-to-drain breakdown is more problematic than from gate-to-body since an input/output node failure is more probable.

Much of the understanding of the effects of breakdown on circuits has been obtained from simulation program with integrated circuit emphasis (SPICE) modeling. To use this tool, an equivalent circuit is needed to replicate post breakdown $I$–$V$ characteristics. For gate-to-drain breakdown, equivalent circuits employing components solely between gate and drain terminals are typically utilized [5], [6], [8], [12]–[15]. However, it was recently shown that these models can underestimate device degradation in state-of-the-art technologies because a significant coupling between drain and source arises after SBD [11]. Indeed, degradation in both drain and source currents is still observed when $V_D = V_G$ [11] as shown in Fig. 2. Some possible explanations for the drain to source coupling could be materials in the gate-stack and/or source/drain regions being introduced into the channel during the breakdown transient [16], or due to the channel length becoming on the order of the size of the breakdown path [17]. An equivalent circuit model that accurately reproduces all post gate-to-drain SBD terminal currents has been developed [11].

The effect of device dimensions on post SBD degradation is an important concern. It has been shown that as the device width ($W$) is scaled down so that it approaches the size of the breakdown spot, transistor characteristics become severely degraded [18]. As the channel length ($L$) approaches the size of the breakdown spot, degradation of post SBD transistor characteristics might also become increasingly severe due to stronger drain to source coupling. The change in $V_{\mathrm{TLIN}}$ after gate-to-drain SBD for two different channel lengths is shown

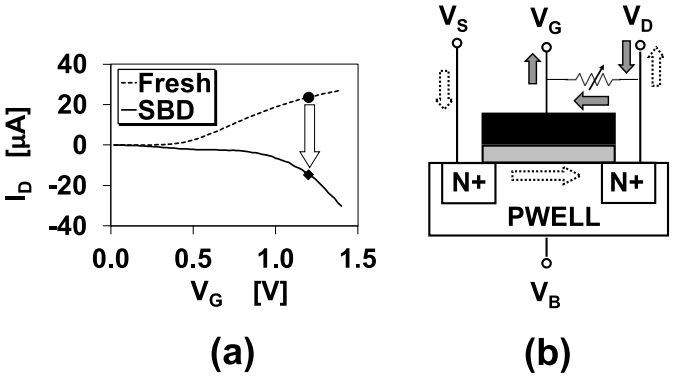


Fig. 1. (a) $I_D$ versus $V_G$ at $V_D = 0.05$ V before and after gate-to-drain SBD. The post SBD $R_{\mathrm{EFF}}$ is 50 KΩ. The degradation is so severe that $I_{\mathrm{DLIN}}$ (symbols) changes sign. (b) Electron flow resulting in $+I_D$ for a fresh device (open arrows) and $-I_D$ after SBD (gray arrows). After Nicollian *et al.* [11].

Manuscript received September 9, 2013; accepted November 18, 2013. Date of current version December 20, 2013. This work was supported by Texas Instruments Inc. The review of this paper was arranged by Editor B. Kaczer.

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Digital Object Identifier 10.1109/TED.2013.2292551

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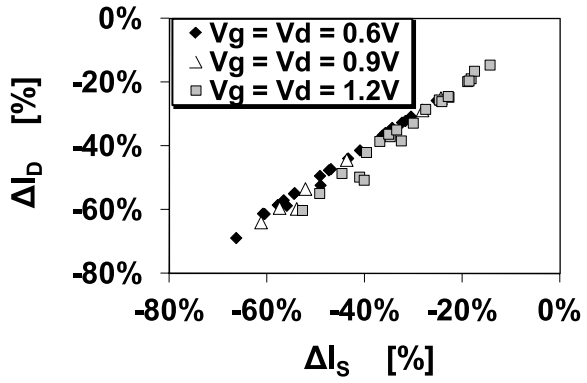


Fig. 2. $\Delta I_D$ versus $\Delta I_S$ for $V_G = V_D$. Despite there being no potential difference between the gate and the drain, significant degradation in both $I_S$ and $I_D$ are observed, with $\Delta I_D = \Delta I_S$. After Nicollian *et al.* [11].

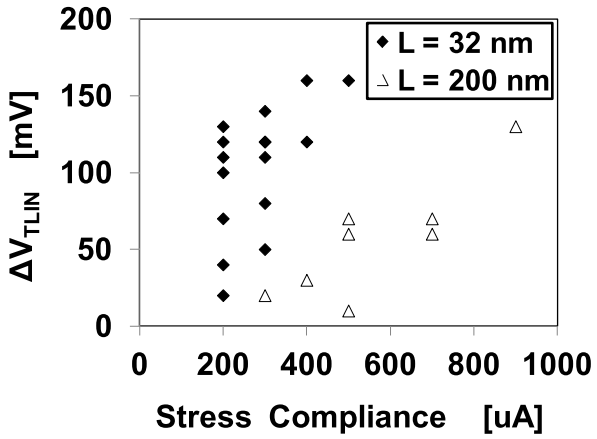


Fig. 3. $\Delta V_{\mathrm{TLIN}}$ versus stress compliance comparing 32 nm and 200 nm drawn channel length devices with the same $W$. At a given compliance, the $\Delta V_T$ resulting from gate-to-drain SBD is larger for shorter $L$.

in Fig. 3. It can be seen that at a given stress compliance, $\Delta V_{\mathrm{TLIN}}$ is significantly larger for shorter $L$.

Using the equivalent circuit model in [11], SPICE simulations show that post SBD resistance ($R_{\mathrm{EFF}}$) and $V_T$ play a complex role in determining post breakdown functionality [10]. Consequently, post breakdown reliability projections that invoke only gate current could be, in some cases, overly optimistic and in light of Fig. 3, may become even more so as $L$ is further scaled. Accordingly, the understanding of post breakdown degradation for short channel devices and the implications on circuits warrant further analysis.

In this paper, we show how to separate the channel characteristics from the gate current after SBD where the degradation has resulted in $-I_D$ as shown in Fig. 1(a). We present a method for resolving the effects of mobility degradation and $V_T$ shift on post SBD $I_D$. Using an accurate equivalent circuit model [11], we analyze the impact of SBD in short channel devices on circuit functionality, implications for post breakdown reliability projections, and circuit design.

## II. Experiment

nMOS devices with polysilicon gate electrodes and 1.4 nm EOT SiON gate dielectrics are subjected to constant voltage

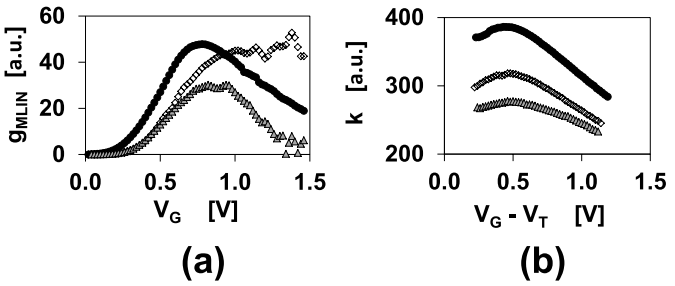


Fig. 4. Fresh and post SBD characteristics for an $L = 32$ nm device with $R_{\mathrm{EFF}} = 31$ KΩ. Solid circles: fresh device. Open diamonds: gate-to-drain breakdown. Gray triangles: gate-to-source breakdown. (a) Linear region $g_{\mathrm{MLIN}}$, $V_D = 0.05$ V. $g_{\mathrm{MLIN}}$ ($I_S$) and $g_{\mathrm{MLIN}}$ ($I_D$) are measured for gate-to-drain and gate-to-source SBD respectively. (b) Instantaneous value of saturation region $k$ at $V_G = V_D$, where $k = I_{\mathrm{DSAT}}/(V_G - V_T)^n$ measured at each $V_G$.

stress at 378 K until a preset compliance is reached. The compliance is varied from $2 \times 10^{-4}$ to $9 \times 10^{-4}$ A to obtain a distribution of post breakdown degradation. The currents in the lower portion of this range are of particular interest since they will occur in multifinger devices that are commonly used in logic circuits to reduce area and capacitance [19] and increase robustness to dielectric breakdown [9], [10]. We define that HBD has occurred when the slope of a log $I_G$ versus log $V_G$ curve is equal to one. In this paper, only SBD is studied. The drawn transistor W/L's are 200 nm/32 nm (short channel) and 200 nm/200 nm (long channel). The breakdown position $X_{\mathrm{BD}}/L$ is determined using the ratio method [20].

To separate the linear region channel characteristics from the gate current after gate-to-drain SBD, where source to gate coupling will be small, the source current rather than the drain current is measured to determine $V_{\mathrm{TLIN}}$ and $g_{\mathrm{MLIN}}(I_S)$

$$g_{\mathrm{MLIN}}(I_S) = \partial I_S / \partial V_G. \tag{1}$$

For gate-to-drain SBD, the channel characteristics can also be separated from the gate current by setting $V_G = V_D$ so that $I_G$ is negligible. For this method, $I_D$ is measured and is most suitable when gate-to-source coupling is small. For gate-to-source SBD, linear region drain current can still be measured since $I_{\mathrm{DLIN}} > 0$ and the coupling between drain and gate is small. The results from these techniques are shown in Fig. 4.

## III. Device Characterization and Model

We will start with the basic equation for saturation [21] and its differential in (2) and (3) respectively to derive a model for resolving the effects of mobility and $V_T$ degradation on $I_D$

$$I_D = k(V_G - V_T)^n \tag{2}$$

$$\Delta I_D = \Delta[k(V_G - V_T)^n]. \tag{3}$$

To solve this expression, let

$$x = (-V_T / V_G) \tag{4}$$

Then

$$k(V_G - V_T)^n = k V_G^n (1 + x)^n. \tag{5}$$

TABLE I
COMPARISON OF $I_{DSAT}$ POWER LAW EXPONENTS FOR 32 nm CHANNEL LENGTH DEVICES BEFORE AND AFTER SBD

| $R_{EFF}$ [KΩ] | time-0 $I_{DSAT}$ n | post BD $I_{DSAT}$ n |
|---|---|---|
| 46 | 1.75 | 1.87 |
| 31 | 1.86 | 1.96 |
| 27 | 1.74 | 1.76 |
| 15 | 1.63 | 1.71 |
| 12 | 1.83 | 1.82 |
| 9 | 1.63 | 1.94 |

Written in this form, (5) is a binomial series. Inserting (5) into (3) and as an example, expanding the series to third order and partitioning the solution into two terms, where one describes the contribution from the reduction in mobility $(\Delta I_D/I_D)_{\Delta\mu}$ and the other from the increase in threshold voltage $(\Delta I_D/I_D)_{\Delta \mathrm{VT}}$

$$\Delta I_D/I_D = (\Delta I_D/I_D)_{\Delta\mu} + (\Delta I_D/I_D)_{\Delta V_T} \tag{6}$$

$$\begin{aligned}(\Delta I_D/I_D)_{\Delta\mu} = {} & (\Delta k/k)(V_G^n - nV_G^{n-1}V_T \\ & + \frac{1}{2}n(n-1)V_G^{n-2}V_T^2 \\ & - \frac{1}{6}n(n-1)(n-2)V_G^{n-3}V_T^3)/(V_G - V_T)^n \end{aligned} \tag{7}$$

$$\begin{aligned}(\Delta I_D/I_D)_{\Delta V_T} = {} & \big(-nV_G^{n-1}\Delta V_T + \frac{1}{2}n(n-1)V_G^{n-2}\Delta(V_T^2) \\ & - \frac{1}{6}n(n-1)(n-2)V_G^{n-3}\Delta(V_T^3)\big)/(V_G - V_T)^n \end{aligned} \tag{8}$$

where in (8)

$$\Delta(V_T^2) = 2V_T\Delta V_T \tag{9}$$

$$\Delta(V_T^3) = 3V_T^2\Delta V_T. \tag{10}$$

For strong inversion, $(V_T/V_G) < 1$, so (6) is a converging series. If $n$ is an integer, the series is finite and in the long channel limit $n = 2$, for any order expansion (6) has an exact solution

$$\Delta I_D/I_D = (\Delta k/k) - 2\Delta V_T/(V_G - V_T). \tag{11}$$

In (11), the mobility degradation component $(\Delta I_D/I_D)_{\Delta\mu} = (\Delta k/k)$ and the $V_T$ shift component $(\Delta I_D/I_D)_{\Delta \mathrm{VT}} = 2\Delta V_T/(V_G - V_T)$. For non-integer $n$, where $1 < n < 2$, for high order expansions the solution to (6) can be approximated as

$$\Delta I_D/I_D \cong (\Delta k/k) - n\Delta V_T/(V_G - V_T). \tag{12}$$

The parameters in (7), (8), (11), and (12), measured at $V_D = V_G$, are

$$n = \partial \ln I_{\mathrm{DSAT}}/\partial \ln(V_G - V_{\mathrm{TSAT}}) \tag{13}$$

$$k = I_{\mathrm{DSAT}}/(V_G - V_{\mathrm{TSAT}})^n \tag{14}$$

$$\Delta k/k = (k(\mathrm{BD}) - k(0))/k(0). \tag{15}$$

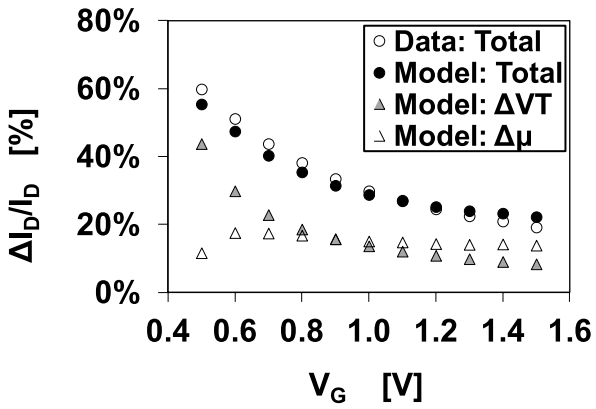


Fig. 5. $\Delta I_D/I_D$ versus $V_G$ with $V_G = V_D$ for an $L = 32$ nm device with $R_{\mathrm{EFF}} = 31$ KΩ. For the total degradation (circles), the model is an excellent fit to data. The absolute contributions (triangles) of $\Delta\mu$ and $\Delta V_T$ are calculated from (7) and (8). The largest absolute component of $\Delta I_D/I_D$ is the $V_T$ shift.

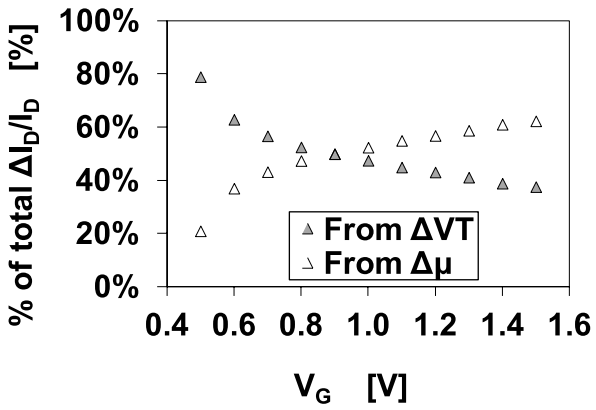


Fig. 6. Relative contribution (percentage of net degradation) of $\Delta V_T$ and $\Delta\mu$ to $\Delta I_D/I_D$ for the device in Fig. 5. $\Delta V_T$ is largest percentage contribution at low $V_G$ while $\Delta\mu$ comprises the largest percentage of degradation at high $V_G$.

In (12), $n$ is the value after SBD and $V_T = V_{\mathrm{TSAT}}(0)$. In (14), because $k$ varies with $V_G$, it is taken as the instantaneous value at each $V_G$ as in Fig. 4(b). $V_{\mathrm{TSAT}}$ is required at both time 0 and post SBD to evaluate (13) and (14) to determine (15). From (12), post breakdown degradation from the $(\Delta I_D/I_D)_{\Delta \mathrm{VT}}$ component increases with increasing $n$. NBTI has also been observed to be worse for higher $I_D$ power law $n$ [22]. Since $n$ tends to be higher after SBD, in effect, the transistor behaves like a longer channel device after SBD as shown in Table I.

Fig. 5 shows the result from (6) expanded to fourth order for a 32 nm channel length device with $R_{\mathrm{EFF}} = 31$ KΩ. The model is a good match to data, even at lower gate voltages where this binomial expansion is the least accurate. The $\Delta V_T$ component is the largest contribution to the absolute change in $I_D$, which occurs at lower voltages. For this same device, Fig. 6 shows that the relative change in $I_D$ (the percent of the total $I_D$ shift) is dominated by $\Delta V_T$ at lower $V_G$, but $\Delta\mu$ comprises the majority of the degradation at high $V_G$. Since the region where $\Delta I_D/I_D$ is highest is dominated by the $V_T$ shift, we will focus on the impact of this parameter on post SBD circuit performance.

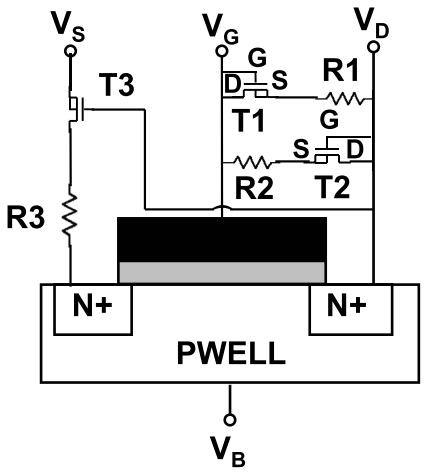


Fig. 7. Equivalent circuit (6 elements) for gate-to-drain SBD. T1 and T2 are depletion mode NFETs operated in saturation to emulate an $I_G$ power law that is polarity symmetric in $V_{GD}$. T3 is operated in the linear mode and couples the source to the drain. Note that there is no component from gate to source. After Nicollian *et al.* [11].

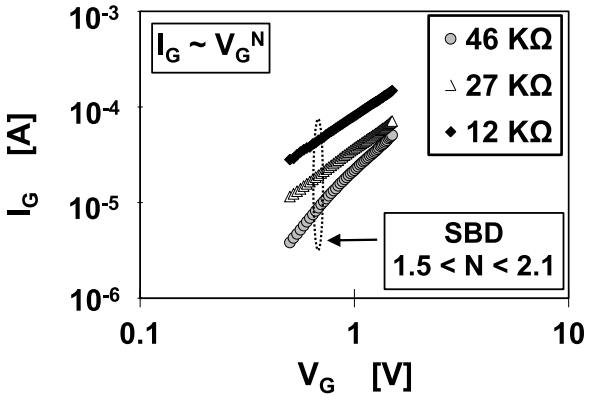


Fig. 8. Post soft breakdown $I_G$ versus $V_G$ at $V_D = 0$ V.

## IV. Circuit Impact

The effects of gate-to-drain SBD on circuit performance for short channel devices will be analyzed through SPICE simulations using the equivalent circuit in Fig. 7, which has been shown to accurately reproduce the terminal currents of actual broken down devices [11]. Post SBD $I_G$ has been proposed to follow a power law in $V_G$ [23], [24]. Our data agree as shown in Fig. 8. Post breakdown $I_G$ has been shown to be polarity symmetric in $V_{GD}$ such that $I_G \sim V_{GD}^N$ with $1 < N < 2$ [11]. This behavior is reproduced by two parallel depletion mode N-channel field effect transistors (NFETs) (T1, T2) operating in saturation between the gate and drain, each with a series resistor (R1, R2). The exponent $N$ can be varied between 1 (short channel velocity saturated limit) and 2 (long channel saturation current limit) by either tuning the channel lengths or by adjusting the saturation velocities of T1 and T2. T3 is operated in the linear mode to provide a voltage controlled resistance that together with R3, models the drain to source coupling.

The range of $R_{EFF}$ and $\Delta V_{TLIN}$ in the 32 nm channel length devices used for circuit simulations is from 7 KΩ to 46 KΩ and 40 mV to 160 mV, respectively. Devices that functionally

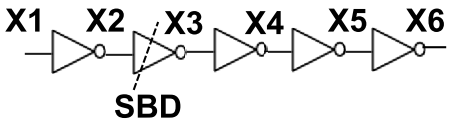


Fig. 9. Circuit with path-depth of 5 used for simulations of post breakdown inverter performance. The NFET device in the second stage has undergone SBD. The delay time is measured from node $X1$ to node $X6$.

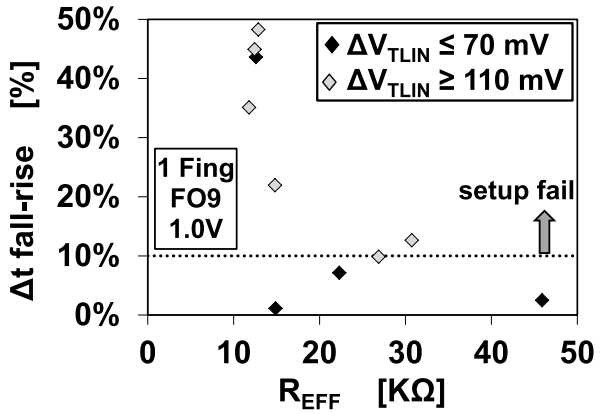


Fig. 10. Change in delay time after SBD versus $R_{EFF}$ for 1 finger devices with a fan-out of 9 operated at 1.0 V. The channel length is 32 nm. The dotted horizontal line represents a failure criteria of 10% increase in setup time.

failed do not appear in plots of timing delays. The circuit used to simulate the effects of SBD on inverter performance is shown in Fig. 9. The path depth = 5, with the switching delay measured from the input of the first stage (node $X1$) to the output of the fifth stage (node $X6$). The effects of multiple device fingers, fan-out, and operating voltage are analyzed. In all cases, only one device finger is broken down.

The reduction in voltage headroom ($V_G$–$V_T$) after SBD can result in setup time failures (where the data transfer is too slow relative to the clock). The SBD NFET is in the second stage, so that $\Delta V_T$ from SBD results in the fall-rise time (odd number nodes falling) being worse than the rise-fall time (odd number nodes rising) for setup fails. If a node floats above 0 V due to SBD, its off–on voltage swing can be reduced and can result in hold time failures (where the data transfer is too fast relative to the clock). Rail-to-rail switching is nearly restored two nodes from the SBD stage, so the results are independent of SBD position for longer path lengths unless it is in the last or second-to-last stage. The failure criteria are defined as a change of +10% for setup time and −10% for hold time.

The change in delay time versus $R_{EFF}$ after SBD for 1 finger devices with fan-out = 9 is shown for $V_{DD} = 1.0$ V in Fig. 10. The change in threshold voltage is grouped into two bins: 1) $\Delta V_{TLIN} \leq 70$ mV and 2) $\Delta V_{TLIN} \geq 110$ mV. All devices with $\Delta V_{TLIN} \geq 110$ mV failed for setup time regardless of $R_{EFF}$. Accordingly, post breakdown reliability projection methods that increase time to breakdown beyond the first SBD event with only $I_G$ as the failure criterion can be overly optimistic. Note that one device with ≤70 mV $\Delta V_{TLIN}$ also failed, underscoring the complex interplay between device parameters and their effects on post SBD circuit functionality.

The effect of fan-out on post SBD delay time at 1.0 V operation is shown in Fig. 11 for (a) fan-out = 9 and

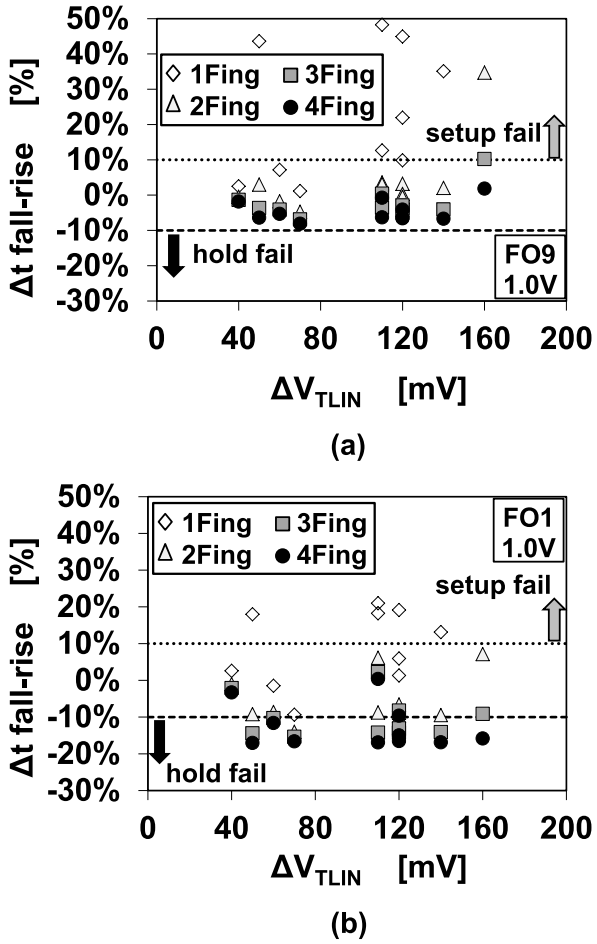


Fig. 11. Change in delay time after SBD versus $\Delta V_{\mathrm{TLIN}}$ at $V_{\mathrm{DD}} = 1.0$ V with finger count as a parameter. (a) Fan-out = 9. (b) Fan-out = 1. The channel length is 32 nm. Above the dotted horizontal line, the failure criteria of 10% increase in setup time is exceeded and below the dashed horizontal line, the failure criteria of 10% reduction in hold time is exceeded. As a guide to the eye, the symbols become darker as the number of fingers increase.

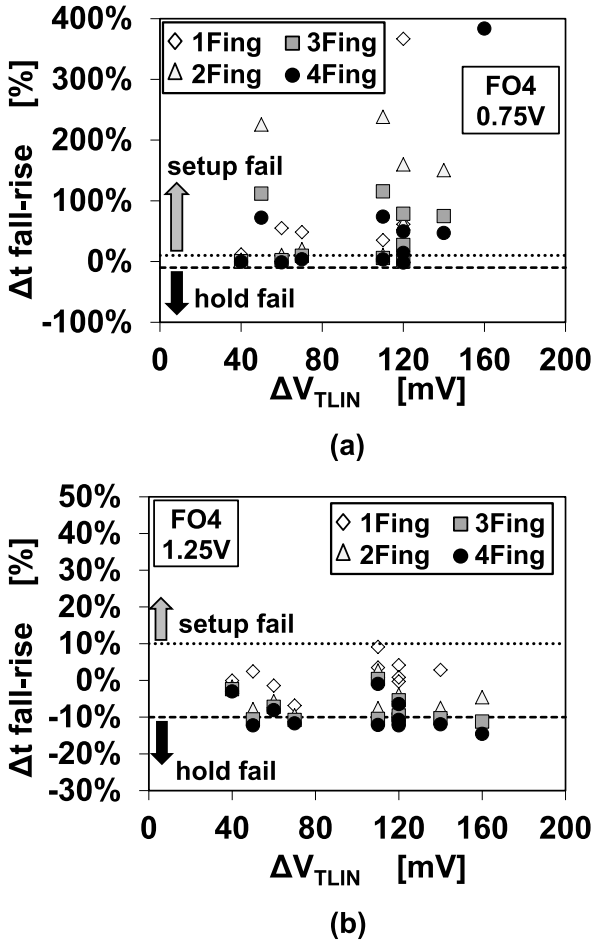


Fig. 12. Change in delay time after SBD versus $\Delta V_{\mathrm{TLIN}}$ for fan-out = 4 with finger count as a parameter. (a) $V_{\mathrm{DD}} = 0.75$ V. (b) $V_{\mathrm{DD}} = 1.25$ V. The channel length is 32 nm. Above the dotted horizontal line, the failure criteria of 10% increase in setup time is exceeded and below the dashed horizontal line, the failure criteria of 10% reduction in hold time is exceeded. As a guide to the eye, the symbols become darker as the number of fingers increase. Note the change in $y$-axis scaling in (a) required by the severe degradation.

(b) fan-out = 1. The effect of heavier loading for fan-out = 9 makes the circuit more susceptible to setup failures, but is improved by increasing the number of device fingers. In contrast, for fan-out = 1, the circuit is more resistant to setup timing violations, but hold time failures arise for multiple fingers.

The effect of operating voltage on post SBD delay time for fan-out = 4 is shown in Fig. 12 for (a) 0.75 V and (b) 1.25 V. Due to lower post SBD head-room, setup time violations are severe for $V_{\mathrm{DD}} = 0.75$ V and the use of multifinger devices is essential. In contrast, 1.25 V operation is robust to setup fails, but multiple fingers introduce hold time violations. From Figs. 11 and 12, the use of multiple finger devices does not, in general, improve circuit robustness to SBD. A possible explanation for getting setup fails in 1-finger devices and hold fails in multifinger devices for the same waveform direction (fall-rise for both cases) is shown in Fig. 13. SBD results in a gate current at node $X2$ that is counterbalanced by the source current in the first stage NFET, resulting in the voltage at $X2$ rising above 0 V. If $\Delta V(X2) < \Delta V_T$, then a setup fail can result due to reduced headroom. However, for multifinger devices, there is no change in headroom for the good devices so with $X2 > 0$ V, the reduced voltage swing (off–on) as $X1$ falls and $X2$ rises could result in hold time fails.

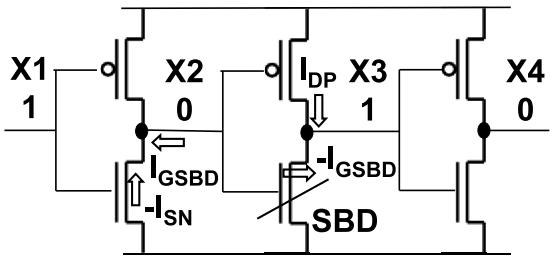


Fig. 13. Beginning of fall-rise cycle. Node $X2$ can float above 0 V due to $I_{\mathrm{SN}}$ counterbalancing $I_G$(SBD). If $\Delta V(X2) < \Delta V_T$, a setup fail can result. For multiple fingers, there is no headroom reduction for the good devices so due to $X2 > 0$, the reduced voltage swing (off–on) as $X1$ falls and $X2$ rises could result in hold time failures.

## V. Conclusion

Post SBD channel characteristics were separated from the gate current where $I_{\mathrm{DLIN}}$ had changed polarity and showed that at a given compliance, the threshold voltage shift after SBD

is more severe for short channel compared to long channel devices. For the first time, we showed that post SBD mobility degradation is significant, but the maximum degradation in channel current is due to the $V_T$ shift. However, additional channel length scaling could lead to an increased role for mobility degradation through stronger post SBD source-drain coupling and merits further investigation.

Using an accurate equivalent circuit model, the effects of SBD on inverter performance were evaluated. For short channel devices, the $V_T$ shift nicely correlates with post SBD circuit performance. Accordingly, post breakdown reliability projection methods that solely use $I_G$ as the failure criteria are incomplete. They are best suited for long channel lengths, low compliance currents, and circuits that are insensitive to $V_T$ shift and mobility degradation.

Our simulations showed that the approach for making circuits more robust to SBD by incorporating multiple device fingers does not appear to be generally applicable. A single finger breakdown in multiple finger devices can still introduce hold time failures.

## ACKNOWLEDGMENT

The authors would like to thank S. Zuhoski, J. Ondrusek, C. Cirba, X. Zhang, S. Krishnan, L. Salmon, and B. McKee for their support of this paper.

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