DESIGN AND IMPLEMENTATION OF ADAPTIVE BUS ENCODING FOR TRANSITION REDUCTION ON OFF-CHIP BUSES

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***Abstract*—** This paper presents an adaptive encoding framework for the reduction of transition activity in high-capacitance off-chip data buses, since power dissipation associated with those buses can be significant for high-speed communication. The technique relies on the observation of data characteristics over fixed window sizes and formation of cluster with bit lines having highly correlated switching patterns. The proposed method utilizes redundancy in space and time to prevent loss of information while retrieving data. We present analytical and experimental analyses, which demonstrate the activity reduction of our encoding scheme for various data. The extra power cost due to the encoder and decoder circuitry along with redundancy is offset due to reduced number of off-chip transitions.

***Keywords*—** *Bus encoding schemes, encoder–decoder architecture, low power VLSI design, off-chip bus.*

I. INTRODUCTION

The increase of speed and complexity of today's designs due to need for increased performance and the demand, there is significant increase in the power consumption of VLSI chips. Power optimization has become a serious concern for achieving high reliability and low packaging cost. A substantial fraction of the total energy consumption comes from system buses [1], [2], because the capacitance associated with an external pin is usually much larger (up to three orders of magnitude) than that of the internal nodes [3], [4]. Therefore, researchers have explored many techniques for minimizing switching activity at external high capacitance off-chip buses at the expense of additional transitions on internal low capacitance nodes. Off-chip bus power minimization can be done by reducing the supply voltage, bus capacitance, or the total number of signal transitions in each bit line. Bus encoding schemes are techniques that reduce the transitional count, which further enhances the energy savings. Several groups utilize spatial redundancy [2], [9] in the form of extra bus lines while others exploit temporal redundancy [5] in the form of excess bit transmission to develop transition reduction encoding mechanism. In majority of applications, it is difficult to know the data characteristics in advance, hence the challenge to encode data bus [2]–[6] is much higher as compared with address bus. Data streams are more random and less sequential in nature than the contents of address buses, so an adaptive encoding technique is highly advisable for data buses.

However, bus encoding techniques used for address bus [5]–[1] can also be used for data bus. The reduction in transition count may be degraded if the switching characteristics vary a lot temporally and spatially. Adaptive encoding techniques take care of these changes to ensure transition count reduction.

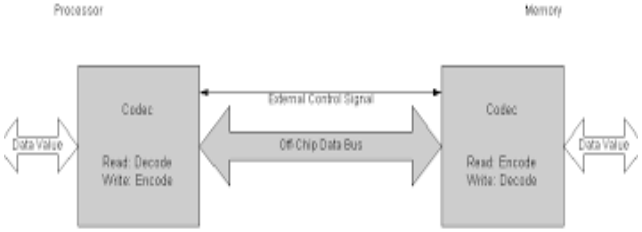

Fig 1.Off Chip Communication/Bus

Objective:

In this paper, we are focusing on reducing transitional activity on data streams whose statistics are not known a priori and switching characteristics change spatially (across the width of the bus) and temporally. We propose an adaptive clustering technique by observing data over time with the aid of spatiotemporal redundancy. In each observation window, we extract local switching statistics and form a subgroup, i.e., a set of bit lines that has highly correlated switching pattern in that observation window.

II. LITERATURE SURVEY

2.1.Dedicated Short-Range Communications (DSRC) Standards in the United States:

The paper shows how these standards fit along to provide a comprehensive answer for DSRC. Most of the key standards are either recently printed or expected to be completed within the returning year. A reader can gain an intensive understanding of DSRC technology for transport communication, together with insights into why specific technical solutions are being adopted, and key challenges remaining for winning DSRC readying. The U.S. Department of Transportation is reaching to decide in 2013 whether to require DSRC instrumentation in new vehicles.

2.2. Design of 5.9 ghz dsrc-based vehicular safety communication:

The automotive trade is moving sharply in the direction of advanced active safety. Dedicated DSRC is a key enabling technology for the next generation of communication-based safety applications. One aspect of vehicular safety communication is the routine broadcast of messages among all equipped vehicles. Therefore, channel congestion control and broadcast performance improvement are of particular concern and want to be addressed in the overall protocol design. Furthermore, the explicit multichannel nature of DSRC necessitates a co-occurring multichannel operational theme for safety and non-safety applications. this text provides an summary of DSRC to handle transport safety communications and proposes a coherent set of protocols to address these necessities.

III. EXISTING METHOD

In the bus-invert coding, if the Hamming distance between the present pattern and the last pattern of the bus exceeds a half of the bus width, the present pattern is transmitted with each bit inverted. This coding scheme is not always efficient. An extra bus line, called invert line, is required to signal to the receiver side whether or not the bus is inverted. For example, if there are some bits whose transition probability is very small, it is clearly inefficient to take those bits into account for the bus-invert coding. Furthermore, we have noticed from experiments that the bus-invert coding is not always an optimum solution even when all bits are almost randomly distributed. In the PBI coding, we partition a bus B into two sub-buses based on the behavior of patterns transferred. More precisely, for a bus B (b0 ,b1 ,...,bn1), which transfers a sequence of patterns(, ,..., n 1), where I is the time index, n is the bus width. We partition B into a selected sub bus S and the remaining sub bus R such that S contains a group of bus lines having higher transition correlation and higher transition probability and R contains the remaining bus lines. Because the bus lines in R have low correlation with those in S and low transition activity, they don't need to be involved in the bus-invert coding. Inverting the lines in R will rather increase the transition activity than decrease it. Therefore, by applying the bus-invert coding only for a sub bus S, we can reduce the hardware for the bus-invert coding as well as increase the gain of the bus-invert coding. Once B is partitioned, the PBI coding is performed as follows:

We compute the Hamming distance between ' i S and i1 S, where ' i *S* is the coded version of i S, including the invert line; if it is larger than | S |/2, set the *invert* line to 1 and invert the lines in i1 S without inverting the lines in i1 R. Otherwise, set invert=0 and let i1 B un inverted. Advantage of the PBI coding is its lower hardware overhead of encoding and decoding logic, which implies less power consumption. Another advantage of the PBI coding comes from the fact that the bits with less transition probability are not inverted in contrast to the bus-invert coding. The gain of the PBI coding is always larger than that of the bus-invert coding. The actual gain of the PBI coding over the bus-invert coding is larger, if we take into account the internal transitions of the encoding/decoding.

IV. PROPOSED METHOD

The proposed approach encodes the data to minimize the self-switching activity before they are introduced into the off-chip bus with the objective of reducing average power dissipation. The main idea is to evaluate the switching statistics for each bit line by observing data stream over an observation window, and to establish the transition correlation among them. The highly correlated bit lines form a cluster, which changes across different observation windows as local switching probability changes. In each observation window, one bit line is designated as a basis line, which has maximum correlated switching transitions with the other lines. The lines which have maximum correlation with the basis are clustered together. In other words, the switching transitions of all the clustered lines of the bus in that particular observation window have maximum projection component along the switching transitions of the selected basis line. When all the clustered lines are XOR-ed with the basis, it leads to maximum switching savings. The clustering information is sent using temporal redundancy between two adjacent windows, while the basis is sent as an extra line as a spatial redundancy.

we will demonstrate possible implementation of the proposed algorithm. Fig. 2 shows basic block diagram of proposed encoding methodology for bus of width N. It consists of decision blocks, delay elements, and set of XOR gates and a multiplexer. Decision block consists of eliminator, cluster formation, and basis selection unit. It generates the control information, corresponding to cluster for each observation window and the multiplexer inserts the temporal redundancy. The sequence of operation in the decision block is shown in Fig. 3. Each element of the row evaluates the savings contribution by each line and decides the presence of bit line in cluster for each observation window. Savings computation unit at the end of each row, which takes the output of bitwise savings computation units, computes overall savings for each bit line if it was chosen as basis. It can be implemented by balanced carry save adder tree. Since basis line is an obvious candidate for cluster and incurs no savings from itself, diagonal section of the matrix contributes no additional hardware cost. Basis selection is nothing but an index selection unit, which compares the overall savings contribution due to selection of each bit line as basis and finally determines the potential basis among all.

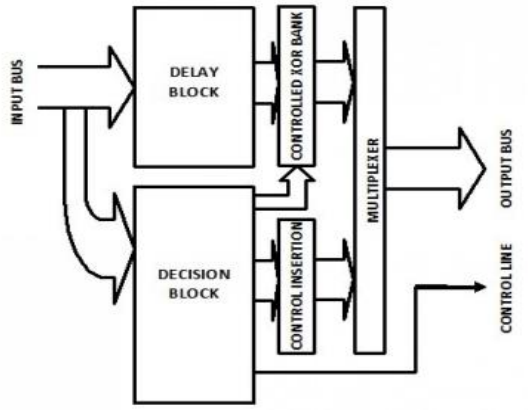

Fig. 2. Block-level encoder architecture of proposed methodology

The overall savings computation unit is an adder stage which takes input from the bitwise savings computation blocks and computes the total switching savings when a particular line is chosen as the basis. The basis selection unit takes the output of all the overall savings computation units and finally selects one of the bit lines as basis . For the logical interpretation of the basis selection unit, consider that t n i represents the nth bit from the left in the N-bit binary representation of the number of switching savings obtained if Fig. 8. Decoder architecture for proposed scheme. ith bit line is chosen as basis. pn i stores the status of the ith line when comparison has been done up to the nth bit from the left, i.e., if pn i = 1, then ith line is still in consideration for being the basis after the most significant n bits have been compared. This has to be repeated for all N bits of the input. The decoder architecture is presented in Fig. 4 which retrieves the data back to its original form. The cluster information is sent as control signal at the beginning of encoded data for every observation window. Before decoding the data, the decoder extracts this cluster information by observing the transition between control signal and encoded data of previous observation window. This information is kept in the register for each bit line until the end of decoding for current window

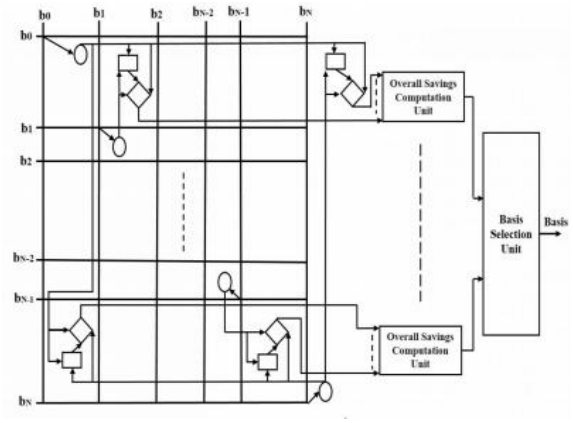

Fig. 3. Decision block, showing bitwise and overall savings computation along with basis selection.

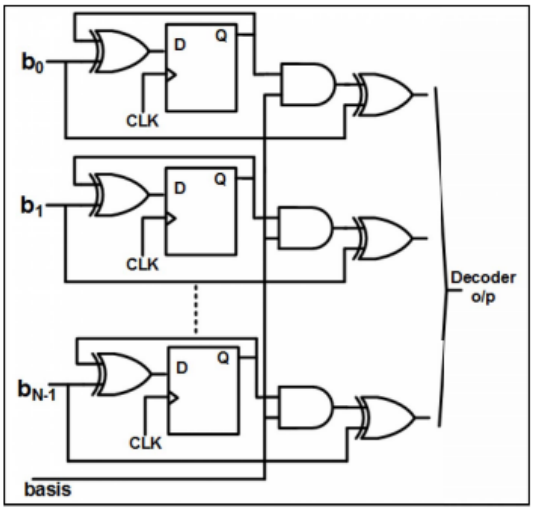

Fig. 4. Decoder architecture for proposed scheme

V. SIMULATION RESULTS

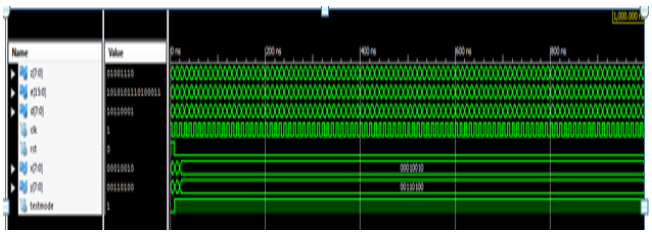

Fig. 5. Simulation waveform

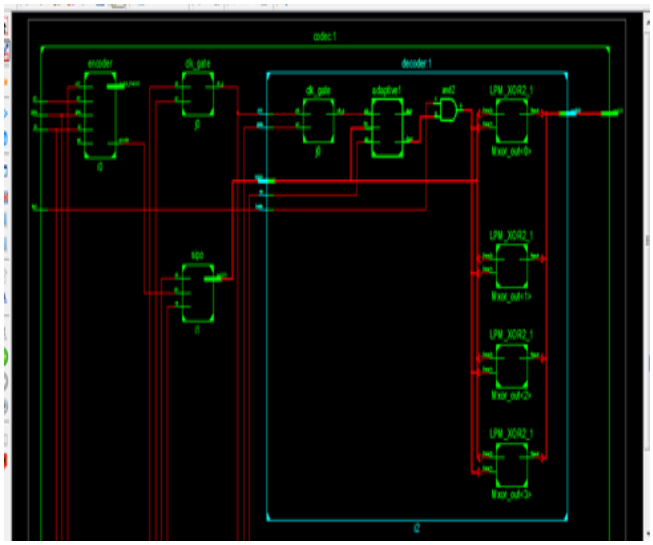

Fig. 6. RTL Schematic

VI.CONCLUSION

The conclusion, a new adaptive bus encoding technique is proposed, which does not require prior knowledge about the signal characteristics. The proposed algorithm selectively encodes a cluster of lines, which have maximum correlated switching transitions within the fixed observation window, by performing XOR operation with a basis bit line, selected based on the switching characteristics of the bit lines in that window. Hence, the clustering is adaptive. The area overhead and the power consumption of the encoder and decoder architectures are studied in Xilinx using 45-nm technology file.

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