Model for the Leakage Instability in Unprogrammed Amorphous Silicon Antifuse Devices

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ABSTRACT

The leakage instability of hydrogenated amorphous silicon (H:a-Si) antifuse devices is one of the important reliability aspects of this new technology, because it determines the standby power for circuit applications. A physical model of the leakage instability is described. After highly accelerated voltage stress, the transport mechanism for the saturated state is shown to be hopping conduction through trap states near the Fermi level. Trap densities on the order of $1x10^{20}$ eV^{-1} cm^{-3} can be induced through stress. This model can be used to facilitate antifuse technology development.

I. INTRODUCTION

An important property of amorphous silicon is that it can be deposited at temperatures below 400°C. Consequently, it is possible to incorporate this material into a process flow after metallization, which allows vertical integration of circuit elements. This feature makes amorphous silicon a desirable material to use as an antifuse device in field programmable gate array (FPGA) applications. To reduce leakage currents, amorphous silicon is hydrogenated in-situ during deposition to passivate dangling bond states [1]. Under high electric field stress, bonds are broken, which can result in several orders of magnitude increase in leakage current [2,3]. This paper describes the physics of the leakage instability, and presents the first quantitative model of the post stress saturated state transport mechanism for devices that have been subjected to highly accelerated voltage stress at electric fields on the order of 1 MV/cm. The model can be used to estimate saturation current as a function of operating voltage.

II. DEVICE FABRICATION

A cross-section of the antifuse device is shown in Figure 1. The bottom metal is deposited on a thick oxide layer. After metal pattern and etch, plasma oxide is deposited and planarized. Following planarization, the interlevel oxide is deposited. The antifuse via is then patterned and plasma etched. An intrinsic H:a-Si film is deposited through plasma decomposition of SiH_4 at temperatures ranging from 200°C to 400°C. Approximately 10 at% hydrogen is incorporated into the H:a-Si film. Top metal is then deposited, followed by a plasma etch of the metal/H:a-Si stack.

III. DEVICE CHARACTERISTICS

Schottky barrier diodes are formed at both top and bottom metal-H:a-Si interfaces shown in Figure 1. The antifuse is a high field device, and the H:a-Si film is fully depleted at small biases [4]. Figure 2 shows that under highly accelerated voltage stress, the leakage current increases in time as a power law, and then saturates. The power law dependence is characteristic of silicon-hydrogen bond breaking, as is known to occur in the Staebler-Wronski (SW) effect [5].

The device is said to be biased VOT when positive voltage is applied to the top metal electrode. VOB bias is the reverse, with positive voltage applied to the bottom metal electrode. The barrier height ϕ of a Schottky barrier is given as [6]

$$\phi = -k \frac{d\ (\ln J_o/T^n)}{d\ (1/T)}, \qquad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, and J_o is the current density extrapolated to zero volts. We have used n = 0 for barrier height calculations on H:a-Si. The effective VOT and VOB barrier heights for conduction are shown for fresh and saturated states in Figure 3. The barrier height is seen to be polarity asymmetric in the fresh state, but is symmetric with a magnitude of 0.1 eV in the saturated state over a range of H:a-Si film thickness. Interface traps alone could not modify the barrier properties in a manner that is consistent with these data. An adequate explanation requires bulk defects throughout the H:a-Si film.

Fresh and saturated device I-V characteristics are shown on a semilog scale in Figure 4. The current is exponentially dependent on voltage in the fresh state, which is not the expected dependence for thermionic emission [7]. This behavior can be due to tunneling from the metal Fermi level to the H:a-Si extended conduction states [8], as illustrated in Figure 5. The current is still exponentially dependent on voltage in the saturated state. Saturated state data are shown in a semilog plot of I/V versus $\sqrt{V}$ in Figure 6. A straight line on this type of plot would indicate Frenkel Poole emission [9], which is frequently encountered in the presence of bulk trap states, but does not agree with saturated state data. Inspection of Figure 4 also eliminates Fowler-

0-7803-2031-X/95/$4.00

Nordheim tunneling [10] and reverse bias generation [7] as possible mechanisms.

The data in Figure 4 are re-plotted on a log-log scale in Figure 7. Below 1 volt, both fresh and saturated states have a slope of 1, which indicates ohmic behavior [7]. A slope of 2 is indicative of space charge limited current transport (SCLC) for both shallow trap and trap free cases [11]. For traps distributed uniformly in energy below the extended conduction states, SCLC is exponentially dependent on voltage [11]. In the next section, we will show that this is not the saturated state transport mechanism.

The temperature dependence of the ohmic conductivity σ is described as [7]

$$\sigma = \sigma_o \exp(-\Delta H/kT), \quad (2)$$

where σ_o is the conductivity pre factor, and ΔH is the activation energy to conduction. σ_o is the conductivity normalized to zero reciprocal temperature, and can be used to help determine transport mechanisms in amorphous semiconductors. In bulk crystalline silicon, charge is transported primarily through valence or conduction band states. In H:a-Si, the equivalent mechanism is called extended state conduction. Since H:a-Si can have a high density of electronic defects, transport can occur through bulk trap states. This is called hopping conduction. The probability of a carrier thermally hopping between trap states in the absence of an electric field is given by [12]

$$p_H = \omega \exp(-2R/R_o - \Delta H/kT), \quad (3)$$

where ω is the phonon frequency, R is the hopping distance, and R_o is the localization distance of a trap state. Hopping probability decreases with increasing spatial and energy separation of trap states. When the trap density and electric field are sufficiently high so that there is no energy separation between nearest neighbor trap sites, the transport mechanism can be nearest neighbor hopping [13]. Otherwise, variable range hopping can occur [13].

The Ohmic conductivities are plotted versus reciprocal temperature for both fresh and saturated states in Figure 8. The y-intercept of this plot yields σ_o. For the fresh state, the experimentally obtained values of σ_o are on the order of 10 $ohm^{-1}\,cm^{-1}$, in reasonable agreement with literature values for conduction in extended states [12]. The conductivity pre-factor is 7 orders of magnitude lower at saturation. As will be shown below, the experimentally obtained values of σ_o in the saturated state are in good agreement with calculated values for nearest neighbor hopping conduction through bulk trap states in the vicinity of the Fermi level.

IV. HOPPING CONDUCTION

As shown in Figures 4 and 7, the I-V characteristics in the saturated state are ohmic at low fields and exponential at high fields. Nearest neighbor hopping conduction is described as [13]

$$J = 2qRkTN_t\,\omega \exp(-2R/R_o - \Delta H/kT) \sinh(qRE/kT), \quad (4)$$

where J is the current density, q is the electron charge, N_t is the trap density, and E is the electric field. Re-writing equation (4) using equation (3) gives

$$J = 2qRkTN_t\,p_H \sinh(qRE/kT). \quad (5)$$

In equation (5), it is seen that an electric field modifies the hopping probability by a factor of sinh(qRE/kT), since the hopping probability is increased by exp(qRE/kT) in the direction of the applied field, and lowered by exp(-qRE/kT) against the field. The term $2kTN_t$ represents the number of electrons per unit volume within an energy range kT of the Fermi energy.

For weak fields, where $qRE \ll kT$, equation (4) reduces to

$$J = 2q^2R^2N_t\omega E \exp(-2R/R_o - \Delta H/kT). \quad (6)$$

Equation (6) shows that hopping conduction results in Ohmic behavior at low fields. Taking the temperature independent part of equation (6), using $\sigma = J/E$, results in the expression for σ_o for nearest neighbor hopping conduction:

$$\sigma_o = 2q^2\,R^2N_t\omega \exp(-2R/R_o). \quad (7)$$

Using commonly used H:a-Si literature values [12,13] $\omega = 1\times10^{13}\ sec^{-1}$, $R_o = 3\times10^{-8}$ cm, and assuming reasonable values of $N_t = 1\times10^{20}\ eV^{-1}\,cm^{-3}$ and $R = 2.5\times10^{-7}$ cm, we get $\sigma_o = 1\times10^{-6}\ ohm^{-1}\,cm^{-1}$, in excellent agreement with experimental results. In contrast, values of σ_o for variable range hopping [13] are on the order of $1\times10^{-13}\ ohm^{-1}\,cm^{-1}$ with these parameters, and do not change significantly for different trap densities.

At high fields, where $qRE \gg kT$, equation (4) becomes

$$J = qRkTN_t\omega \exp(-2R/R_o - \Delta H/kT + qRE/kT). \quad (8)$$

The effect of high fields is to reduce the hopping activation energy. Equation (8) predicts that current is exponential in voltage. The hopping distance R, as determined from the slope of the high field J-V curve using equation (8), is given by:

$$R = kT/q[d\,(\ln J)/d\,E]. \quad (9)$$

We define the energy bandwidth as the approximate range of energies about the Fermi level that hopping occurs. This bandwidth is on the order of ΔH. It is inversely proportional to the both the number of traps per unit volume and energy, and to the volume enclosed by 1 hop. Once R and ΔH have been determined from experimental data, the trap density can be approximated as

$$N_t = 3/4\pi R^3 \Delta H. \quad (10)$$

An activation energy of 0.1 eV (from Figure 3) and a hopping distance of $2.2x10^{-7}$ cm (using Figure 4), yield trap densities on the order of $1x10^{20}$ eV^{-1} cm^{-3}. Saturation trap density versus stress voltage is shown in Figure 9. Inspection of equation (8) shows that if there is to be a realistic probability of observing nearest neighbor hopping, then the electric field must be high enough so that $qRE > \Delta H$. The large trap densities that are generated by highly accelerated stress enable this condition to be fulfilled.

Figure 10 shows that the saturation trap density is independent of H:a-Si film thickness after constant current stress. The SW effect [5] has similar behavior. Constant current stress insures that the electric field and electron fluence during stress are the same for all H:a-Si thicknesses. These conditions are not fulfilled by constant voltage stress. Figure 11 shows that for devices with the same trap density, saturation current is independent of H:a-Si thickness when the current is measured at the same electric field. Inspection of equation (4) shows that this is the expected thickness scaling behavior for hopping conduction. In contrast, SCLC for a uniform trap distribution is given by [11]

$$J = q\mu E n_{co} \exp(\varepsilon\varepsilon_o E/N_t t q k T), \quad (11)$$

where μ is the carrier mobility, n_{co} is the initial equilibrium concentration of thermal carriers, ε is the dielectric constant, ε_o is the permittivity of free space, and t is the semiconductor thickness. Equation (11) shows that at a given trap density and electric field, SCLC decreases with increasing H:a-Si thickness, and should differ by a factor of 4 over the range of film thickness shown in Figure 11. Based on these data, SCLC is ruled out as the transport mechanism in the saturated state, in favor of the hopping conduction mechanism.

Figure 8 showed that the saturated state conductivity pre-factor is 7 orders of magnitude lower than in the fresh state, implying a proportional drop in carrier mobility [12]. Nevertheless, the current is higher in the saturated state. Nearest neighbor hopping conduction through trap states near the Fermi level is illustrated in Figure 12. As shown in Figure 3, the effective barrier height to conduction in the saturated is on the order of 0.1 eV. Since the saturated state conductivity has been shown to be due to a bulk limited mechanism, the injecting barrier height must be < 0.1 eV, compared to 0.7 eV in the fresh state. We hypothesize that the electrons enter the saturated H:a-Si film by tunneling from the metal Fermi level to trap states, instead of extended states as for fresh devices. The tunneling barrier would then represent the energy separation of the Fermi level and unoccupied trap states. The higher current in the saturated state is due to the increased electron supply resulting from the reduction in injection barrier height.

V. RELIABILITY ASSESSMENT

For FPGA circuits, the reliability concern of the leakage instability is excessive standby current. To insure that a quiescent current limit for the product is met at all times, the average current per antifuse must not exceed a specified limit. By measuring the distribution of leakage currents, it has been found that the leakage current is log-normally distributed after stress, with $I_{50\%}$ and σ_{LN} parameters that vary with time. To properly weigh the contribution from the leakiest devices, the leakage distributions are mapped out in linear space:

$$I(z) = \exp[\ln(I_{50\%}) + (z)(\sigma_{LN})], \quad (12)$$

where $I_{50\%}$ and σ_{LN} are the lognormal average and standard deviation respectively of the leakage current distribution, and z is the standard normal variable. Using the standard normal distribution, the average current per antifuse <I> for the distribution described in equation (12) is [14]

$$\langle I \rangle = \exp[\ln(I_{50\%}) + \sigma_{LN}^2/2]. \quad (13)$$

The value of <I> at saturation, $\langle I_{SAT} \rangle$ is plotted versus stress voltage on a semilog scale to obtain the value of $\langle I_{SAT} \rangle$ at operating voltage, as shown in Figure 13. Saturation current increases exponentially with stress voltage. The technology assessed in Figure 13 is reliable for 5.5 V operation.

Figure 14 shows that the relative degradation is dependent on measurement voltage. Consequently, to perform a reliability assessment, the leakage current during stress must be periodically monitored at operating condition. The hopping conduction model can be used to provide estimates for order of magnitude changes in saturation current that might be expected at different operating voltages. Equation (4), along with the data shown in Figure 9 can be used for this purpose. A calculation of saturation current as a function of operating voltage is illustrated in Figure 15. The calculations are in good agreement with experimental data.

VI. SUMMARY AND CONCLUSIONS

We have shown that the saturated state conduction mechanism after highly accelerated stress of H:a-Si antifuse devices is consistent with the creation of high densities of volume generated trap states, which give rise to a dominant hopping conduction mechanism. Trap densities on the order of $1x10^{20}$ eV^{-1} cm^{-3} are found. This model can be used to evaluate the scalability of the leakage instability to any operating voltage.

ACKNOWLEDGMENTS

The authors would like to thank Ping Yang and Rajiv Shah for supporting this work. We would also like to thank Howard Tigelaar, Janet Camp, and Siang Ping Kwok for providing H:a-Si material, and Cathy Chancellor for writing

test software. We appreciate the stimulating discussions held with Ajith Amerasekera, Somnath Nag, Mark Rodder, and Jerry Seitchik.

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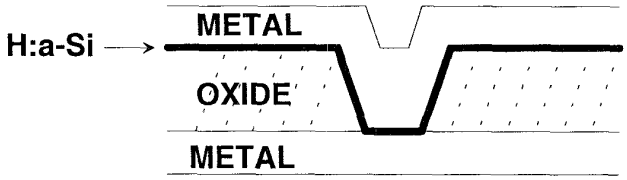

Figure 1. Cross section of antifuse device.

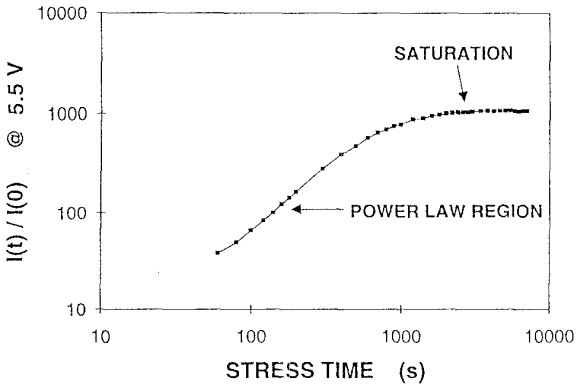

Figure 2. Relative change in leakage current vs. stress time. The device was stressed at 10.4 V VOB, and the current was measured at 5.5 V.

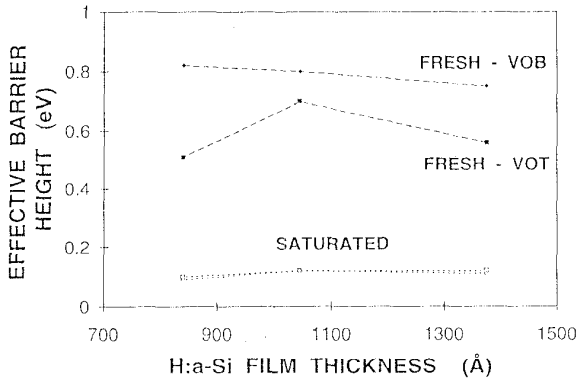

Figure 3. Effective barrier height for conduction in fresh and saturated states. The devices were stressed VOT to saturation.

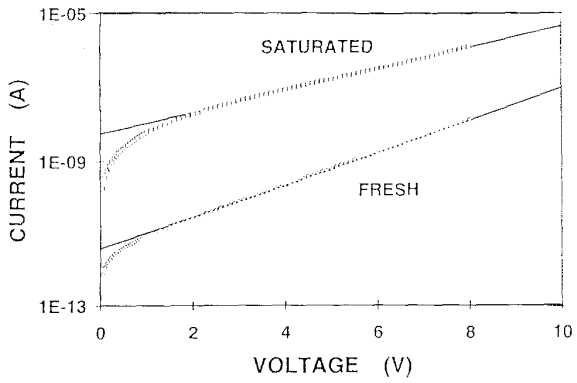

Figure 4. 100°C I-V characteristics on a semilog scale for fresh and saturated states. The solid lines are exponential fits to the data.

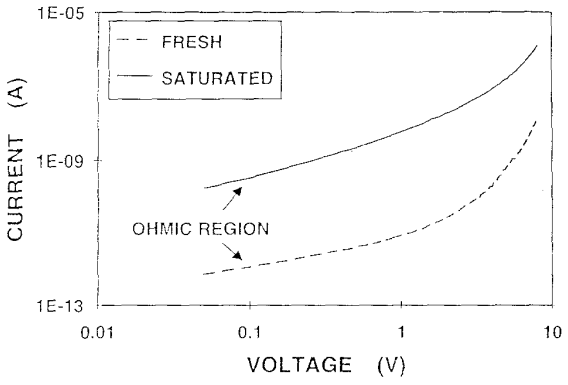

Figure 7. The data from Figure 4 re-plotted on a log-log scale.

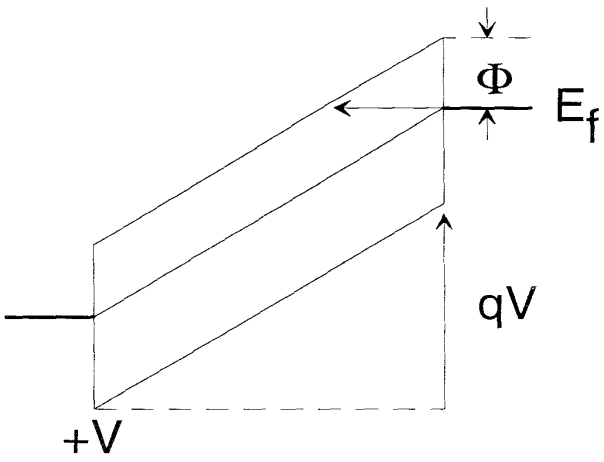

Figure 5. Tunneling from metal Fermi level to H:a-Si extended states. This is the transport mechanism for fresh devices. E_f is the Fermi level, Φ is the barrier height, and V is the applied voltage (after Shannon and Nieuwesteeg, [8]).

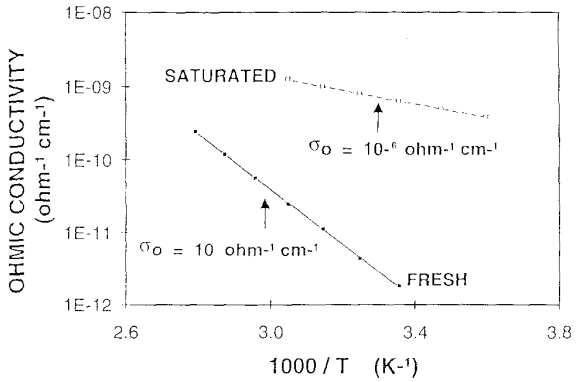

Figure 8. Ohmic conductivity vs. reciprocal absolute temperature for both fresh and saturated states.

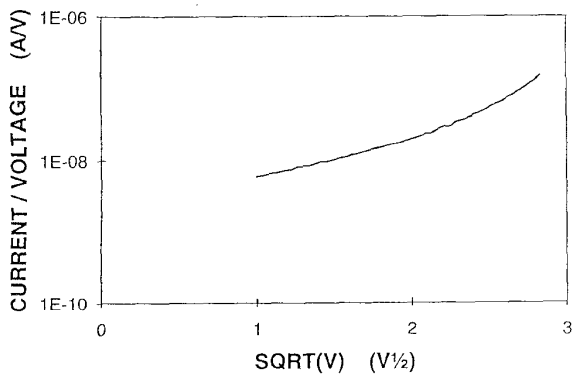

Figure 6. Frenkel-Poole plot, using the saturated state data from Figure 4.

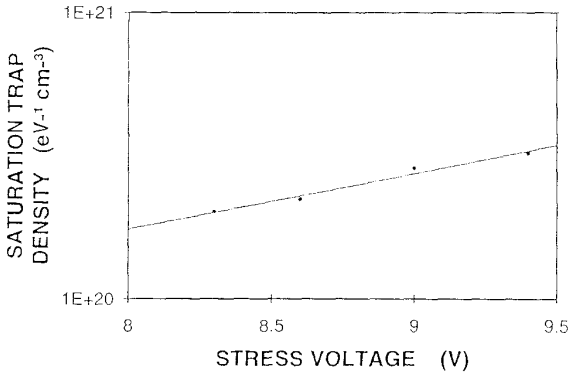

Figure 9. Trap density at saturation vs. electric field.

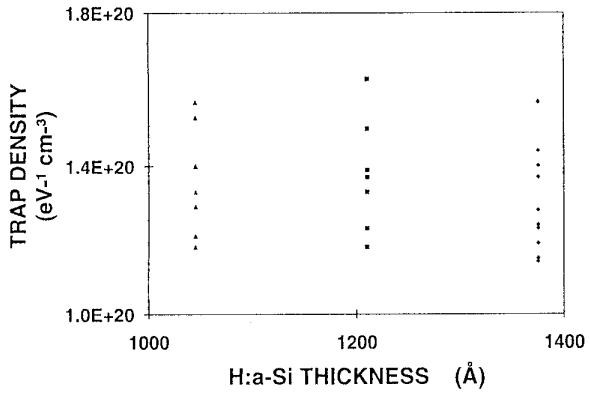

Figure 10. Distribution of saturation trap densities vs. H:a-Si film thickness after 500 nA VOT constant current stress.

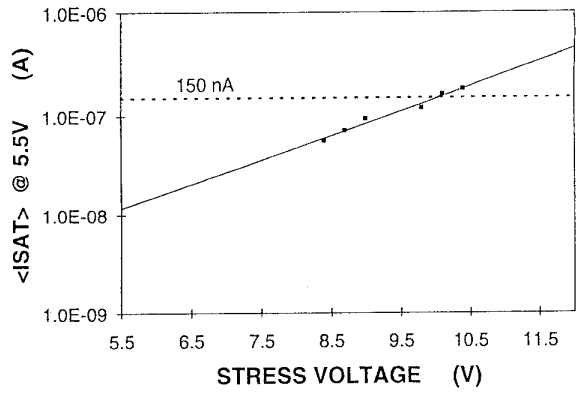

Figure 13. $\langle I_{SAT} \rangle$ vs. stress voltage. The dashed horizontal line denotes the 150 nA average current requirement for the technology illustrated. For all stress conditions, $\langle I_{SAT} \rangle$ was measured at 5.5 V.

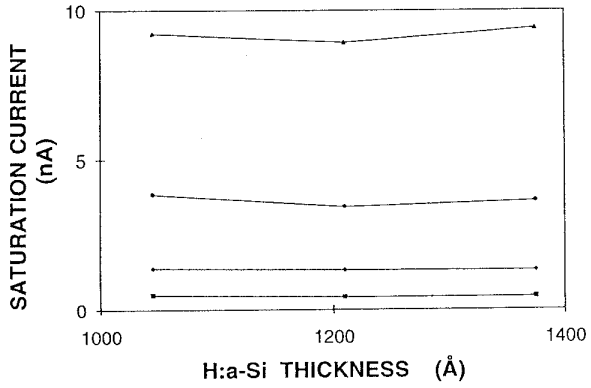

Figure 11. Saturation current vs. H:a-Si thickness after 500 nA constant current stress. The current was measured at electric fields of 0.2 MV/cm (squares), 0.3 MV/cm (diamonds), 0.4 MV/cm (circles), and 0.5 MV/cm (triangles).

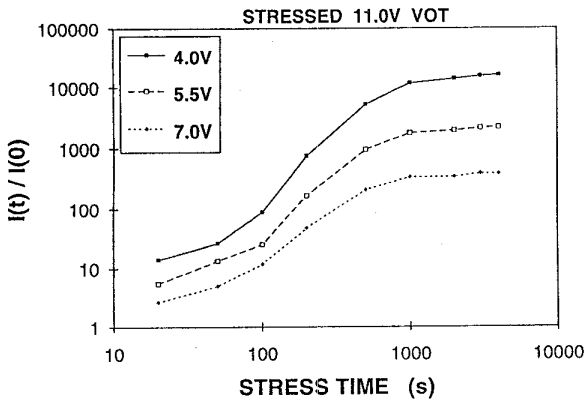

Figure 14. Relative change in leakage current vs. stress time at 3 different measurement voltages. The device was stressed at 11 volts VOT.

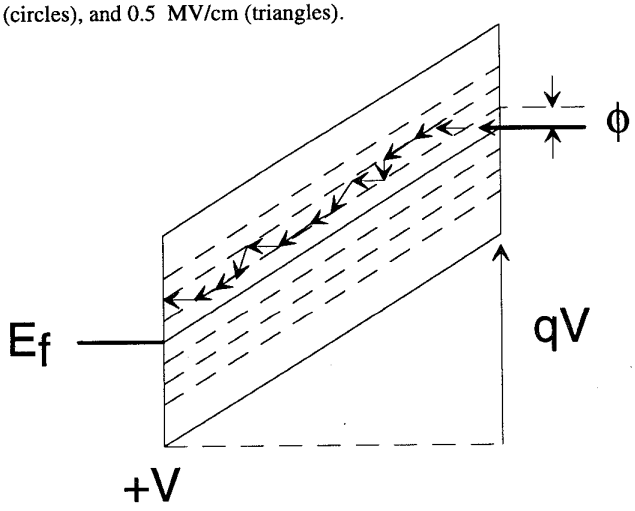

Figure 12. Tunneling from metal Fermi level to trap states in H:a-Si, followed by nearest neighbor hopping conduction in the bulk. This is the model for transport in the saturated state. The dashed lines represent trap states. ϕ is the effective tunneling barrier height.

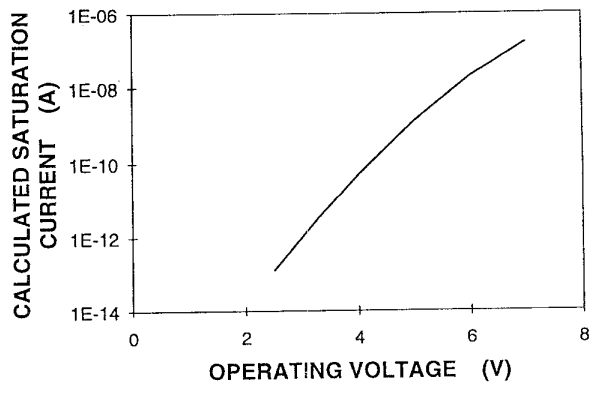

Figure 15. Calculated saturation current vs. operating voltage for the devices used to generate Figure 9.