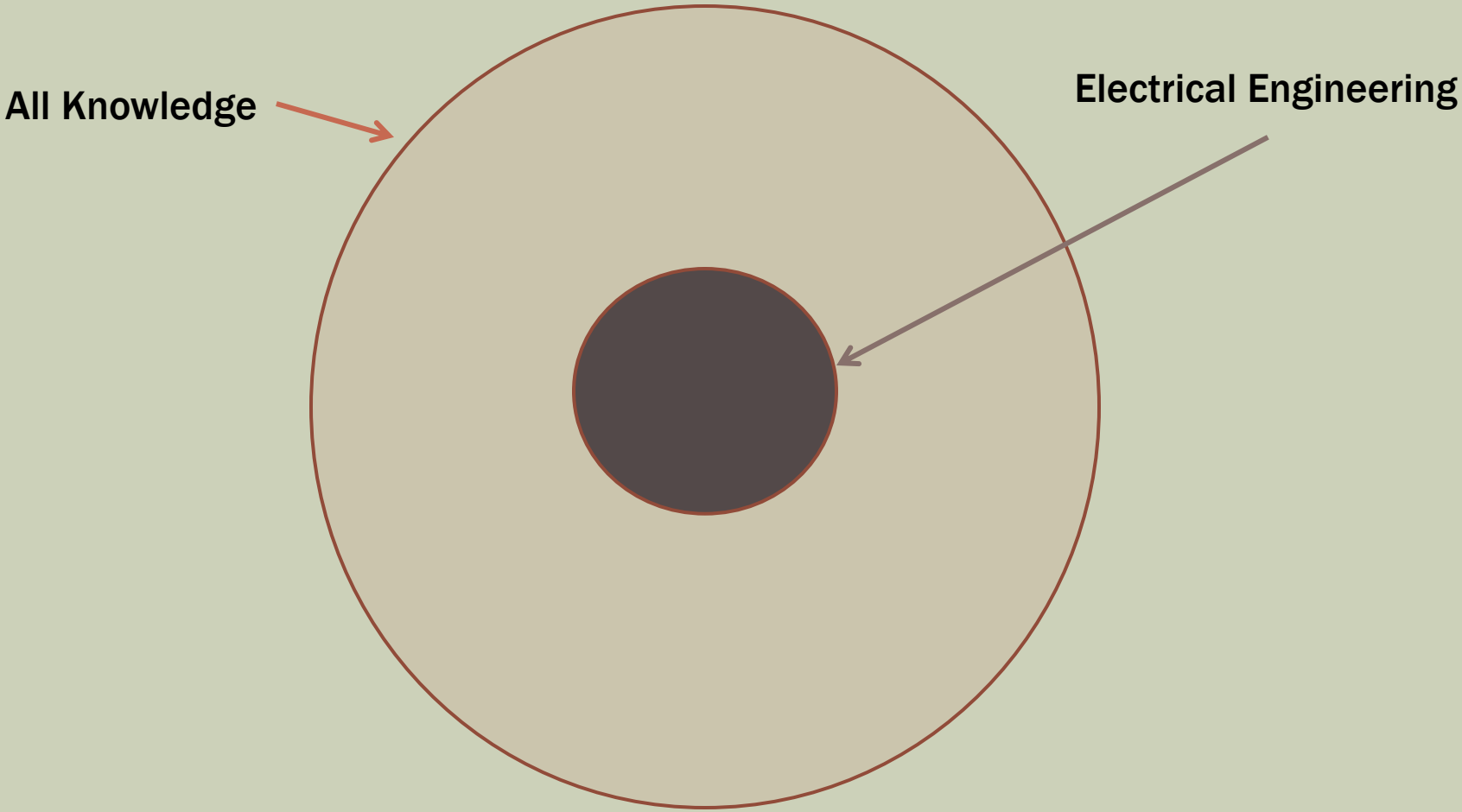
DESIGN, FABRICATION AND TESTING OF MONOLITHIC LOW-POWER PASSIVE SIGMA-DELTA ANALOG-TO DIGITAL-CONVERTERS

by
Angsuman Roy

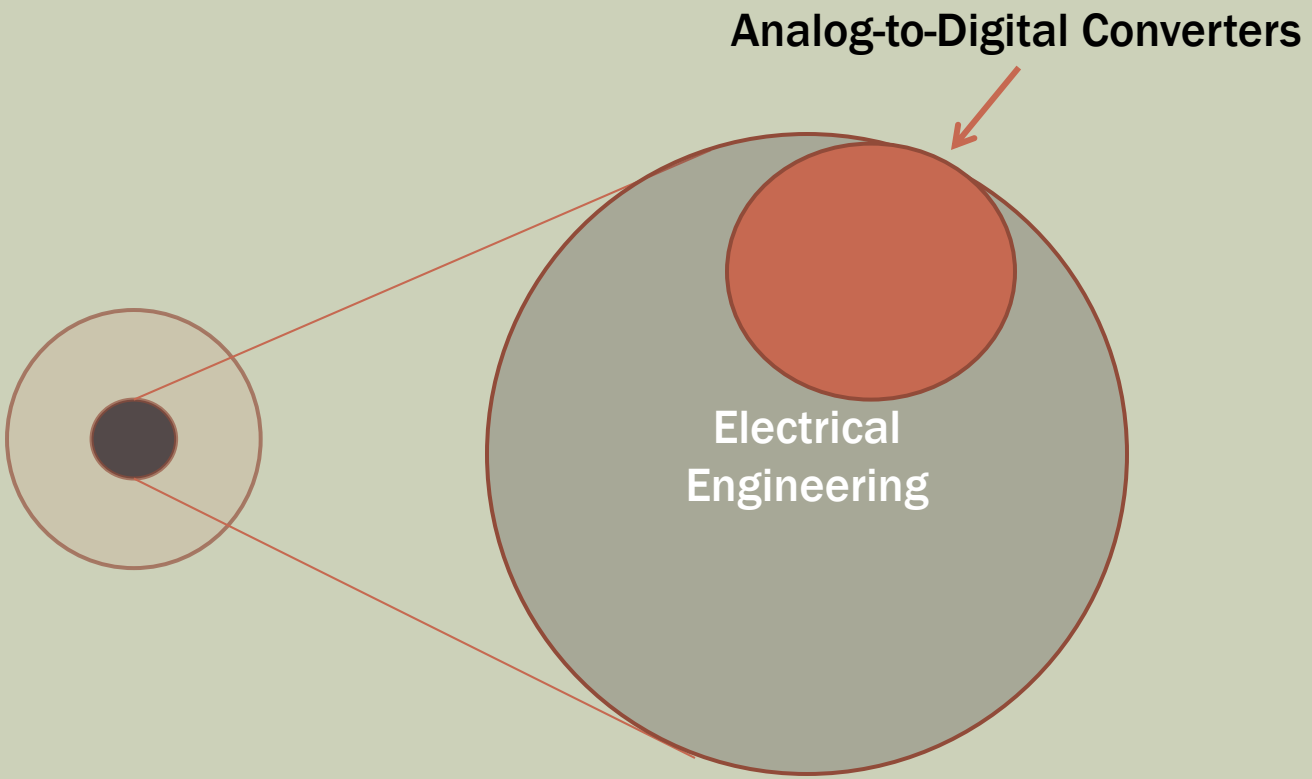
A BRIEF ROADMAP

- Context
- Basic Sigma-Delta ADC Concepts
- Review of Passive Sigma-Delta Topologies
- Proposed Topology
- Continuous-Time IC Implementation
- Switched-Capacitor IC Implementation
- KD1S IC Implementation

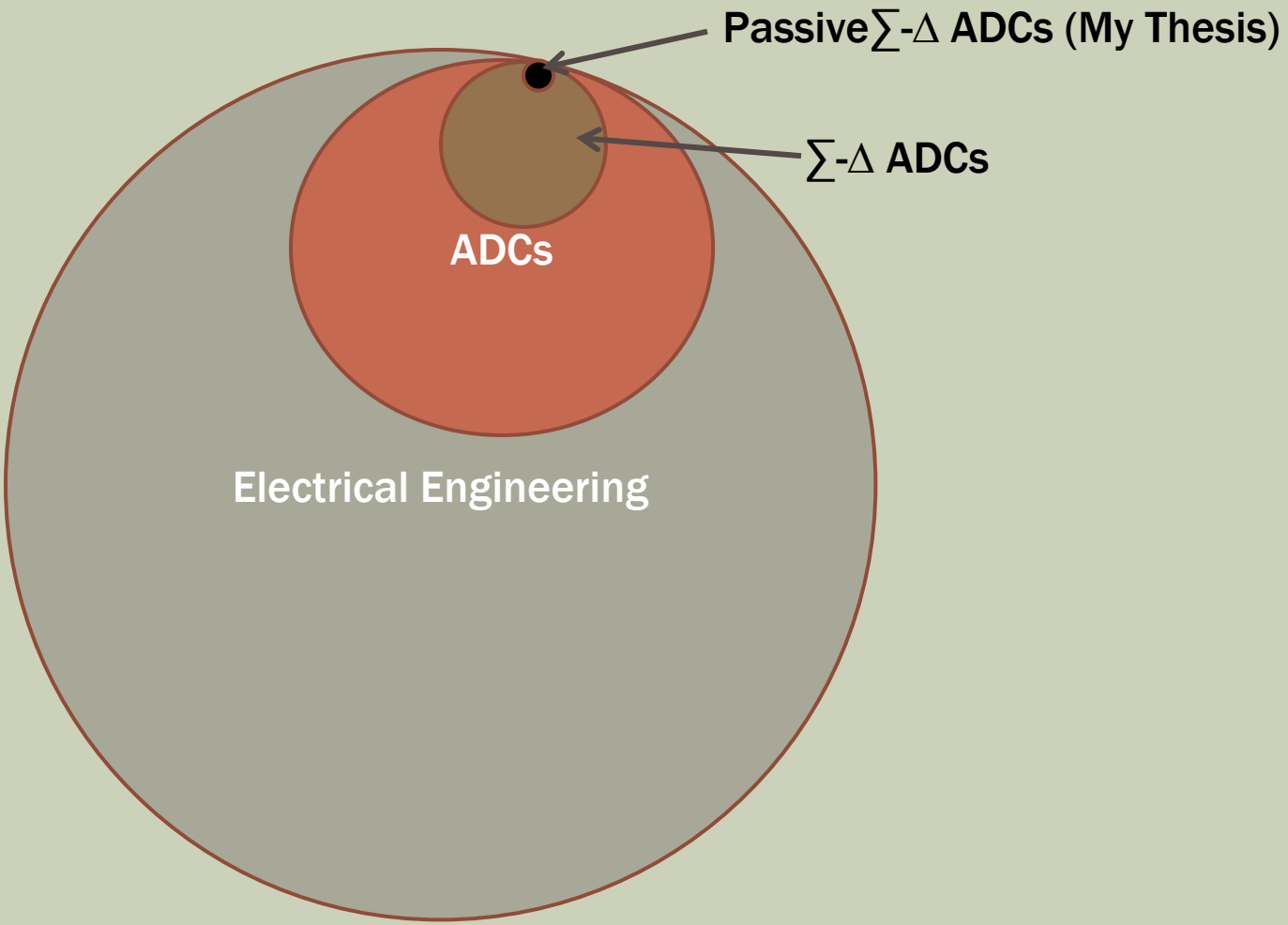
FITTING IN



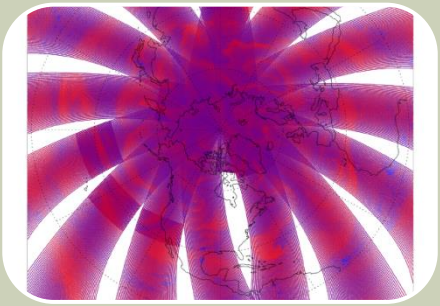
FITTING IN



FITTING IN

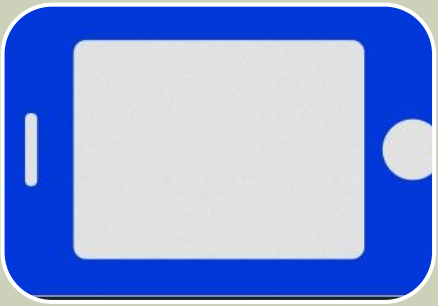

Passive∑-Δ ADCs (My Thesis)
∑-Δ ADCs
ADCs
Electrical Engineering

MARKET NEED FOR LOW POWER ∑-Δ ADC



Remote Sensing

Internet of Things



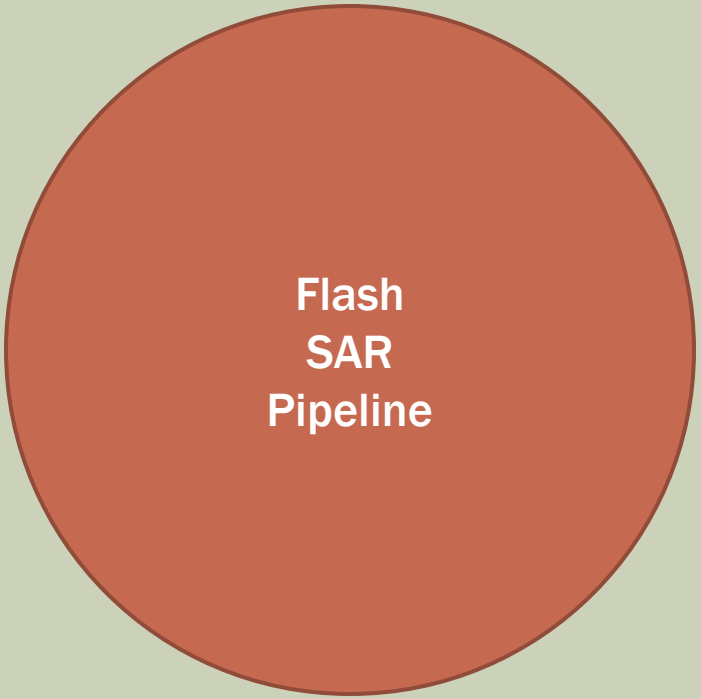
Mobile Devices

All these future devices and trends require low cost, low power ADCs.
High resolution and precision are not prioritized.
Passive ∑-Δ ADCs can meet this need.

All images are from Wikimedia Commons

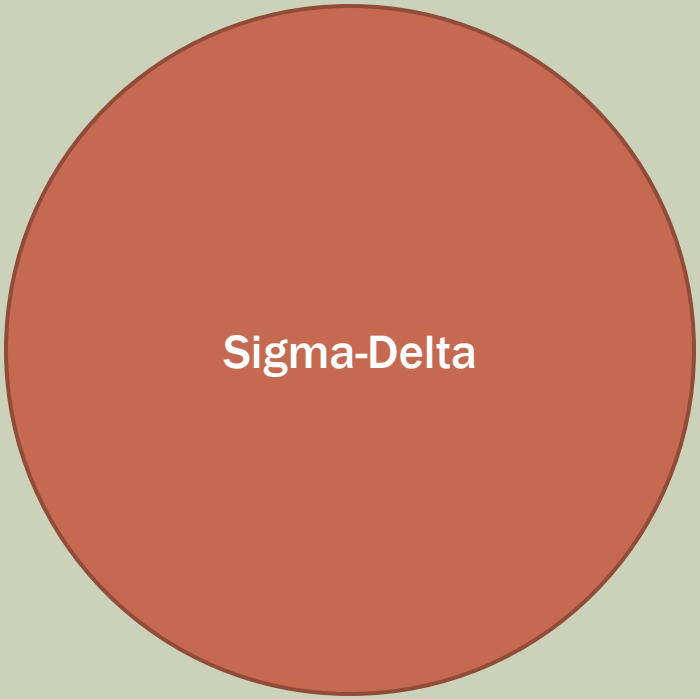
ANALOG-TO-DIGITAL CONVERTERS

Nyquist Rate ADCs



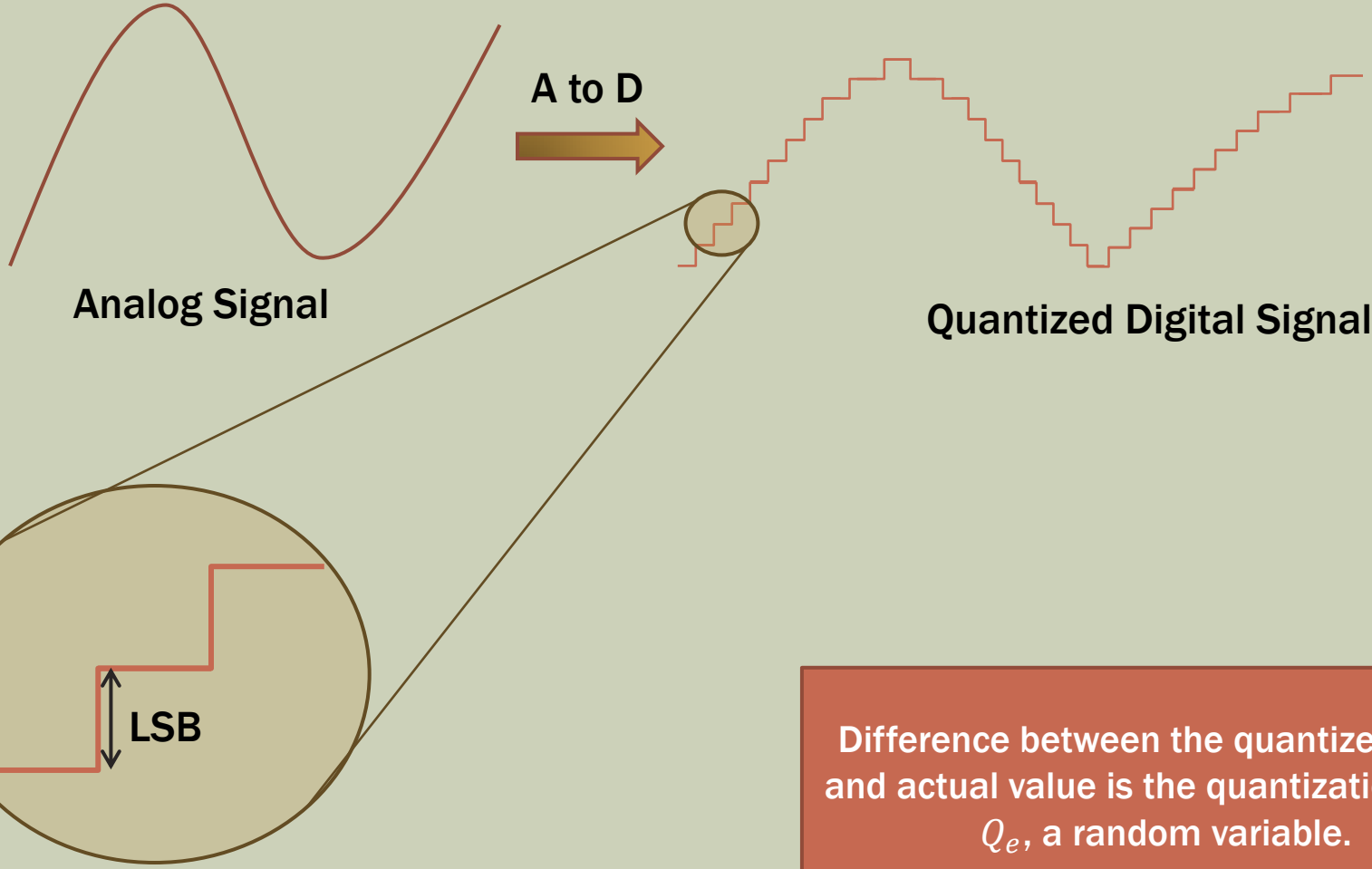
–Sampling rate is at least twice the input bandwidth.
–Resolution is limited to nominal value.

Oversampling ADCs



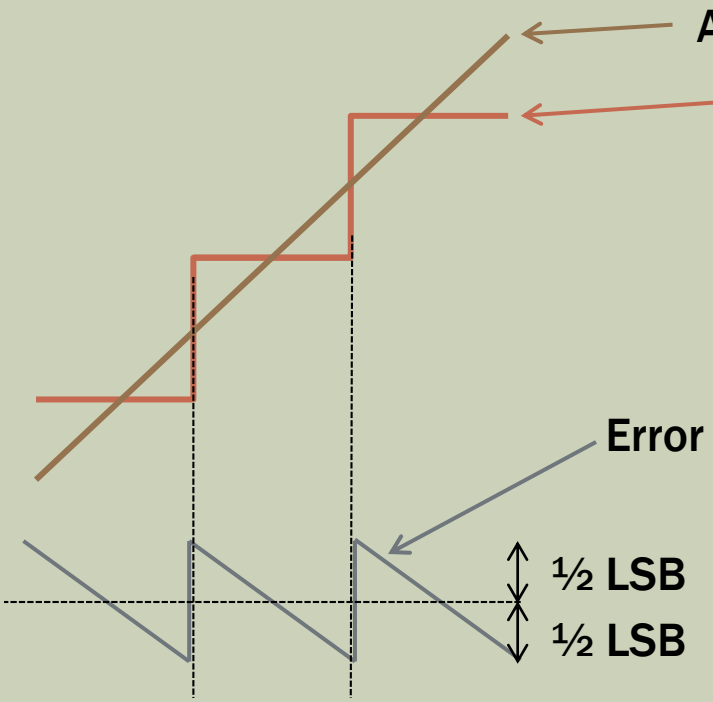
–Sampling rate is much higher than input bandwidth.
–Resolution is higher than the nominal value.

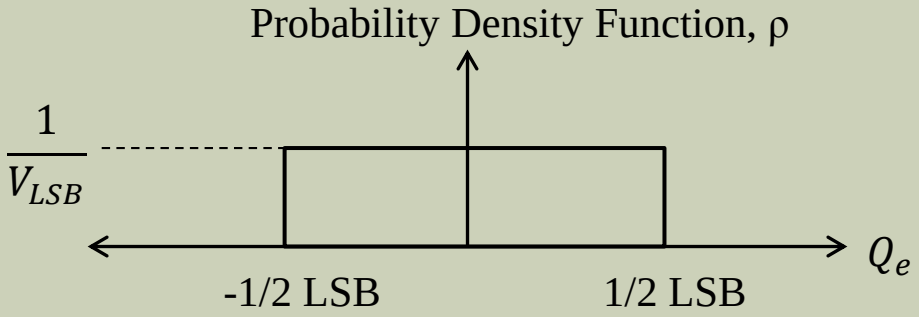
QUANTIZATION ERROR



Difference between the quantized value and actual value is the quantization error, Q_e, a random variable.

QUANTIZATION ERROR



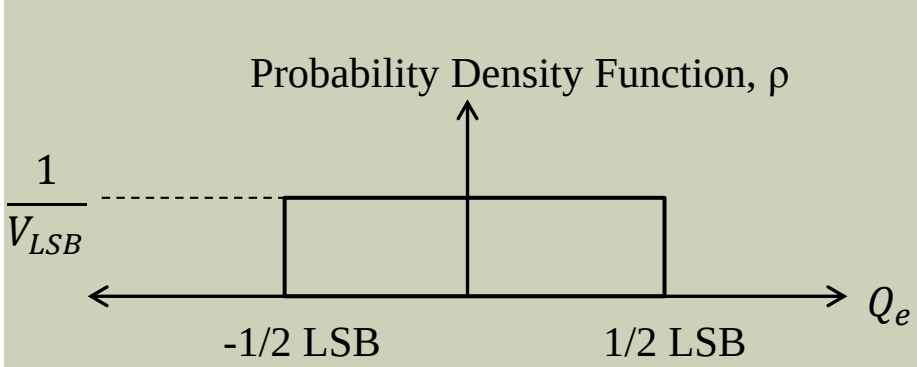


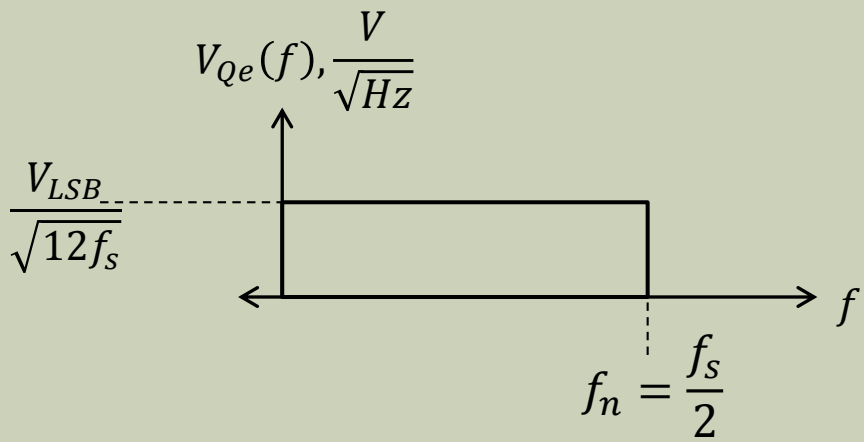
$$P_{Qe} = \int_{-\frac{1}{2}LSB}^{+\frac{1}{2}LSB} \rho * (Q_e) * dQ_e = \frac{V_{LSB}^2}{12}$$

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}}$$

PDF AND PSD OF QUANTIZATION ERROR

$$P_{Qe} = \int_{-\frac{1}{2}LSB}^{+\frac{1}{2}LSB} \rho * (Q_e) * dQ_e = \frac{V_{LSB}^2}{12} = 2 * \int_0^{\frac{fs}{2}} V_{Qe}^2(f) * df$$





$\boldsymbol{P_{Qe}}$:Quantization Noise Power

$\boldsymbol{Q_e}$: Quantization Error

$\boldsymbol{V_{LSB}}$: Least-Significant-Bit Voltage

Key

$\boldsymbol{V_{Qe}(f)}$: Quantization Noise Voltage

$\boldsymbol{V_{Qe}^2(f)}$: Quantization Noise Power Spectral Density

$\boldsymbol{f_n}$: Nyquist Frequency

$\boldsymbol{f_s}$: Sampling Frequency

OVERSAMPLING

Oversampling is running a data converter at a sampling rate beyond the Nyquist criterion in order to increase its resolution.

Nyquist Criterion

$$f_{sampling} = 2f_{MAX}$$

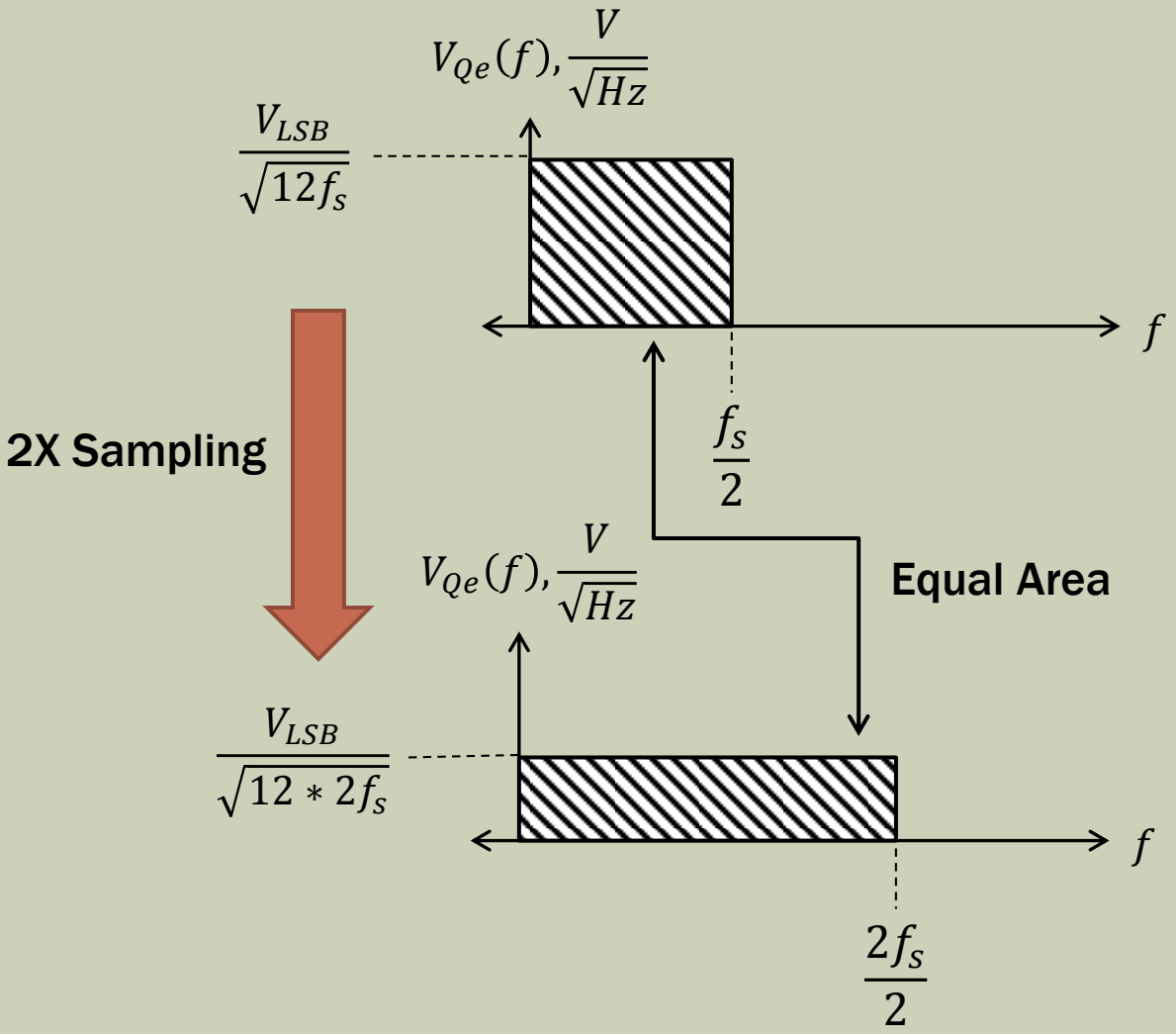
Oversampling Ratio

$$OSR = 2^{2n}$$

QUANTIZATION NOISE

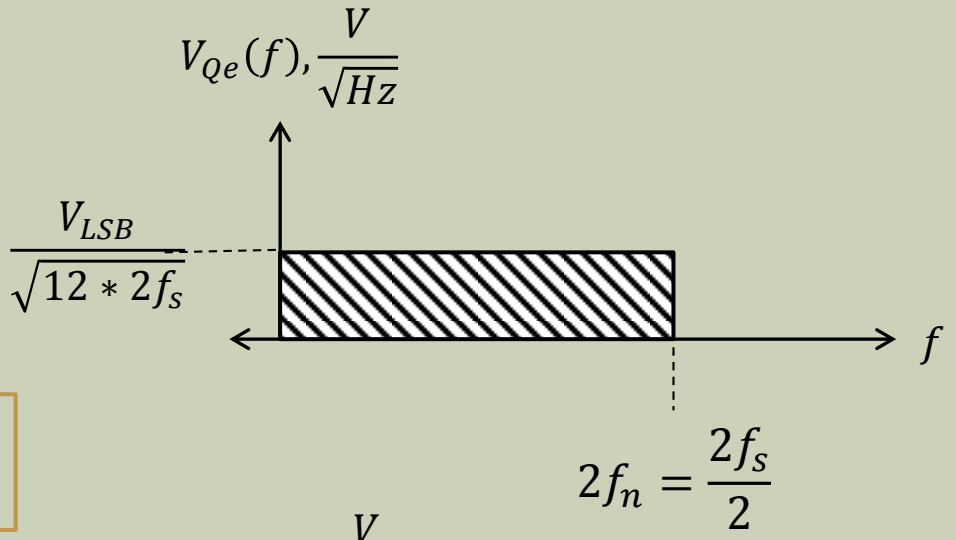
RMS quantization noise Is the same regardless of sampling frequency.

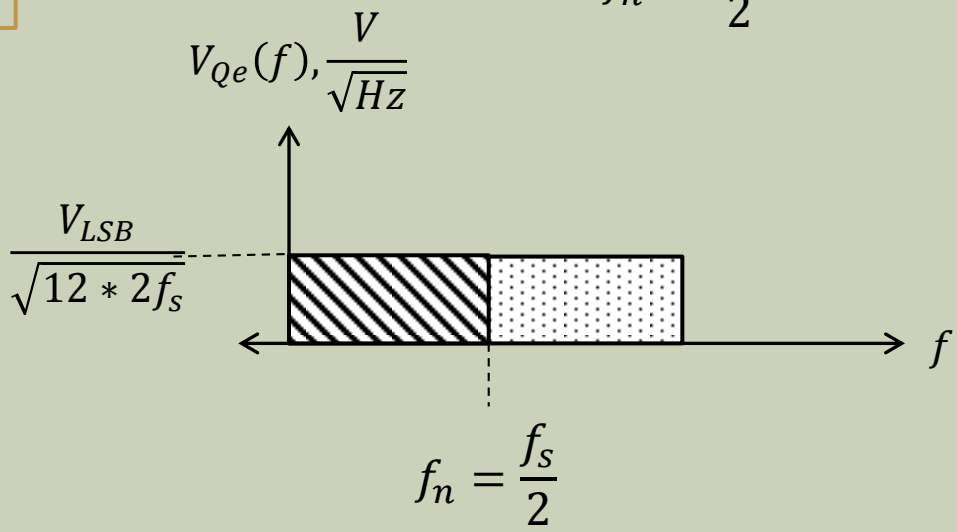
But the distribution as a function of frequency is different.



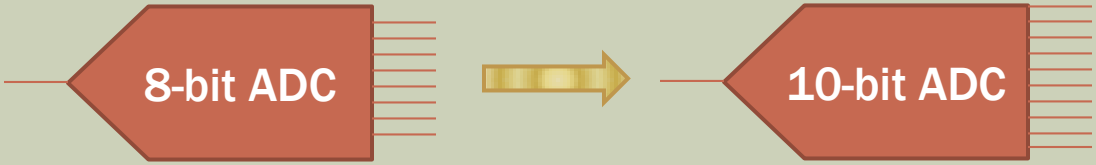
BANDLIMITING

Bandlimiting reduces quantization noise by restricting bandwidth.





OVERSAMPLING EXAMPLE



1 MHz Bandwidth
2 MHz Sampling Rate

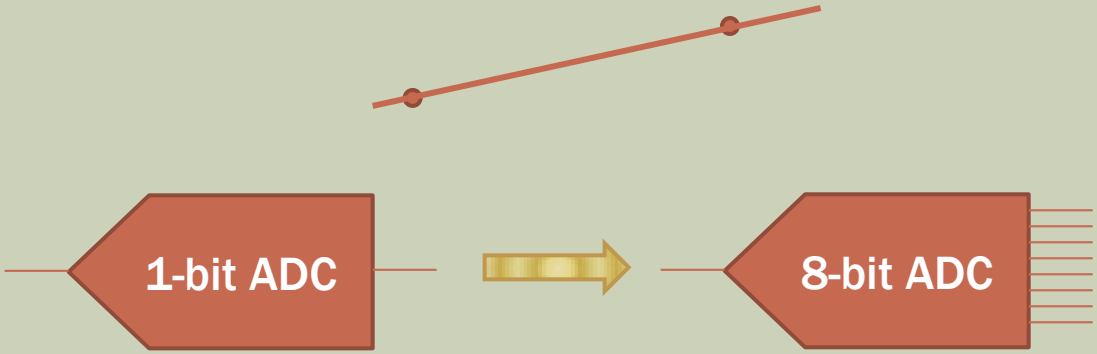
1 MHz Bandwidth
32 MHz Sampling Rate

$$OSR = 2^{2n}$$
$$OSR = 2^{2*2} = 16$$

Caveat Inherent linearity of data converter must be equal to desired resolution.

1-BIT ADC

Solution A 1-bit ADC is inherently linear because two points define a perfectly straight line.



1 MHz Bandwidth
2 MHz Sampling Rate

1 MHz Bandwidth
32.768 GHz Sampling Rate!

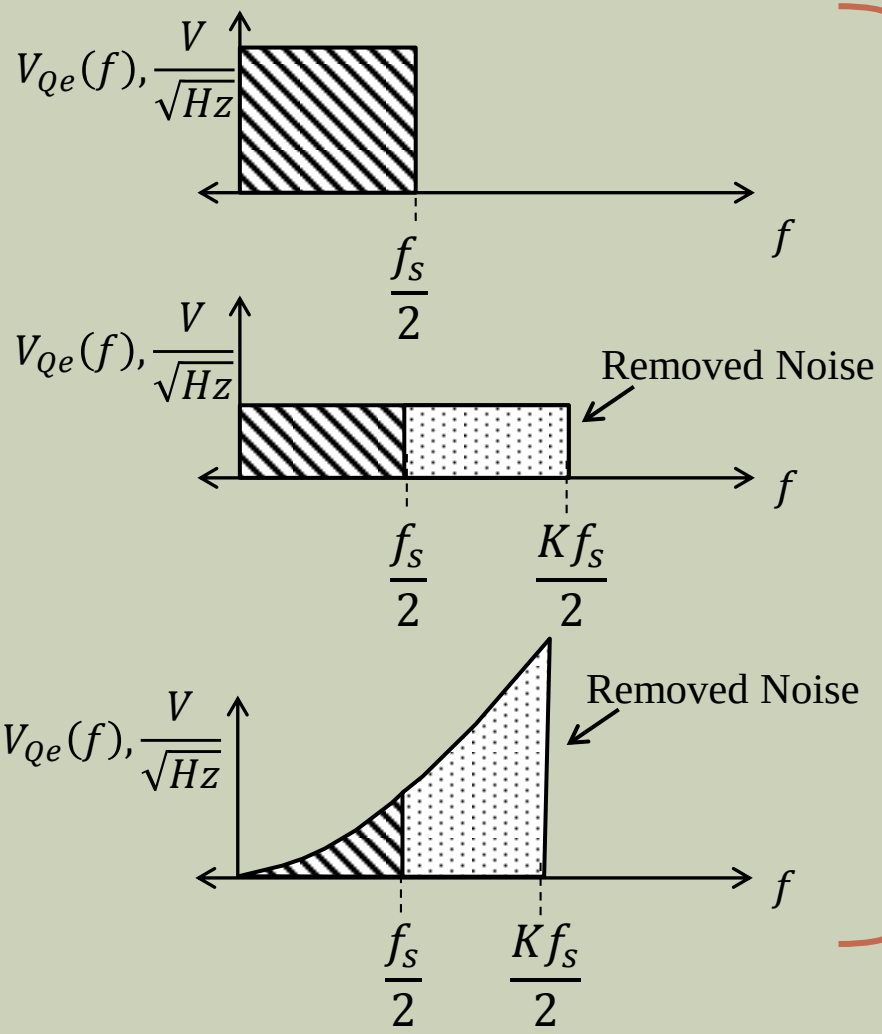
$$OSR = 2^{2n}$$
$$OSR = 2^{2*7} = 16{,}384$$

NOISE SHAPING

Nyquist Rate

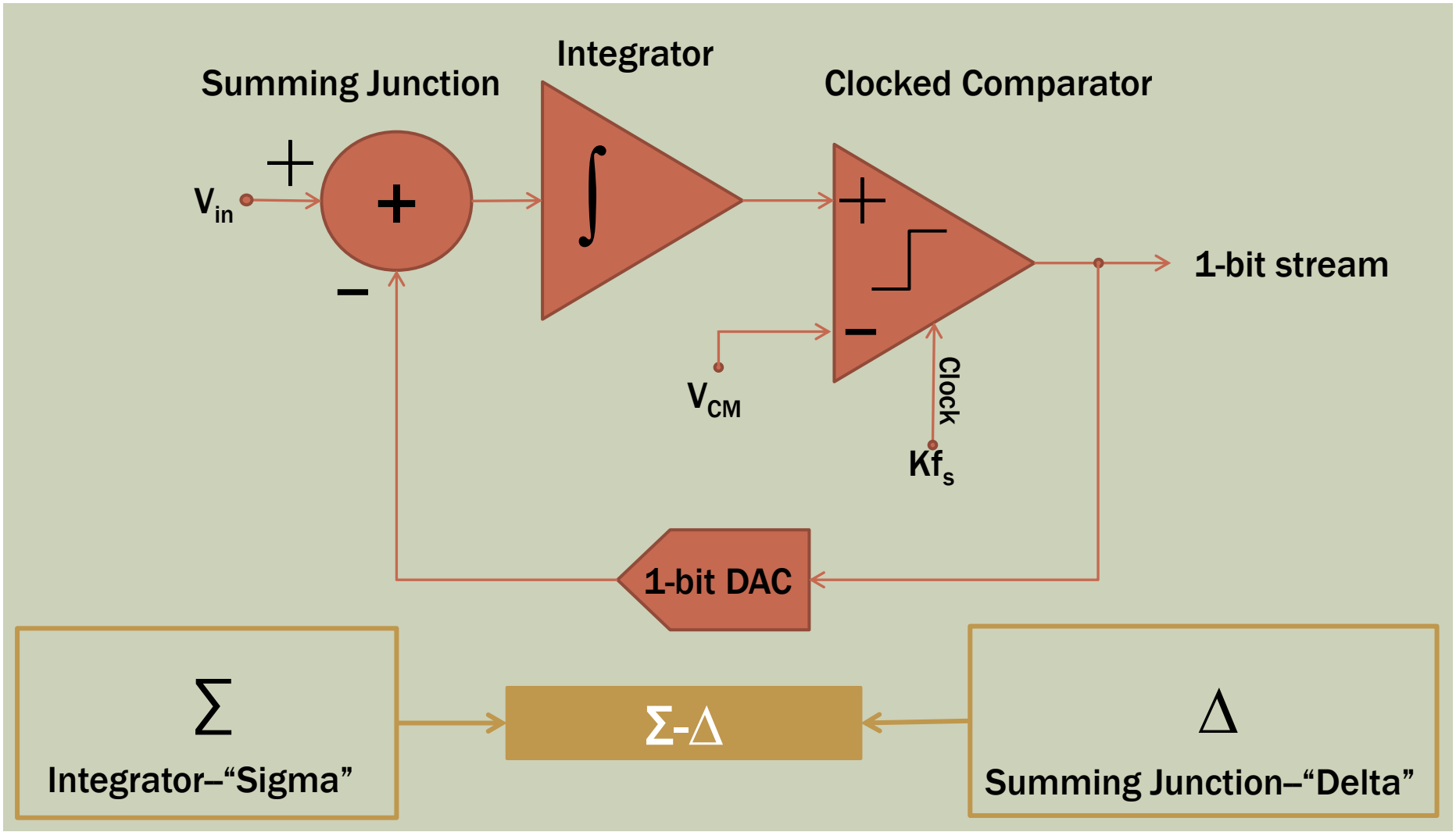
Simple Oversampling

Oversampling with Noise Shaping

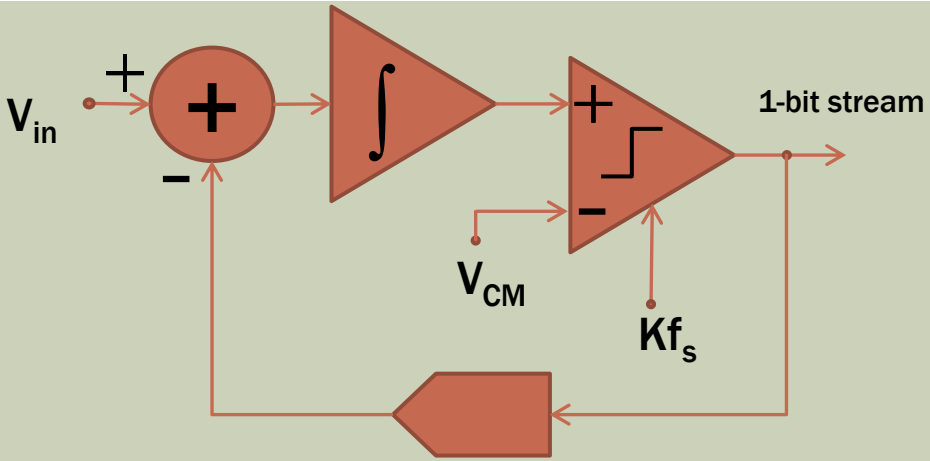


RMS quantization noise, $V_{Qe,RMS}$ remains $\frac{V_{LSB}}{\sqrt{12}}$ in all examples but bandlimiting reduces noise in the signal bandwidth.

BASIC 1ST ORDER ∑-Δ MODULATOR

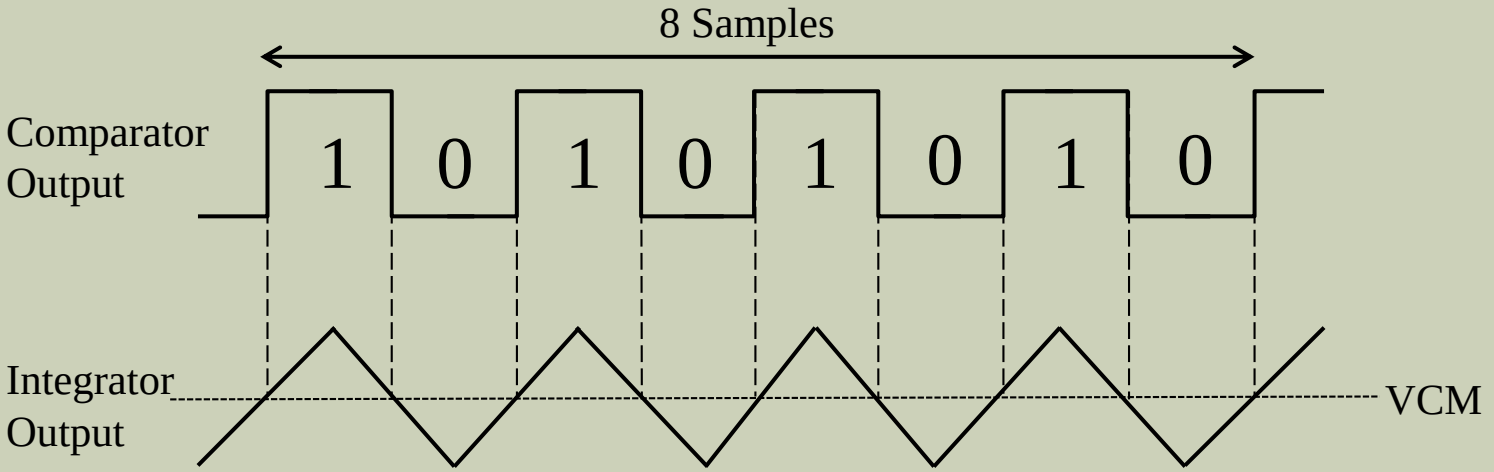


∑-Δ MODULATOR WITH DC INPUT

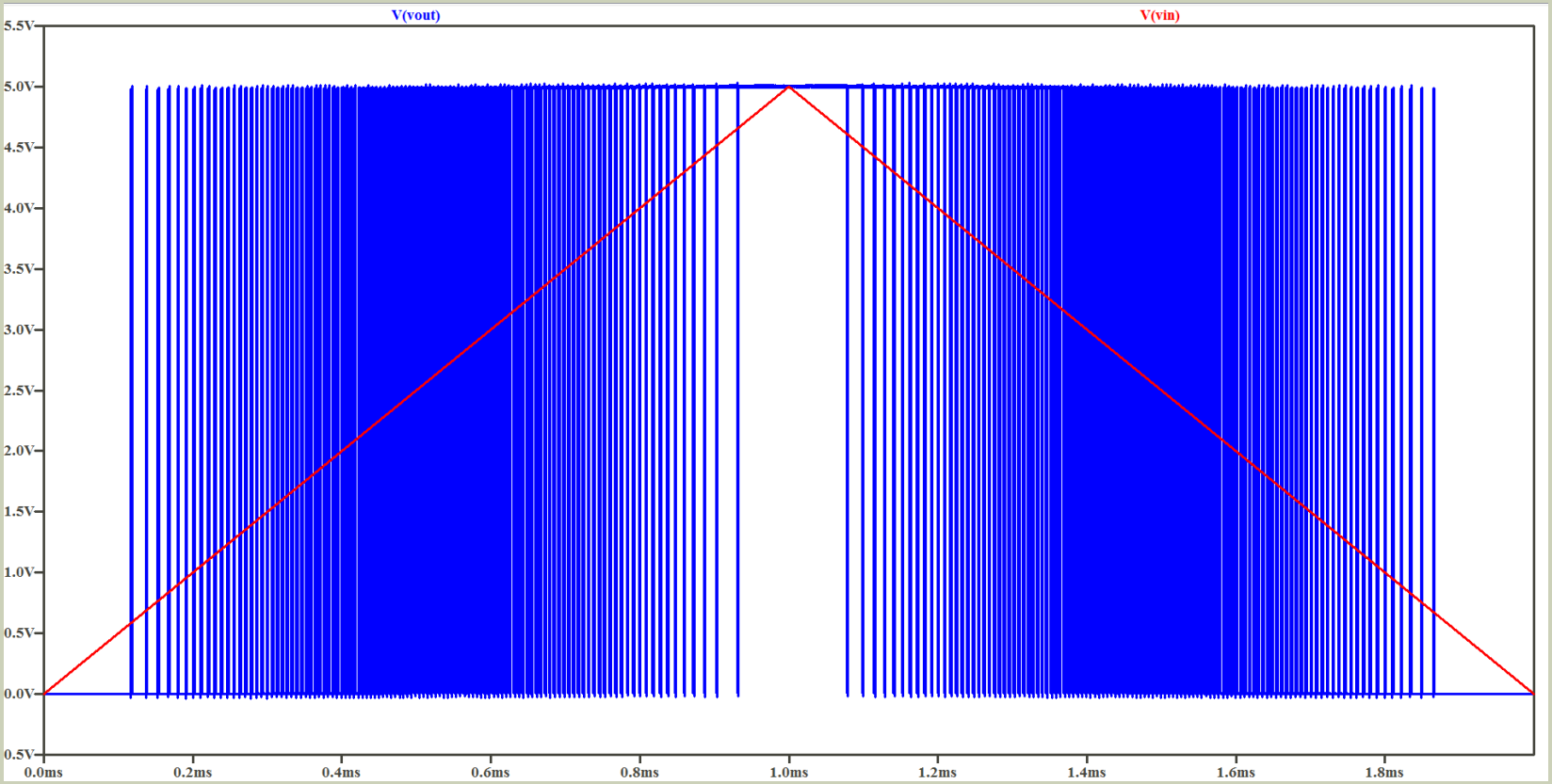


$$Input = V_{CM} = \frac{1}{2} * Full\ Scale\ Voltage$$

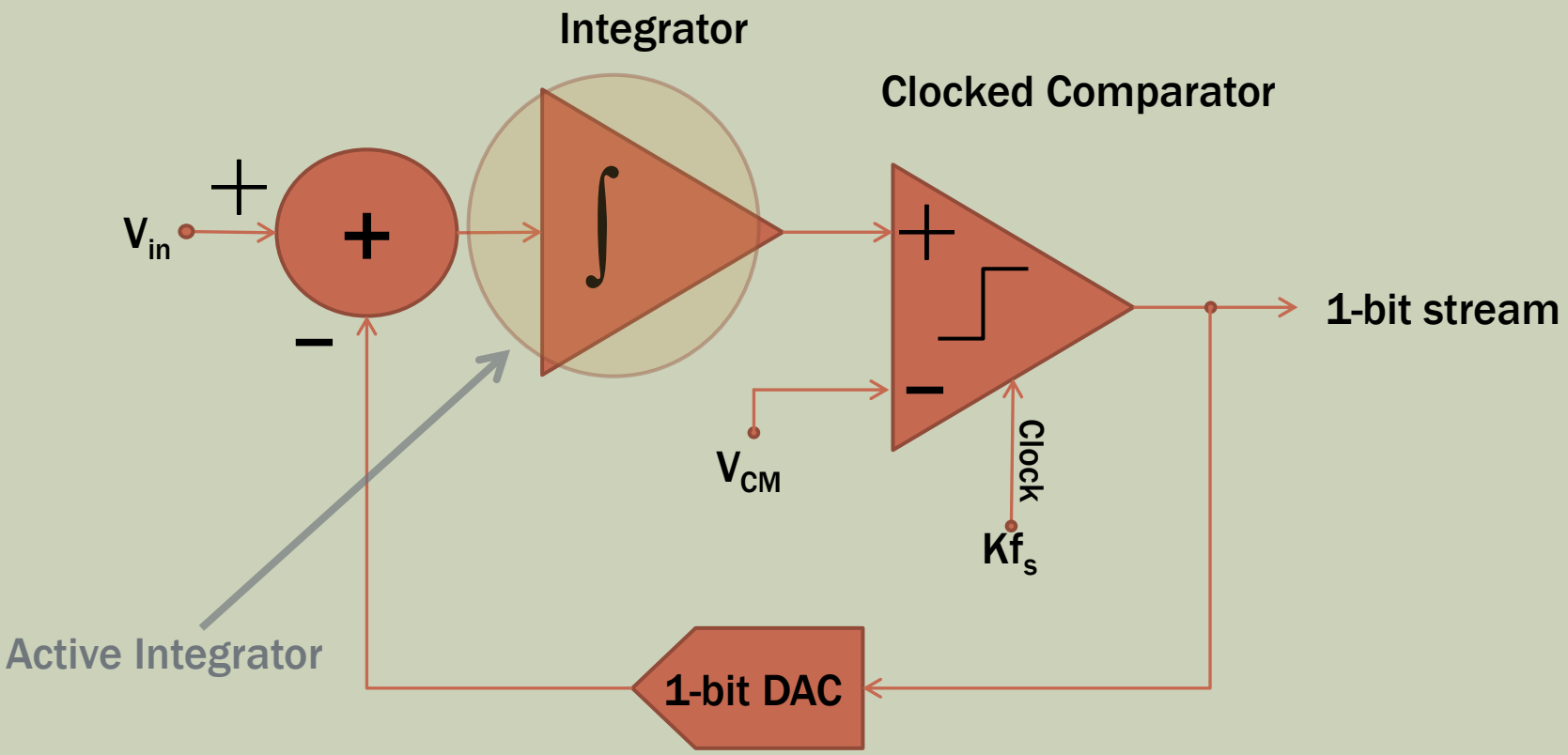
$$Average\ Output = \frac{1+1+1+1}{8} = \frac{1}{2}$$



1-BIT OUTPUT


V(vout)
V(vin)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.5V
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms

BASIC 1ST ORDER ∑-Δ MODULATOR



Generally, ∑-Δ modulators use an active integrator to keep the voltage swing on the integrator's input to a minimum (ideally zero).

WHY PASSIVE?

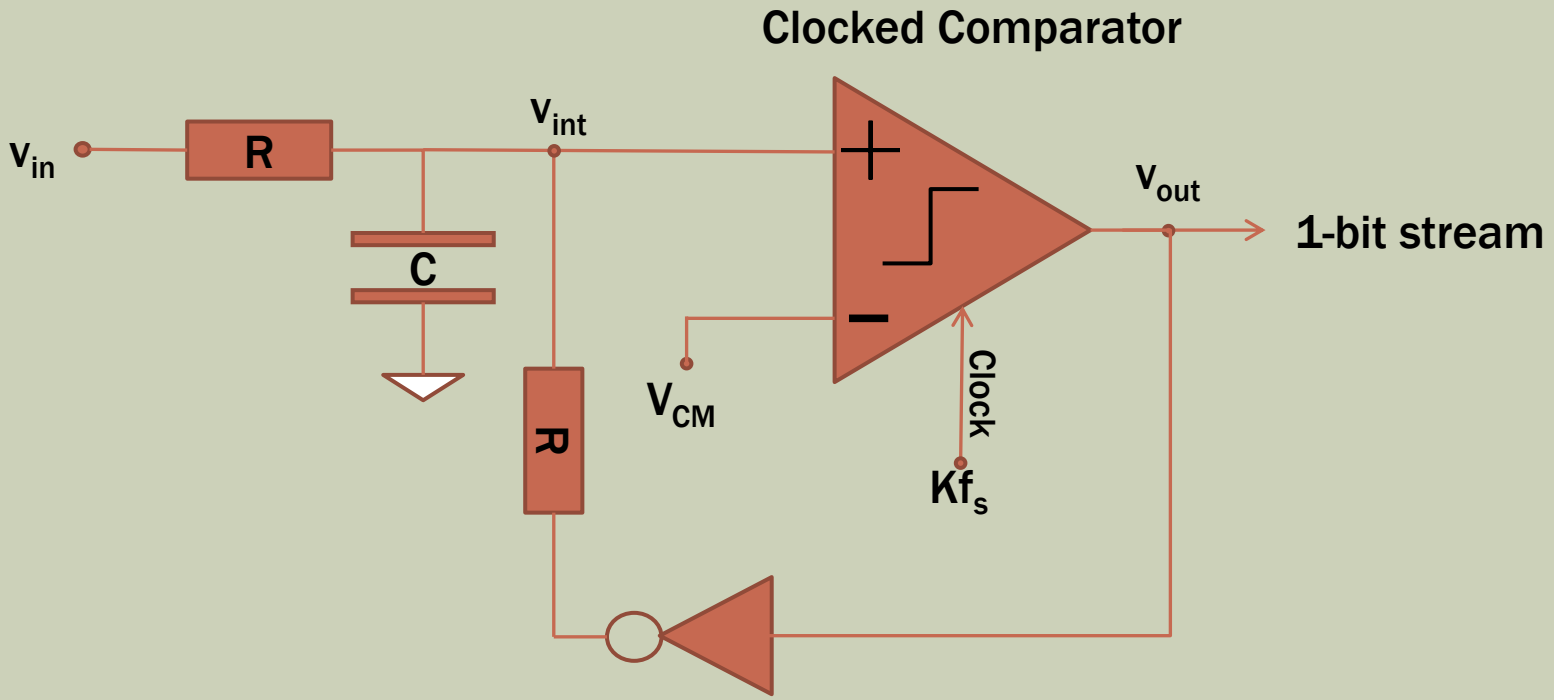
Lower Power

- Active integrators constantly draw current for biasing.
- Passive modulators only draw current while switching.

Higher Speed

- Passive modulators are not limited by op-amp GBW performance.

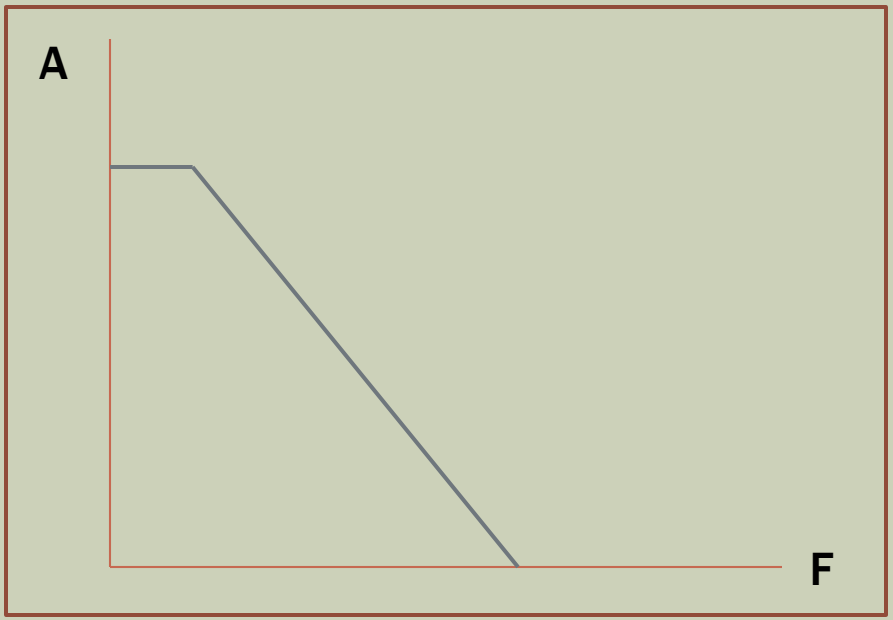
1ST ORDER PASSIVE ∑-Δ MODULATOR



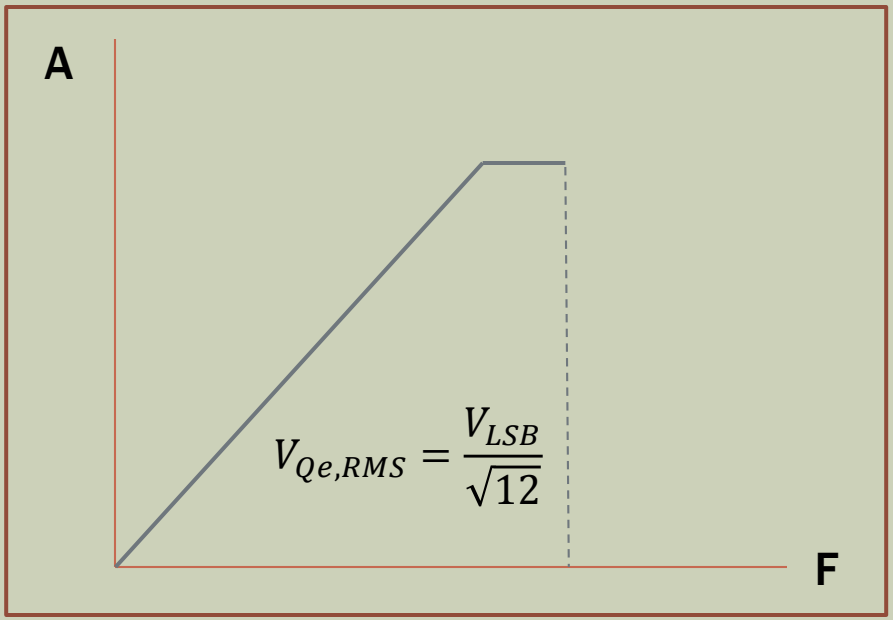
STF NTF DT (distortion term)

$$v_{out} = \underbrace{\frac{1}{1+sRC}}_{\text{STF}} \cdot v_{in} + \underbrace{\frac{sRC}{1+sRC}}_{\text{NTF}} \cdot V_{Qe} + \underbrace{\frac{-2}{1+sRC}}_{\text{DT (distortion term)}} \cdot v_{int}$$

TRANSFER FUNCTIONS

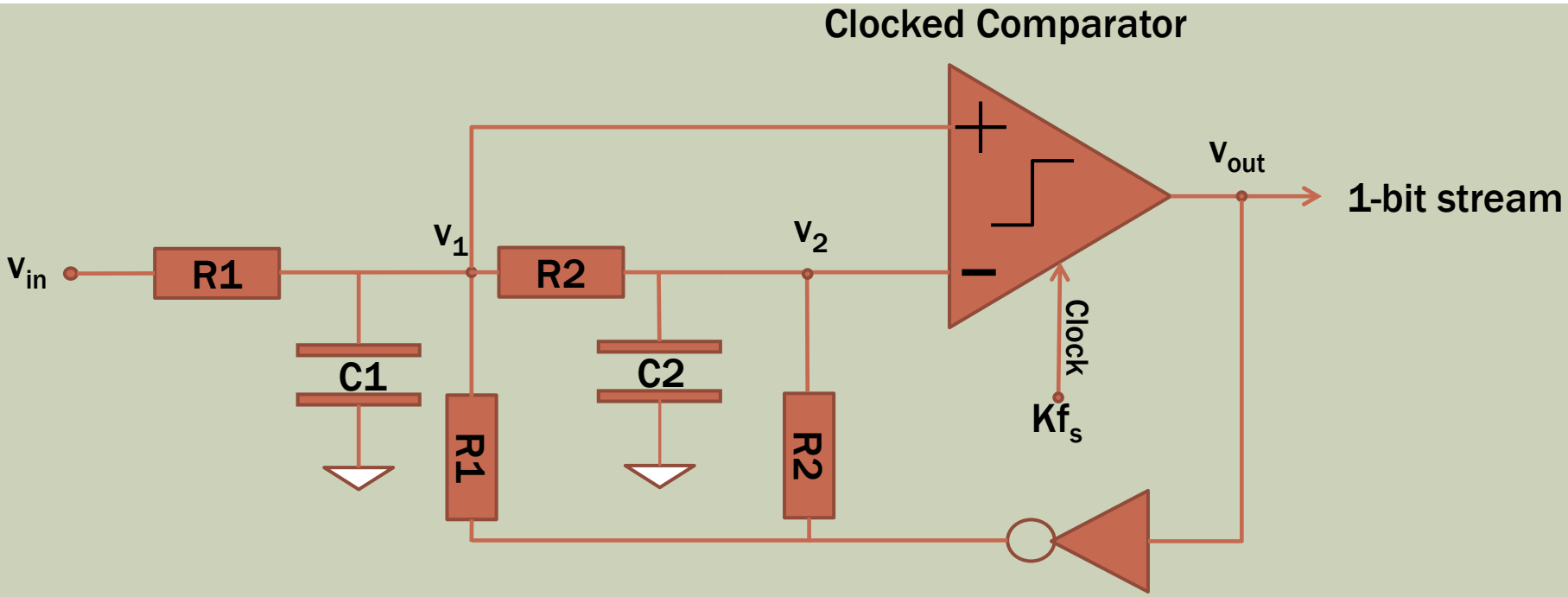


Signal Transfer Function Plot $\frac{1}{1+sRC}$



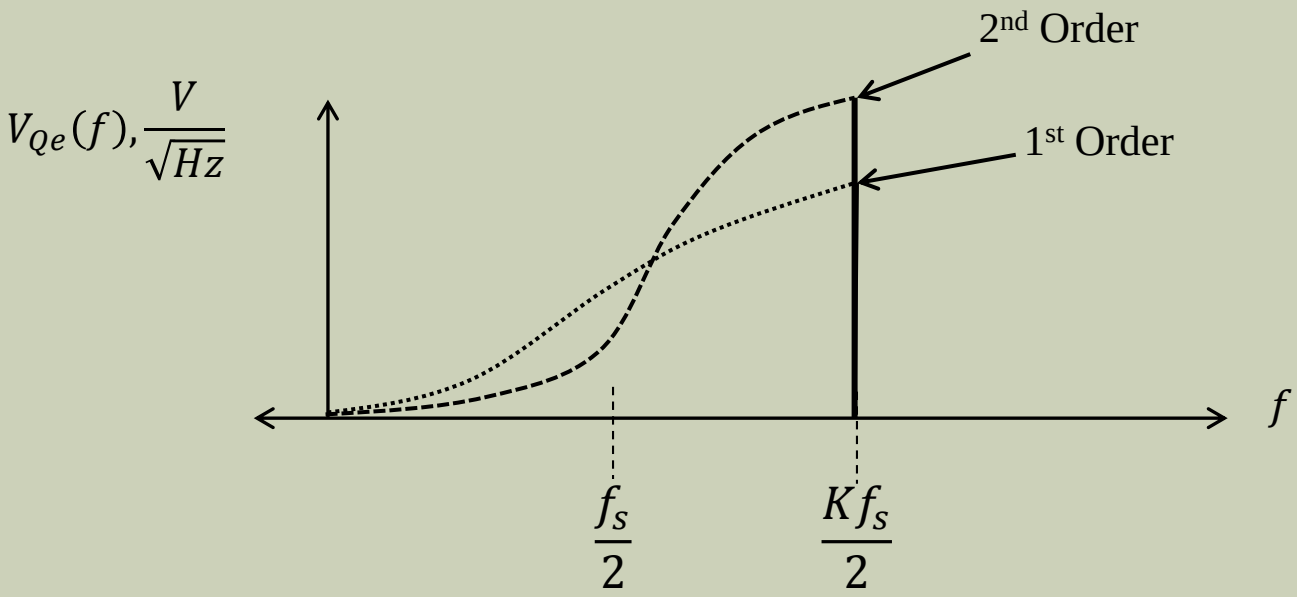
Noise Transfer Function Plot $\frac{sRC}{1+sRC}$

CONVENTIONAL 2ND ORDER PASSIVE ∑-Δ MODULATOR



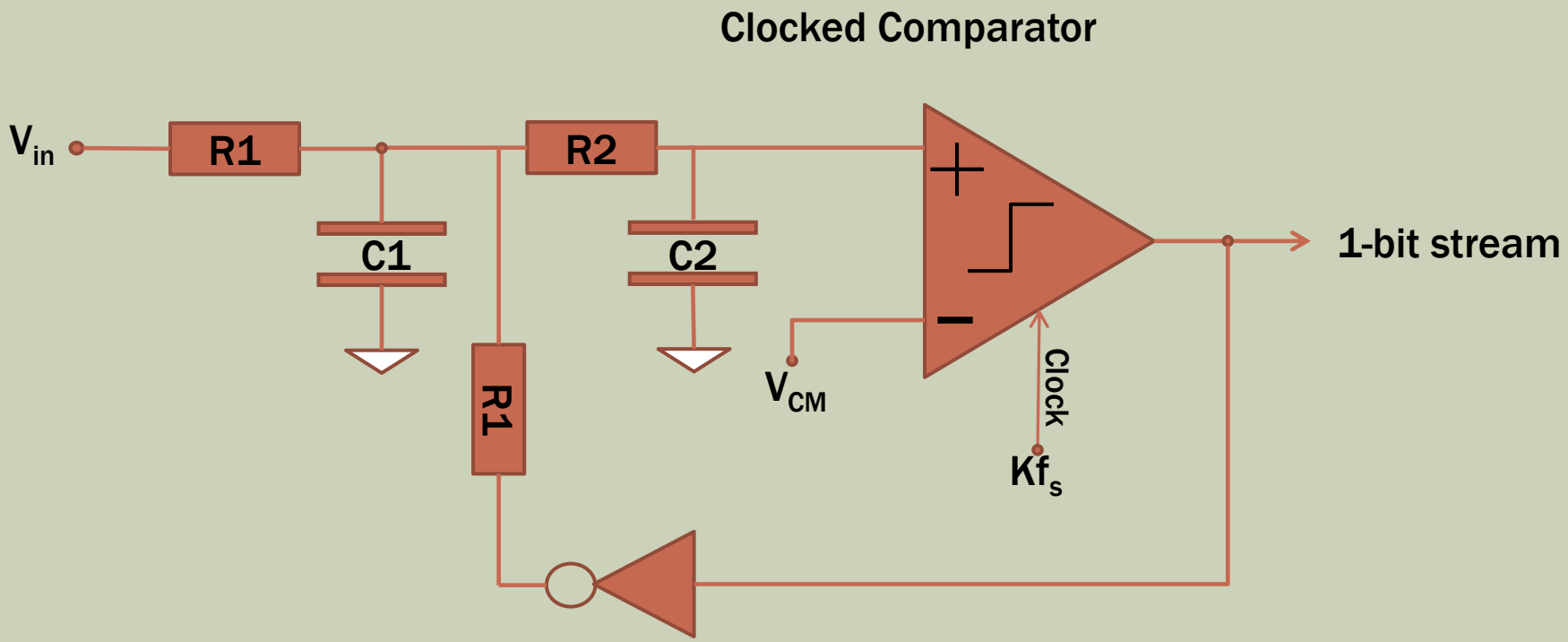
$$v_{out}{}^2 = \overbrace{\frac{1}{1+(\omega RC)^2}}^{\text{STF}} \cdot v_{in}{}^2 + \overbrace{\frac{(\omega RC)^2}{1+(\omega RC)^2}}^{\text{NTF}} \cdot \frac{V_{Qe}{}^2}{2} + \overbrace{\frac{2v_1 + v_2}{1+(\omega RC)^2}}^{\text{DT (distortion term)}}$$

NOISE SHAPING ORDER



Increasing the order of the noise shaping reduces quantization noise within the signal bandwidth.

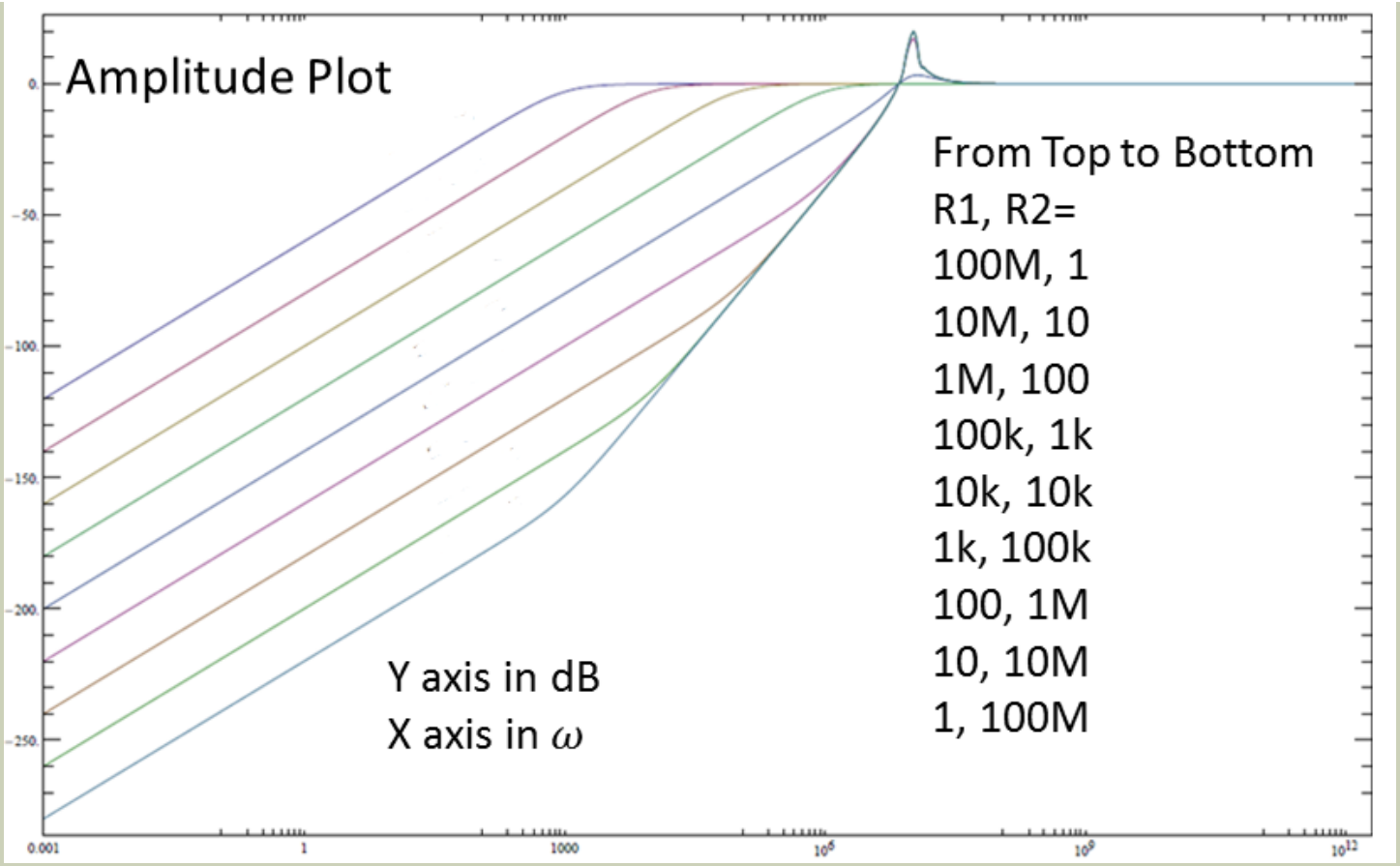
PROPOSED 2ND ORDER MODULATOR



STF NTF DT (distortion term)

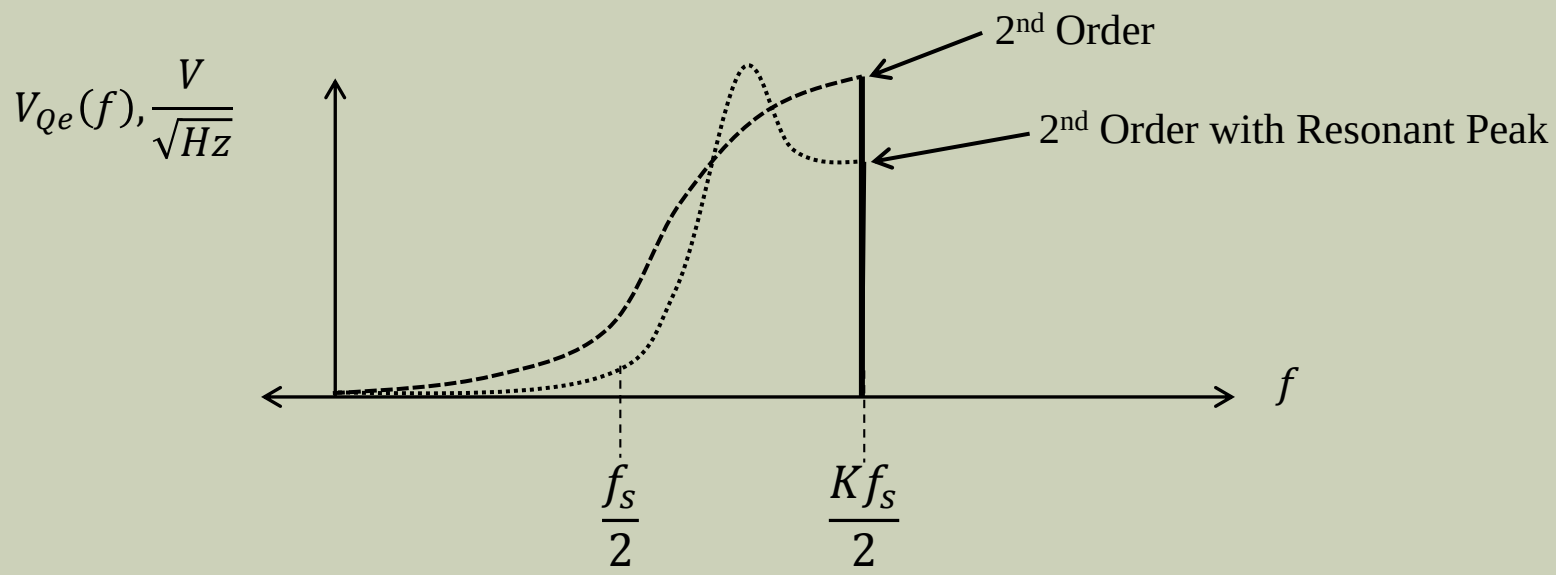
$$v_{out} = \frac{1 + sR_2C_2}{1 + sR_2C_2 + sR_1C_1} \cdot v_{in} + \frac{s(sR_1C_1R_2C_2 + R_1C_1)}{1 + sR_1C_1 + s^2R_1C_1R_2C_2} \cdot V_{Qe} + \frac{1}{1 + sR_1C_1 + (1 + sR_2C_2)} \cdot v_{int}$$

MATHEMATICA PLOT OF NTF



Quantization noise is shifted to a resonant peak.

CONCEPTUAL NTF PLOT



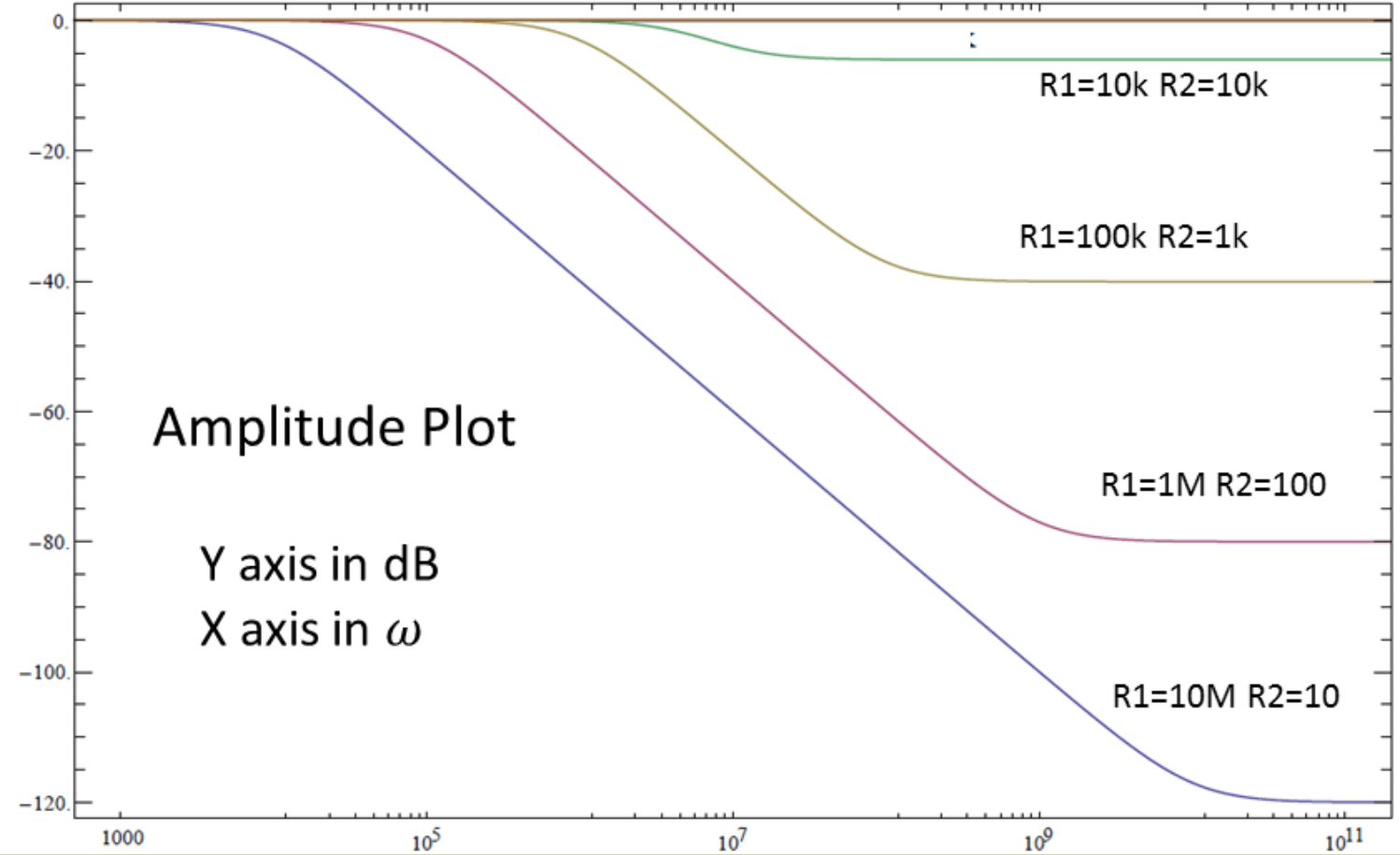
Area under both curves is the same, but the NTF with the resonant peak has less noise within the signal bandwidth.

Low quantization noise within signal bandwidth

Trade-Off

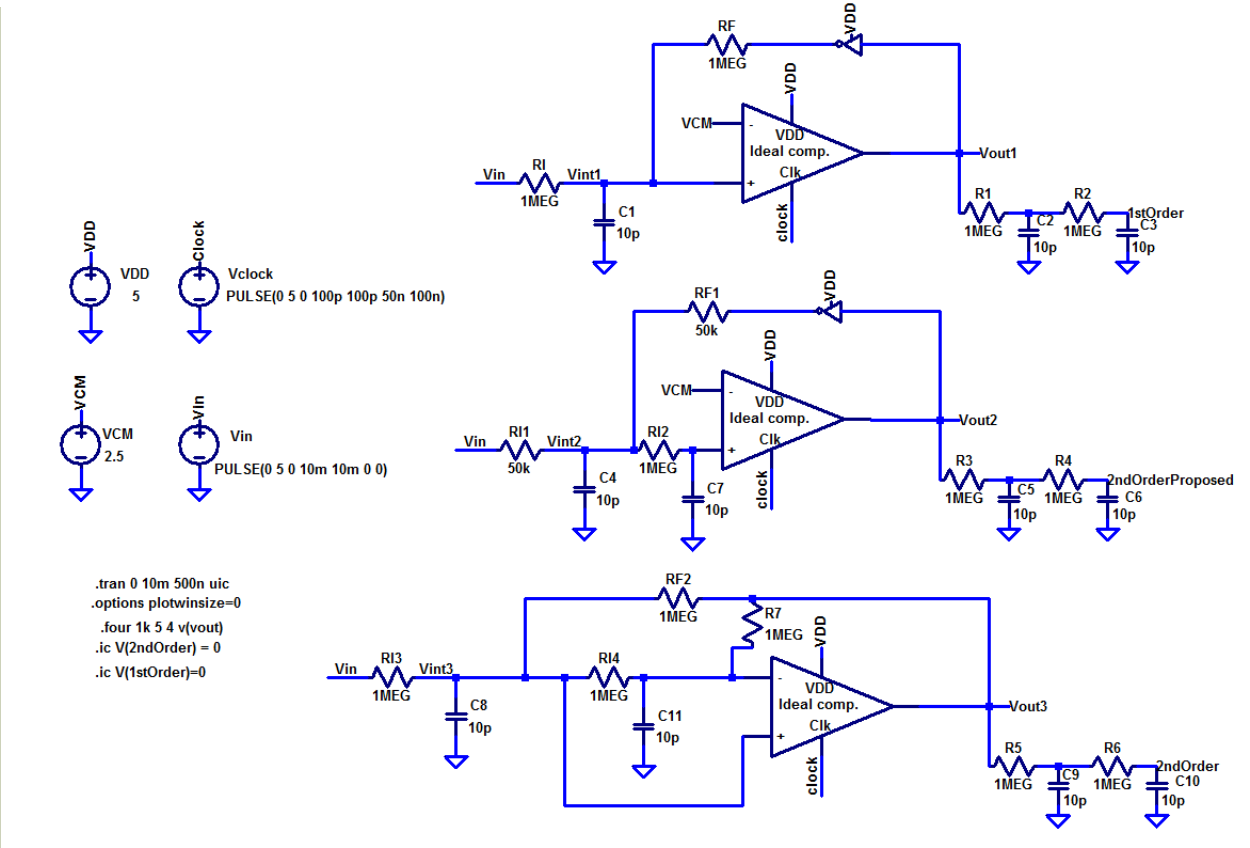
Resonant peak

MATHEMATICA PLOT OF STF



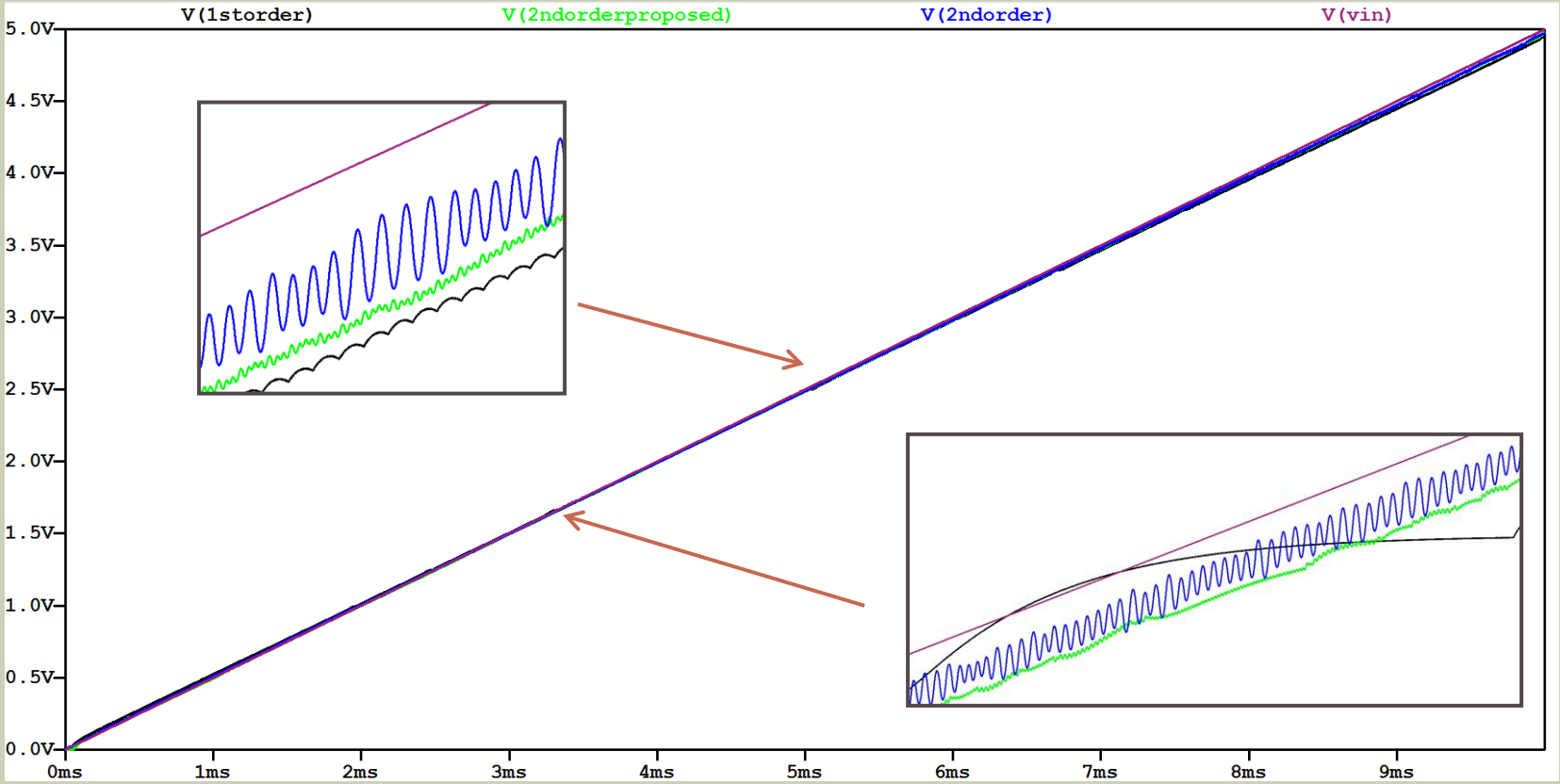
Signal transfer function exhibits 1st order low-pass behavior.

SPICE SIMULATIONS



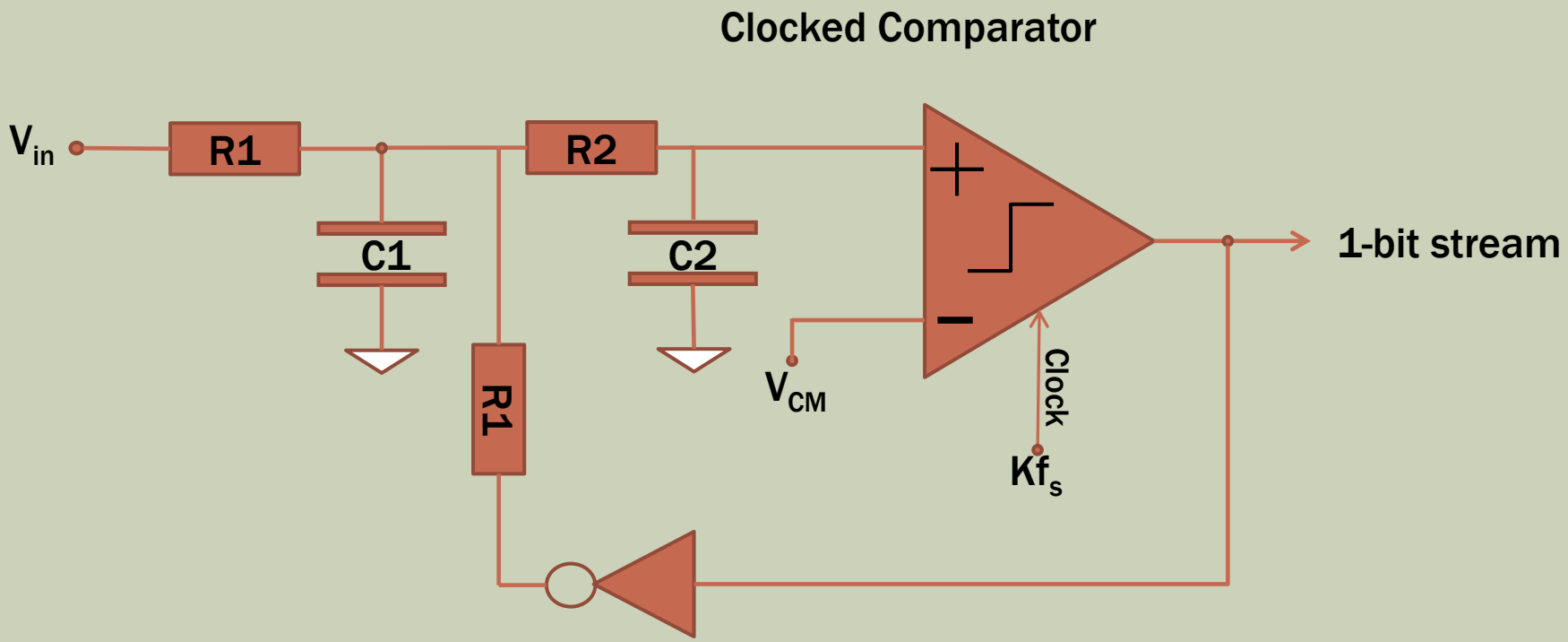
Each topology was simulated in LTspice using ideal components.

SPICE SIMULATIONS

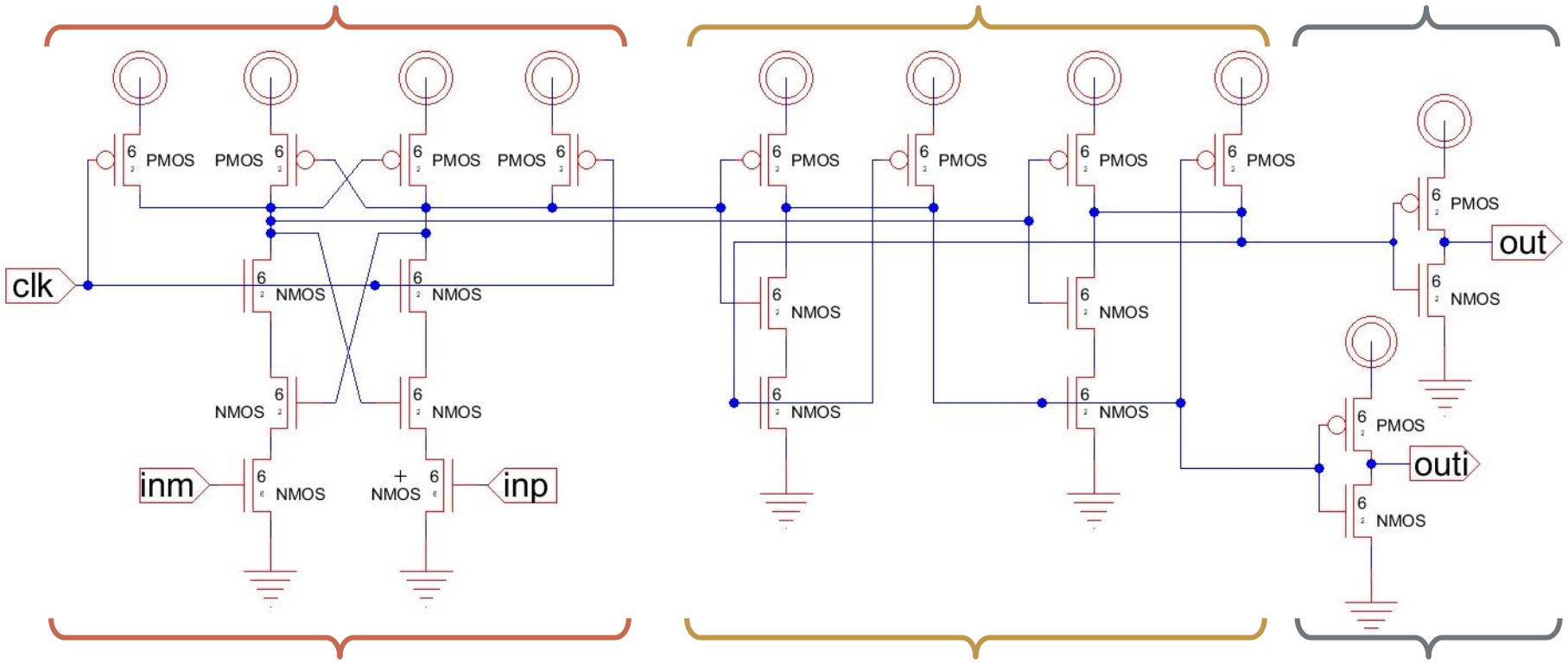


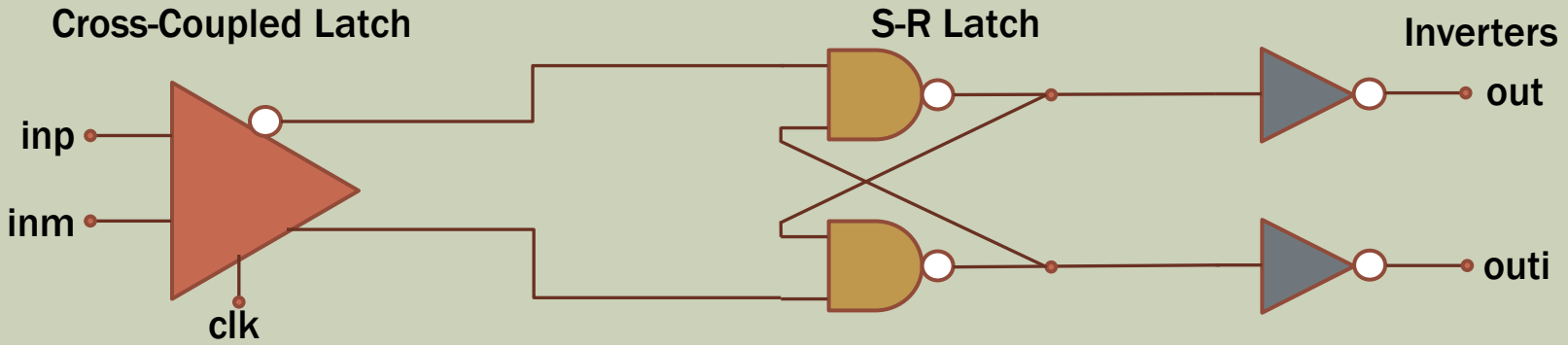
Linearity Comparison of ∑-Δ Modulator Topologies with a 10mS 0-5V Ramp Input

IC IMPLEMENTATION

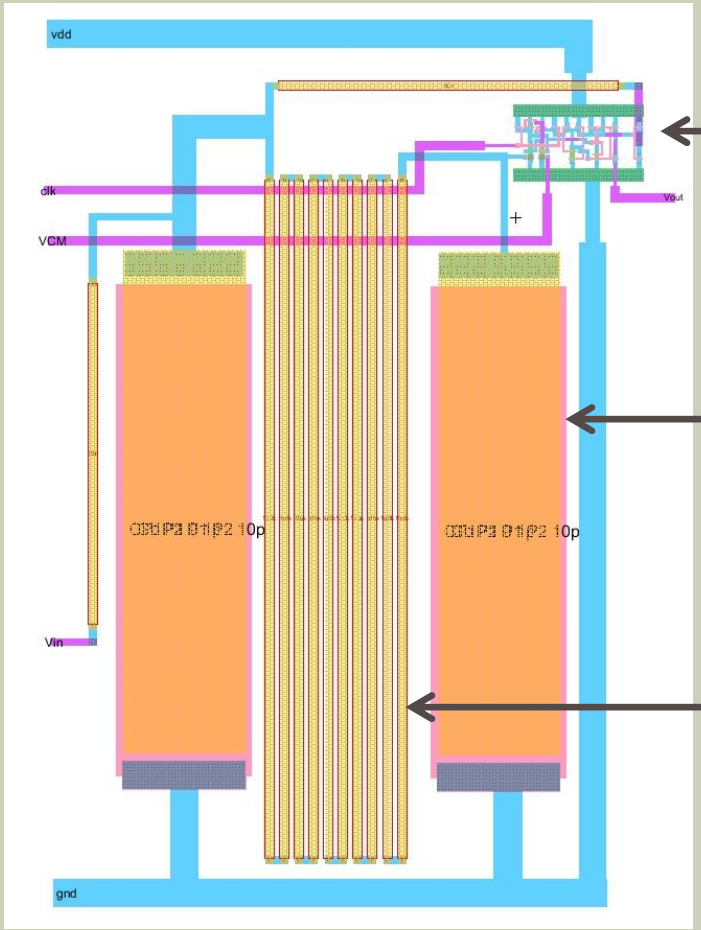


LOW POWER COMPARATOR DESIGN





CHIP LAYOUT



400 µm

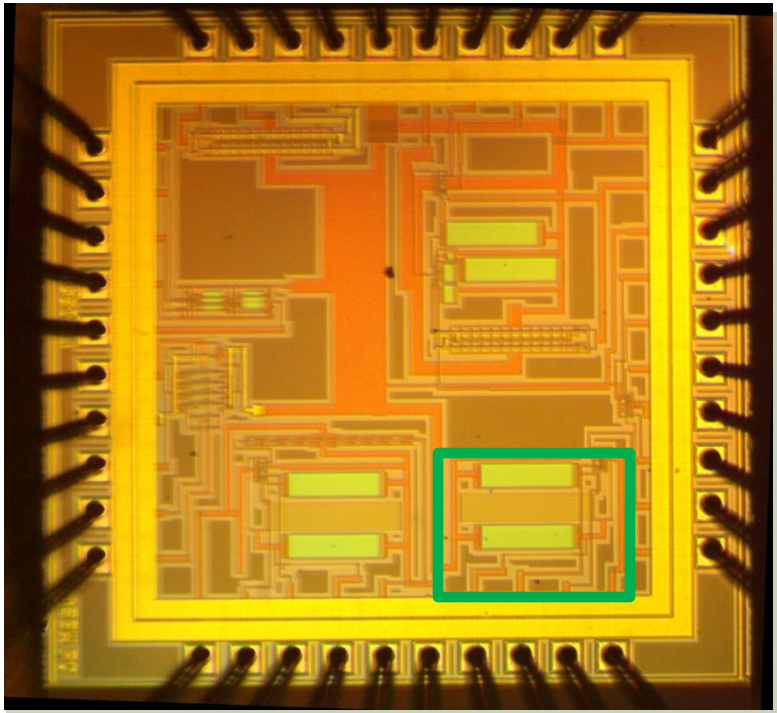
270 µm

Low Power Comparator With Minimum Size Devices

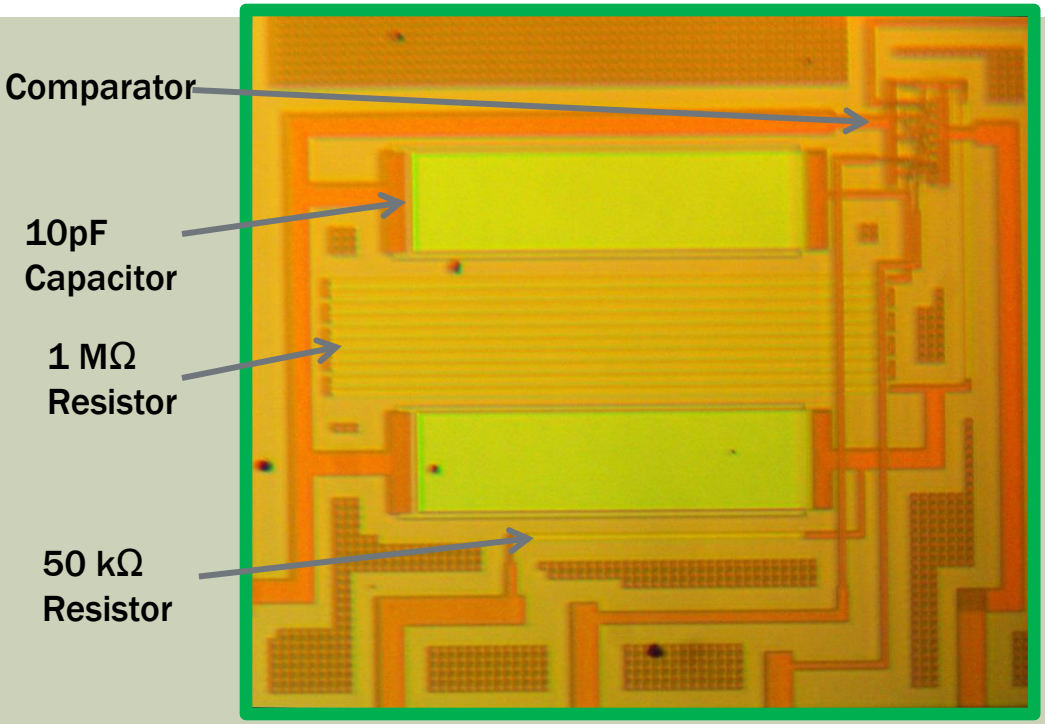
Poly1-Poly2 Capacitor

High Resistivity Poly2 Resistor

CHIP MICROGRAPHS

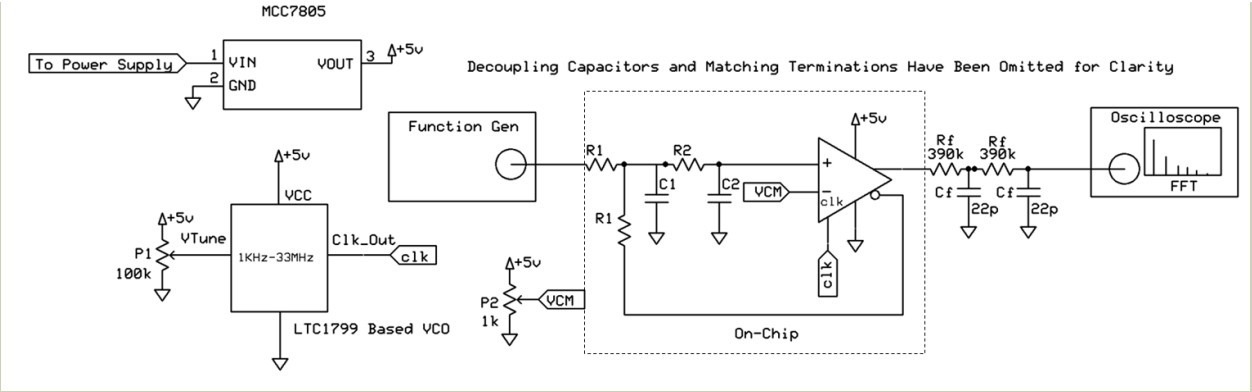


Micrograph of Entire Chip
Area = 1.5 mm^2
Proposed Modulator in Green

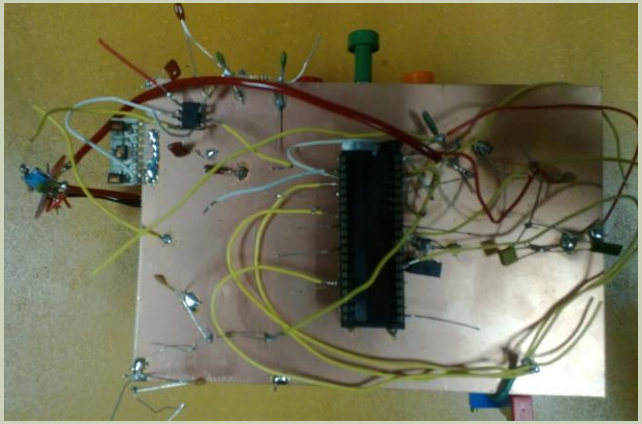


Micrograph of Proposed Modulator
Area in View ≈ 400 μm^2

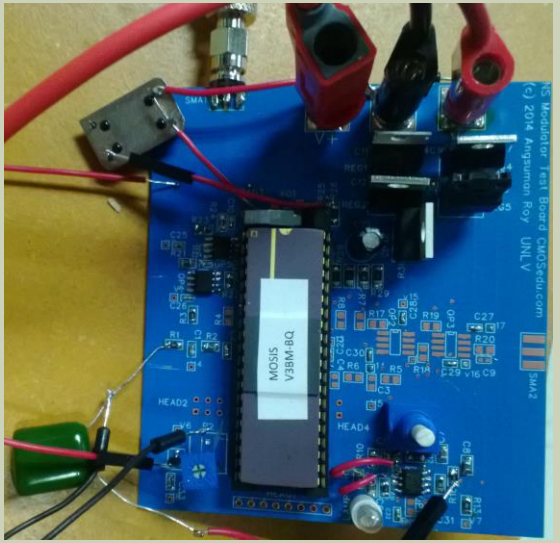
TEST SET-UP



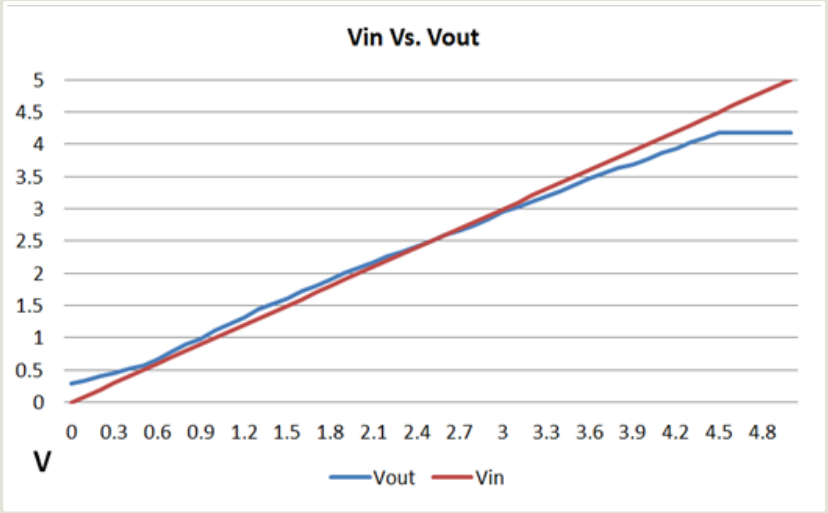
"Dead-bug" Test Set-up



PCB Test Set-up

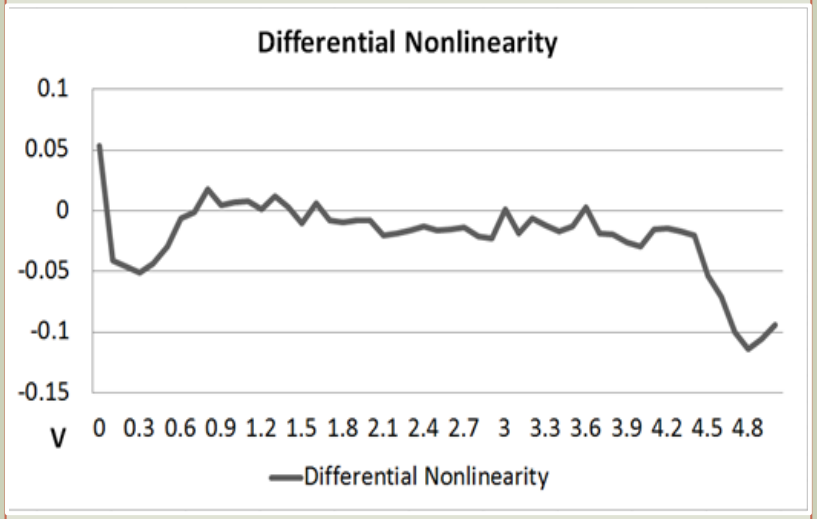


MEASURED DC TEST RESULTS



DC Transfer

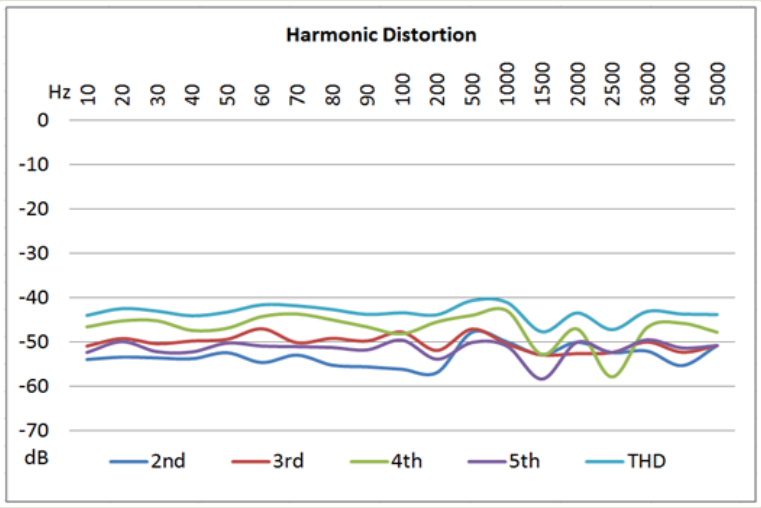
Input and output voltages were compared using a 6.5 digit multimeter.



% Differential Nonlinearity

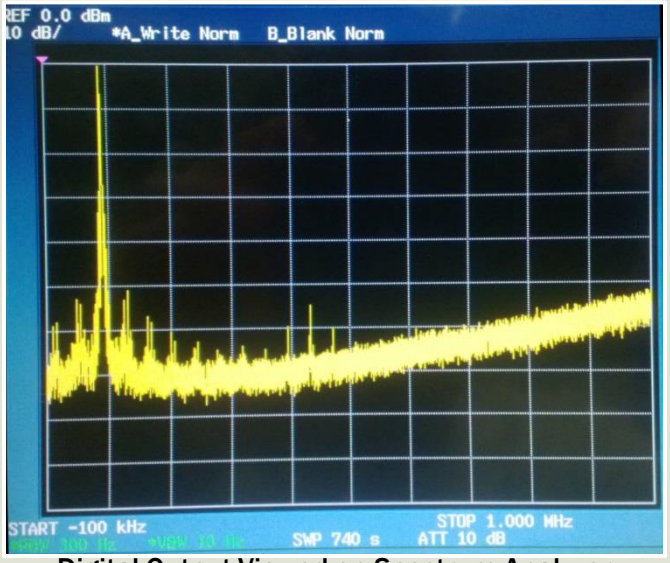
Significant filtering was used to make the output nearly static. DNL was calculated by dividing the measured incremental change by the ideal incremental change between data points.

MEASURED AC TEST RESULTS



Harmonic Distortion (dB Below Fundamental)

Result measured using 8-bit oscilloscope FFT function. This limits SNR to around 50 dB.



Digital Output Viewed on Spectrum Analyzer

Unfiltered digital output with 1kHz sine input. The spuriae free dynamic range is 50dB.

The noise shaping is clearly visible.

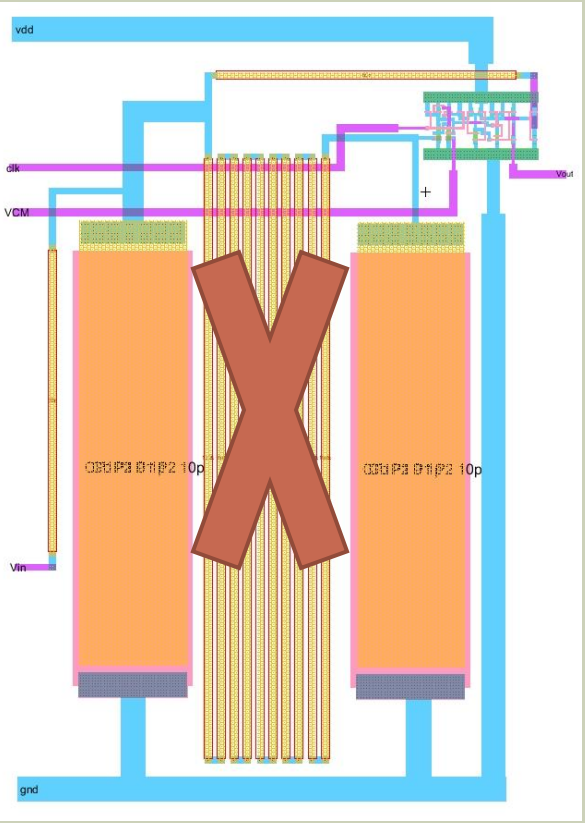
COMPARISONS TO OTHER WORKS

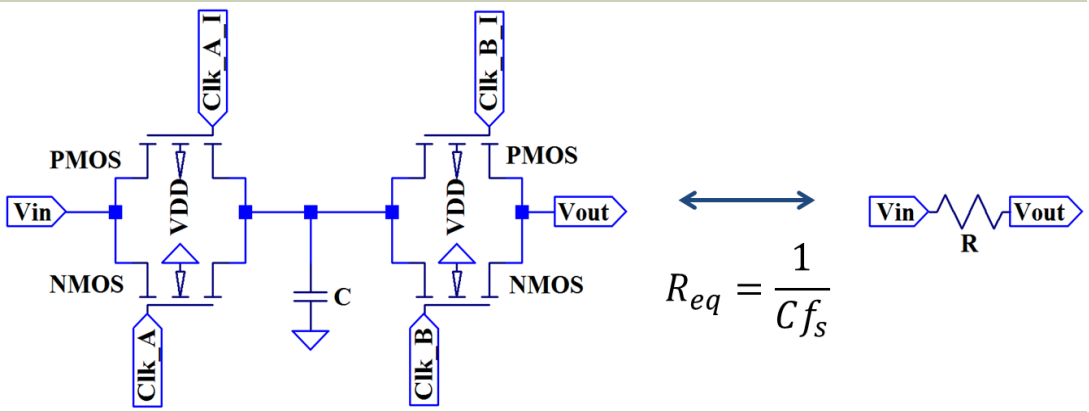
Parameter	2nd Order Passive ∑-Δ Modulator in This Work (Measured)	2nd Order Active ∑-Δ Modulator in [5] (Simulated)	2nd Order Passive∑-Δ Modulator in [2] (Simulated)
Process	500 nm	350 nm	350 nm
Resolution (ENOB)	8-bit	12-bit	10-bit
Power Consumption	100µW (typical) @5V VCC	120 µW @2V VCC	50 µW @3.3V VCC
Signal Bandwidth	5 kHz	1 kHz	4 kHz
Clock Frequency	10 MHz	320 kHz	1 MHz

[2] Guessab, S., P. Benabes, and R. Kielbasa. "Passive Delta-Sigma Modulator for Low-Power Applications," *MWSCAS '04*. (2004): 295-298.

[5] Gundel, Adnan, and Carr, William N. "A Micro Power Sigma-Delta A/D Converter in 0.35µm CMOS for Low Frequency Applications," *LISAT 2007*. (2007): 1-7.

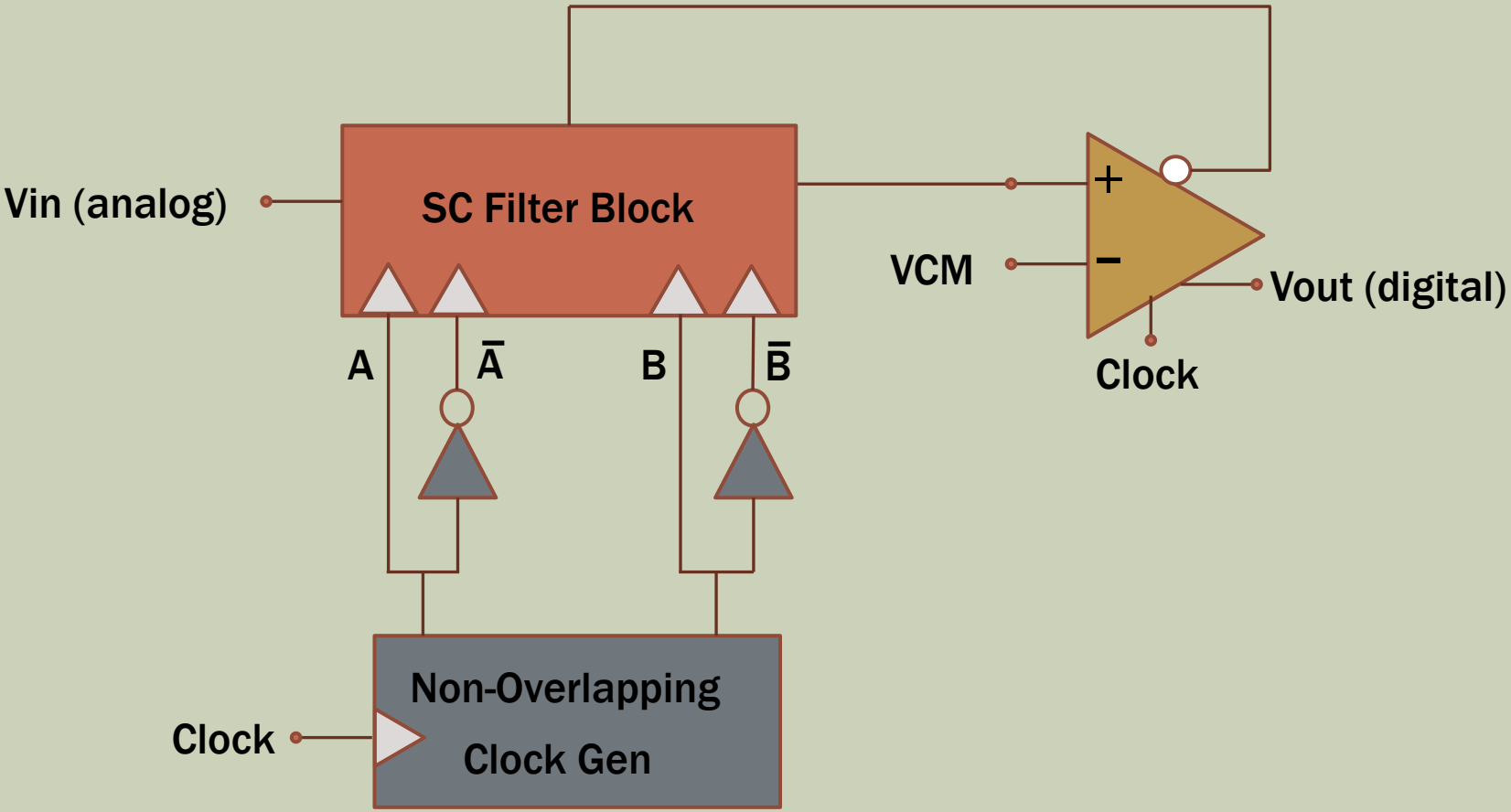
SWITCHED CAPACITOR VERSION



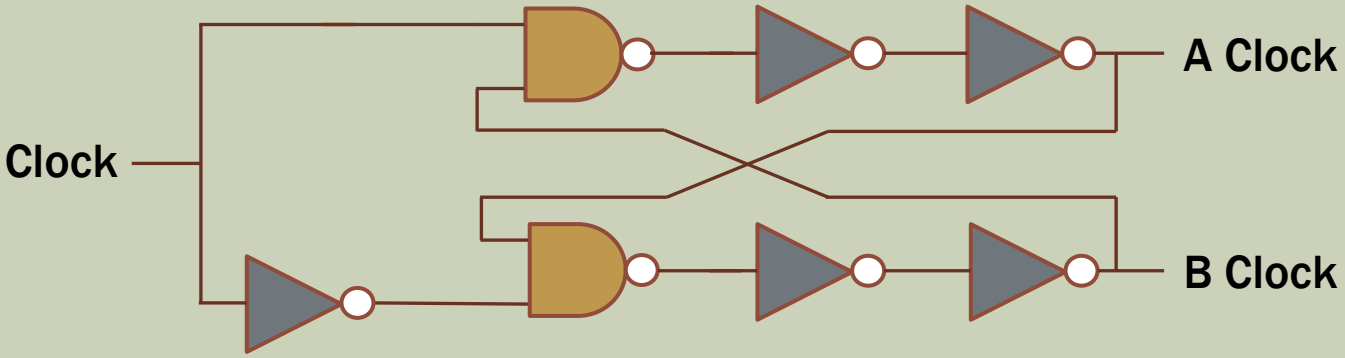


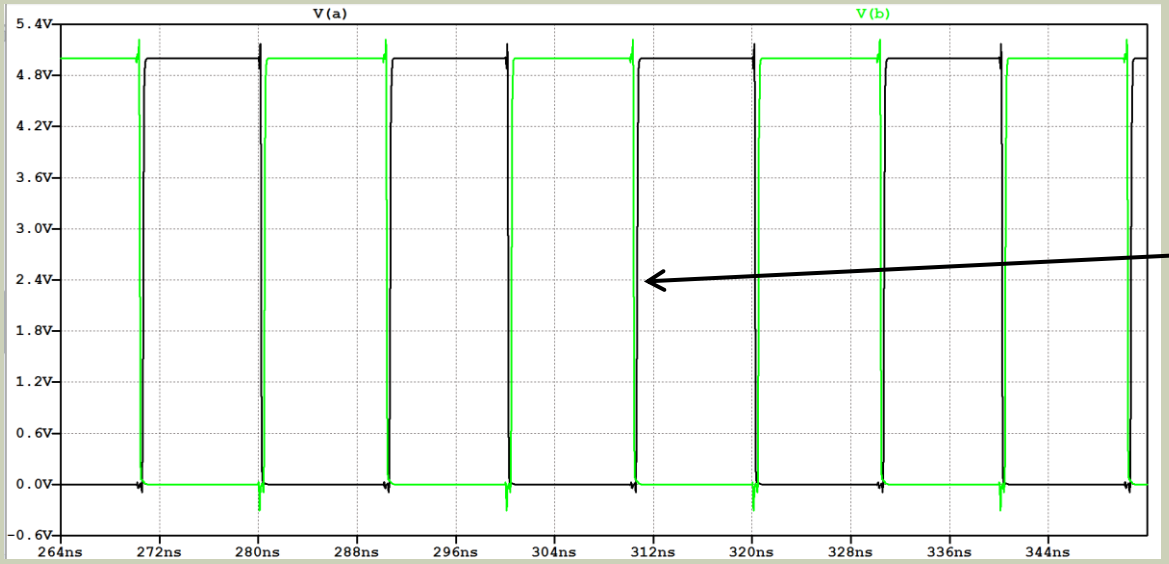
Switched capacitor resistors reduce layout area.

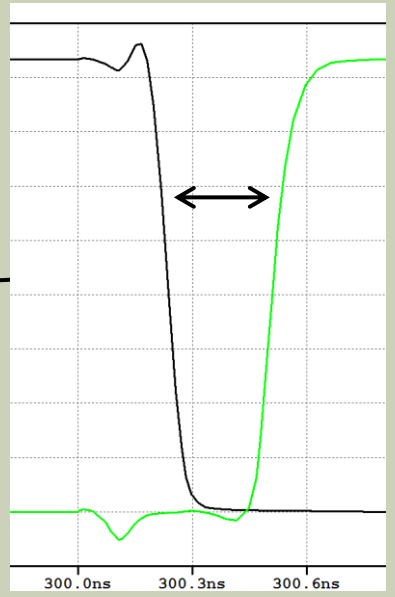
BLOCK DIAGRAM



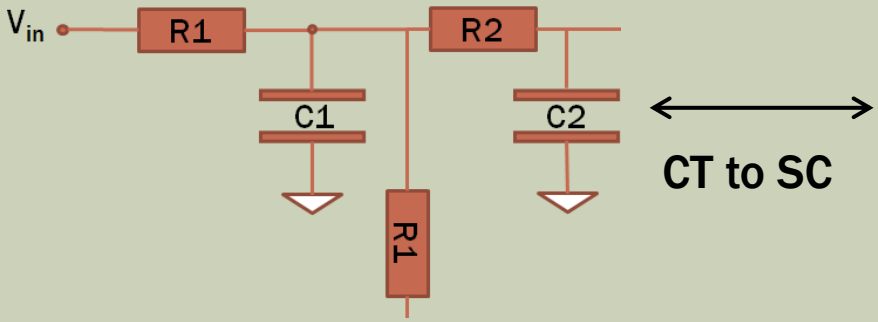
DESIGN OF NON-OVERLAPPING CLOCK GENERATOR



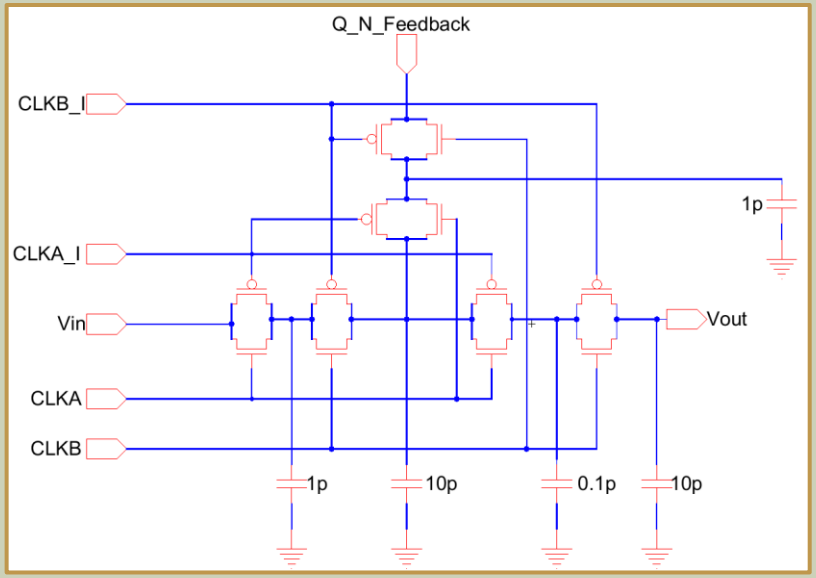




SWITCHED CAPACITOR FILTER



CT to SC



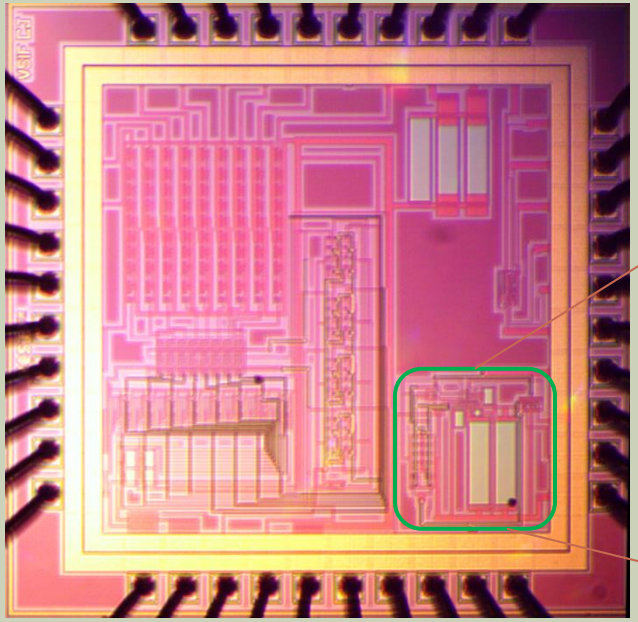
Transmission Gates Used as Switches

- NMOS and PMOS devices are minimum size
- $^{W}/_{L} = {}^{1.8u}/_{0.6u}$

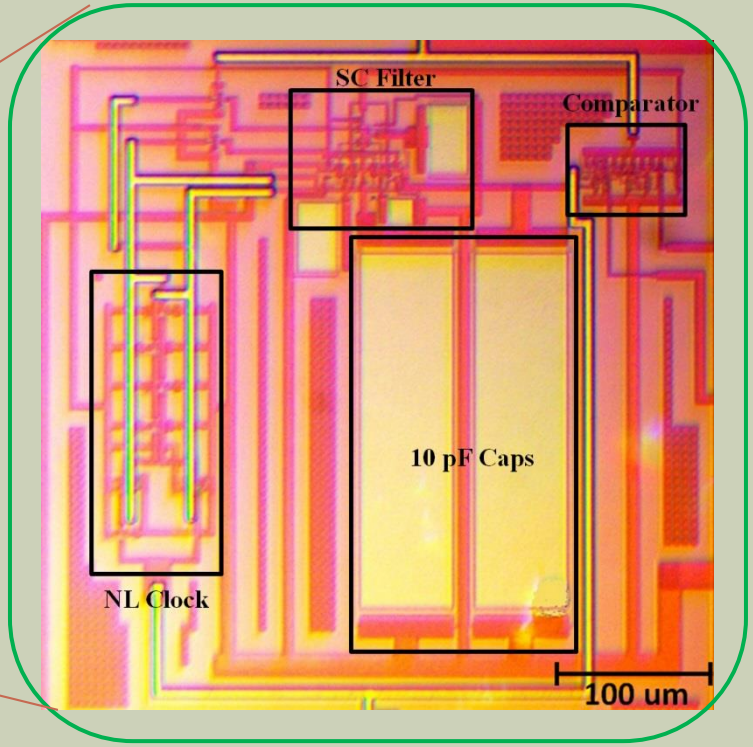
Design is Parasitic Sensitive

- Slight gain error introduced
- Trade off for lower power

FABRICATED CHIP IN 500 NM C5 PROCESS



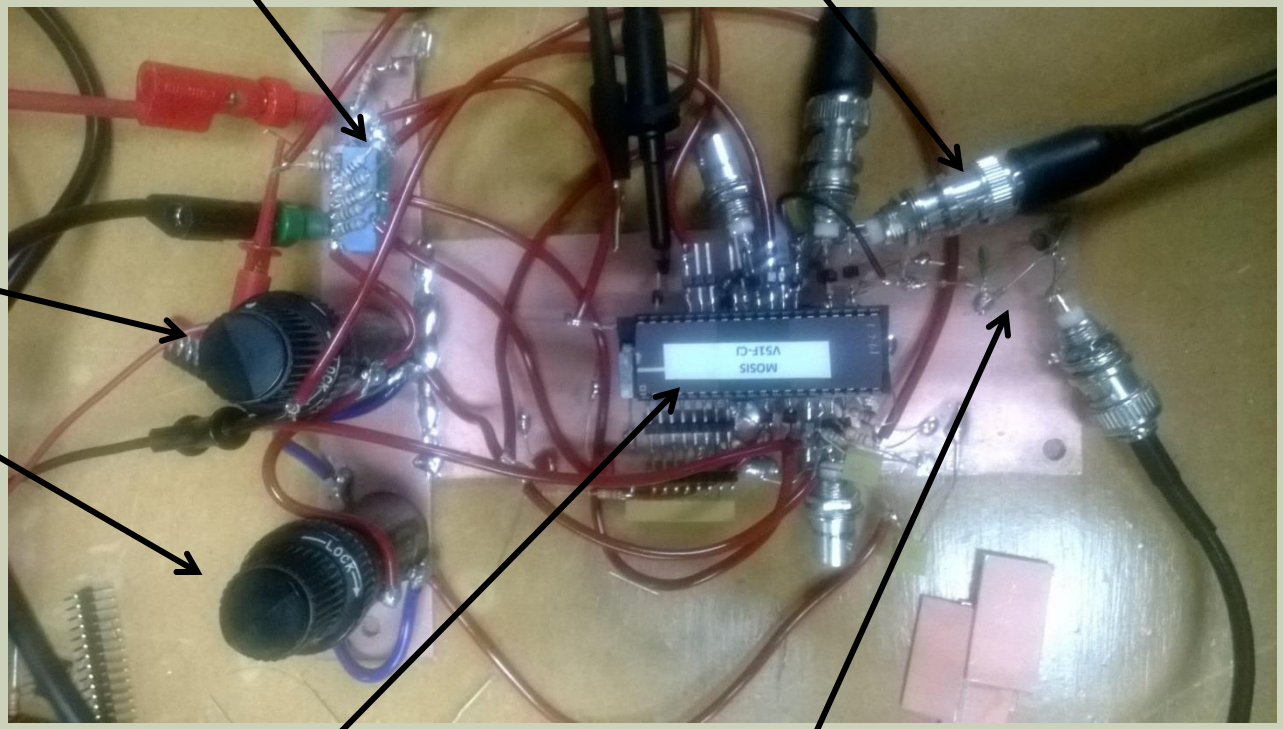
Complete Chip with
Multiple Test Structures



Proposed Σ-Δ Modulator

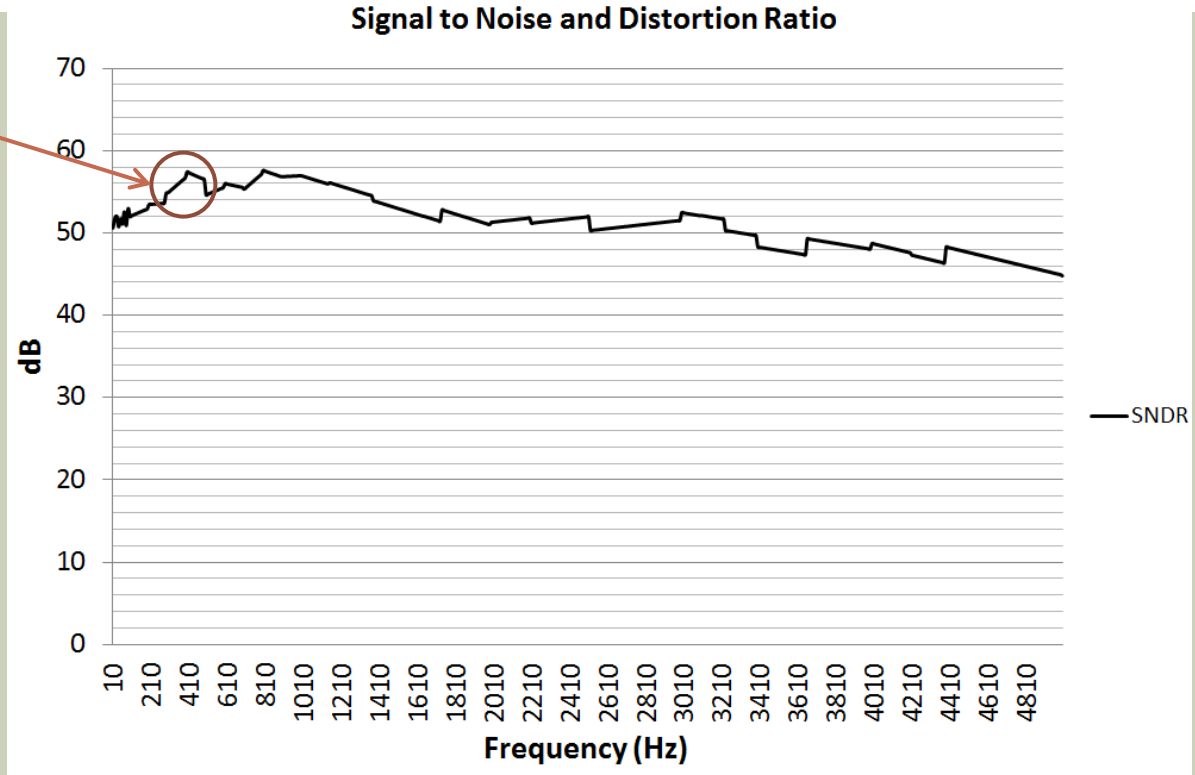
Chips were fabricated with the MOSIS service.

TEST SET-UP


Current Sense Resistors
Input/Output BNC
VCM Set
Clock Set
Chip Under Test
Passive Output Filter

TEST RESULTS

Peak SNDR of 57.6 dB



6.75 uW
2.5V VDD
2.7 uA
@ 1 MHz Clock

Test Conditions

- Digital output was filtered using a 2nd order passive RC filter.
- For each test point filter bandwidth was set to 6X input frequency.
- Clock frequency was adjusted to maintain the same OSR.

COMPARISON TO OTHER WORKS

Parameter	Proposed 2nd-Order SC ∑-Δ Modulator (this work)	2nd-Order SC ∑-Δ Modulator in [4]	3rd-Order SC ∑-Δ Modulator in [5]
Process	500 nm	90 nm	130 nm
Resolution (ENOB)	9.3 bits	10.48 bits	12.3 bits
Signal Bandwidth	3 KHz	10 KHz	20 KHz
Clock Frequency	1.024 MHz	1.28 MHz	3.2 MHz
Power Consumption	6.75 µW @ 2.5 V	17.14 µW @ 1 V	63 µW @ 0.4 V
FOM	1.78 pJ/step	0.60 pJ/step	0.31 pJ/step

[4] Hsu, C. H., Tang, K. T., "A 1V Low Power Second-Order Delta-Sigma Modulator for Biomedical Signal Application," *Engineering in Medicine and Biology Society (EMBC), 2013 35th Annual International Conference of the IEEE, pp.2008-2011,*, July 2013

[5] Yoon, Y., Choi, D., Roh, J., " A 0.4-V 63-µW 76.1-dB SNDR 20-kHz Bandwidth Delta-Sigma Modulator Using a Hybrid Switching Integrator," *IEEE Journal of Solid-State Circuits, vol. no.99, pp.1-12*

K-DELTA-1-SIGMA MODULATOR

New Sigma-Delta Modulator Topology

- First proposed in 2008
- IC implementations used active integrators

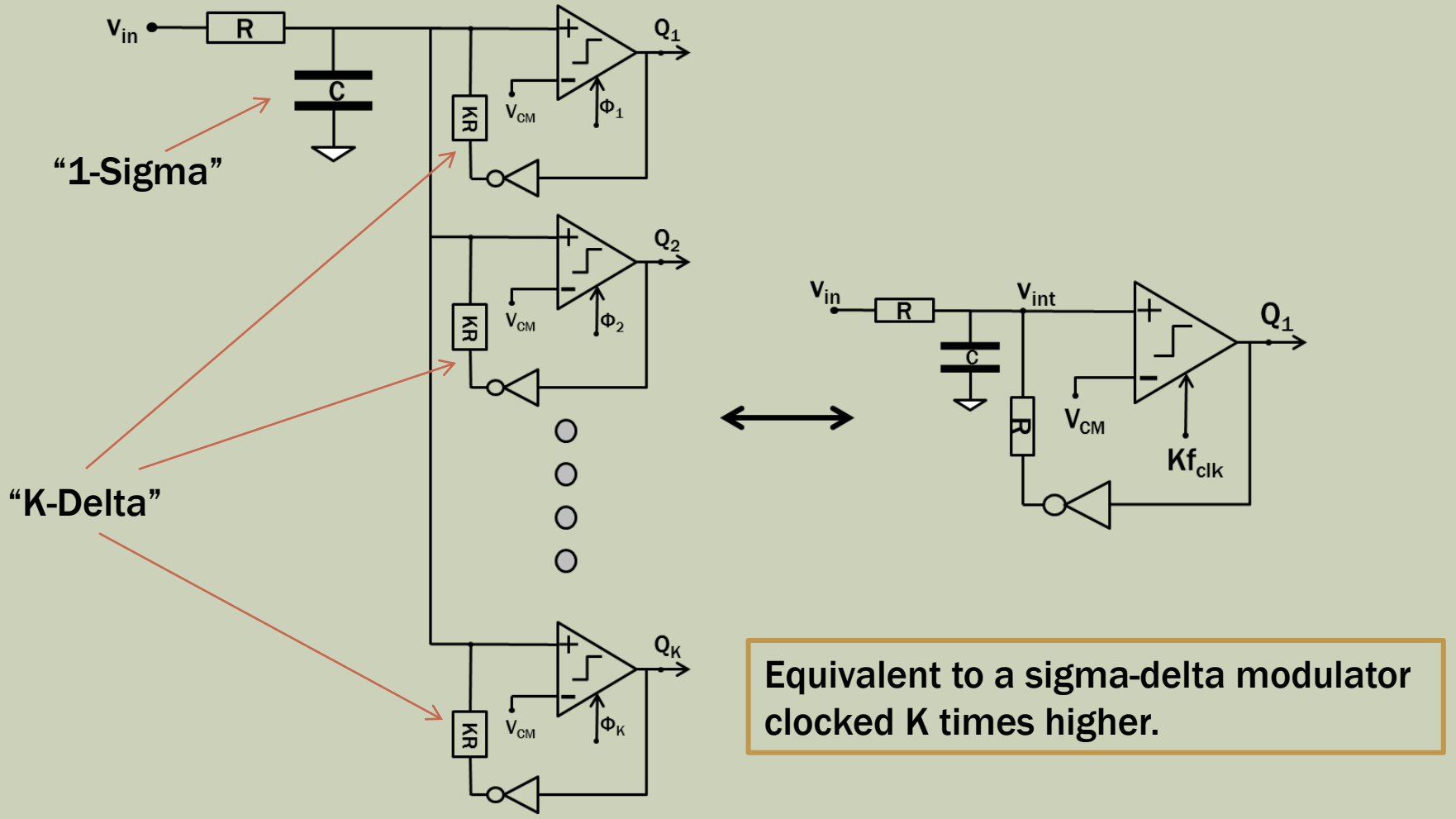
Sampling Rate > Clock Frequency

- Multiple phase shifted clocks are used to increase effective sampling rate.

Passive KD1S

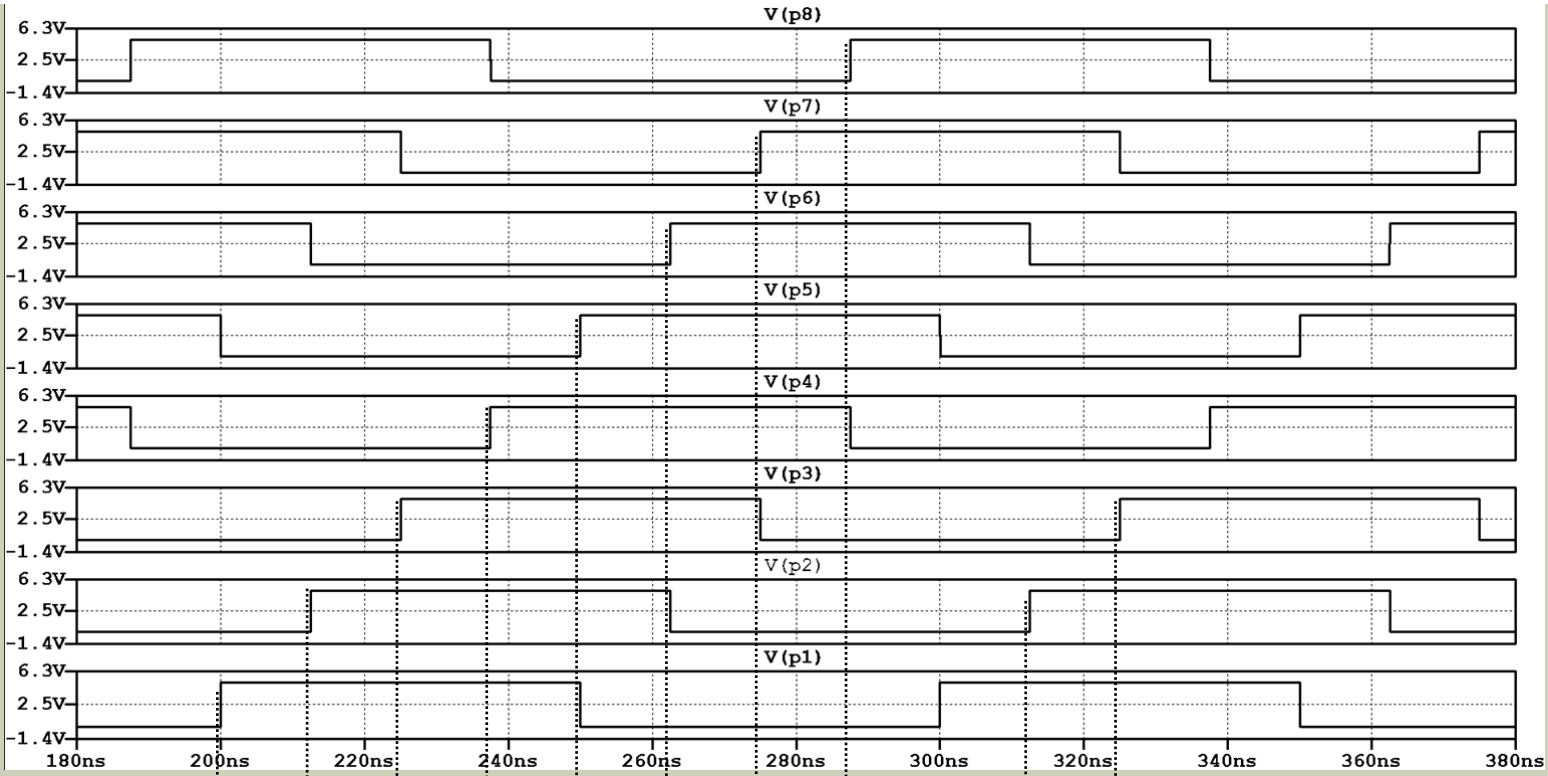
- Passive KD1S modulators are well suited for high-speed applications.

CONCEPTUAL KD1S MODULATOR



Equivalent to a sigma-delta modulator clocked K times higher.

CLOCK PHASES



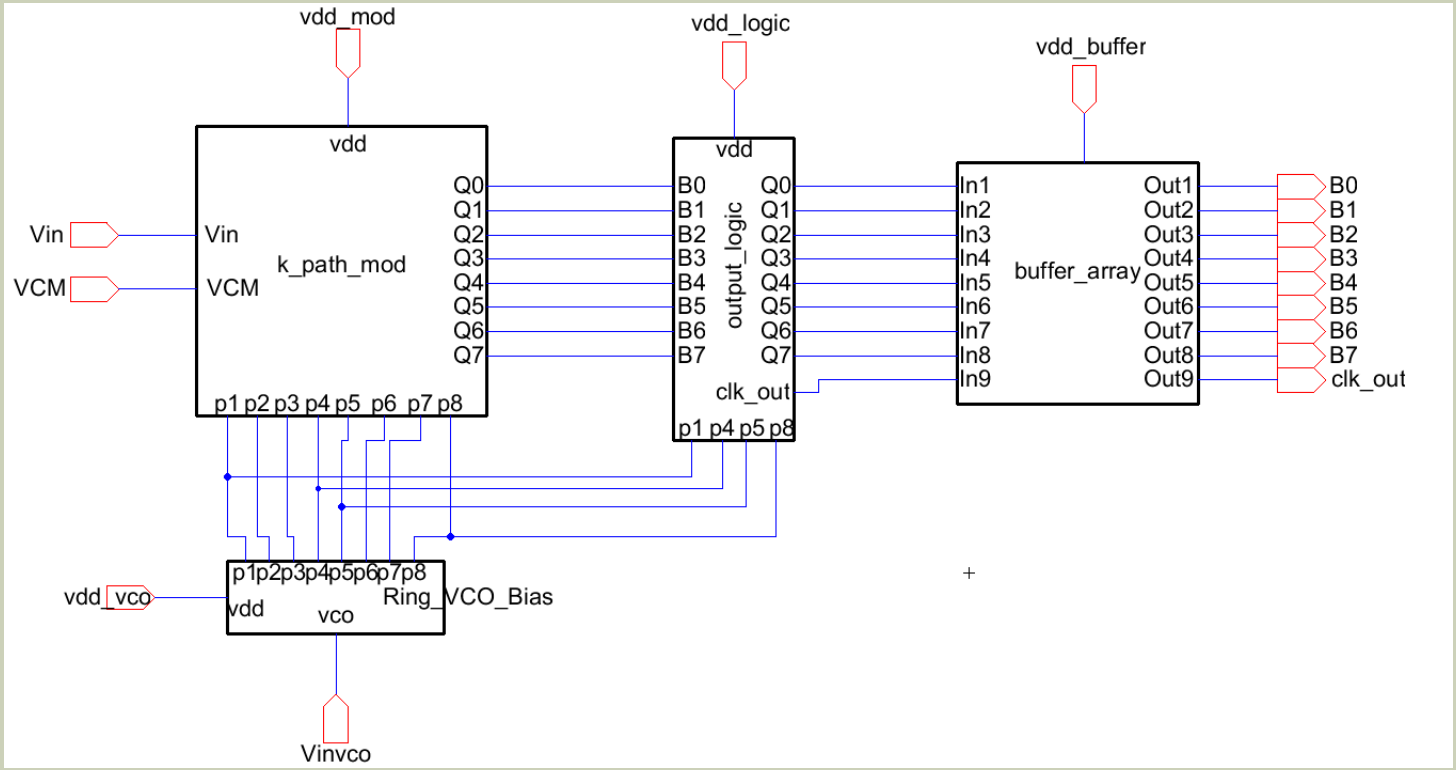
Φ_1 Φ_2 Φ_3 Φ_4 Φ_5 Φ_6 Φ_7 Φ_8

T_s

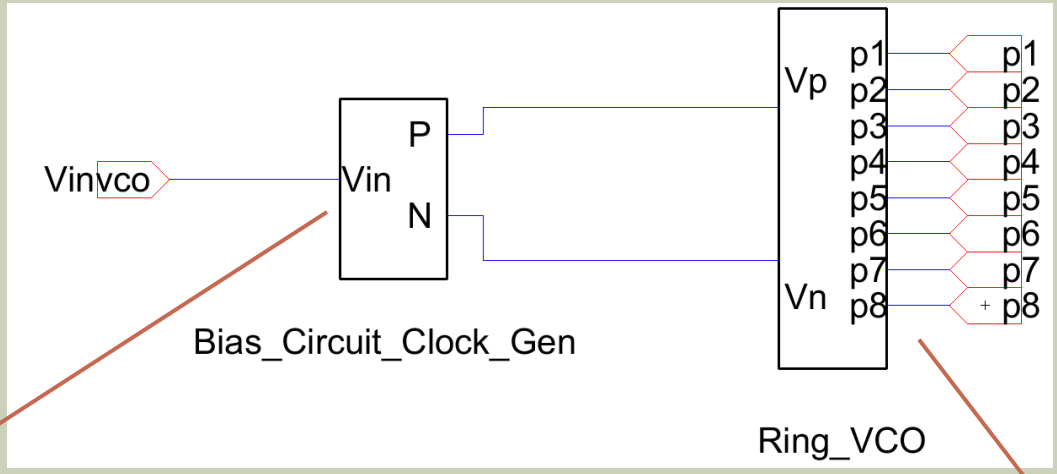
$T_s/8$

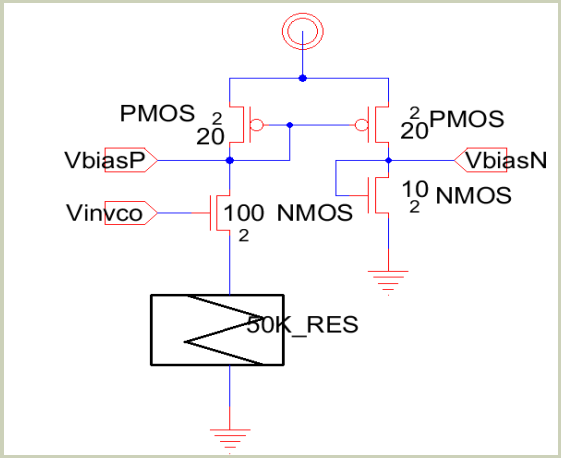
Number of rising edges in the sampling interval sets the clock frequency.

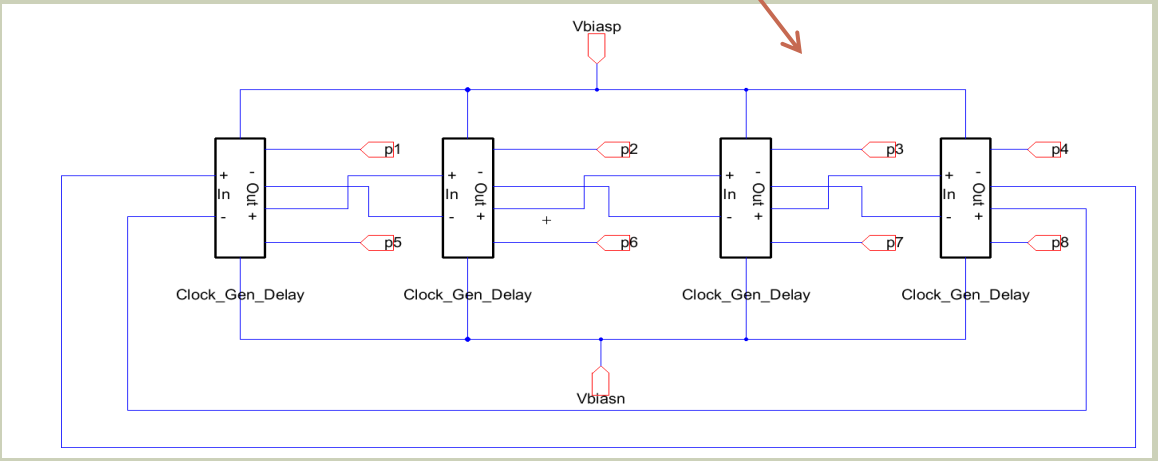
BLOCK DIAGRAM



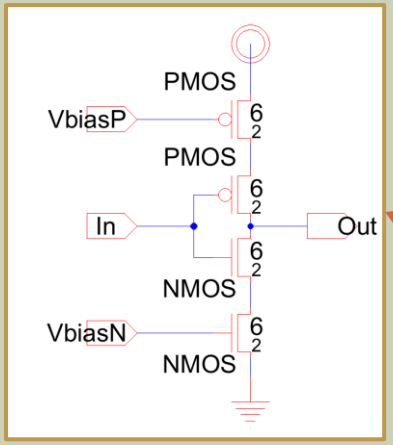
VCO

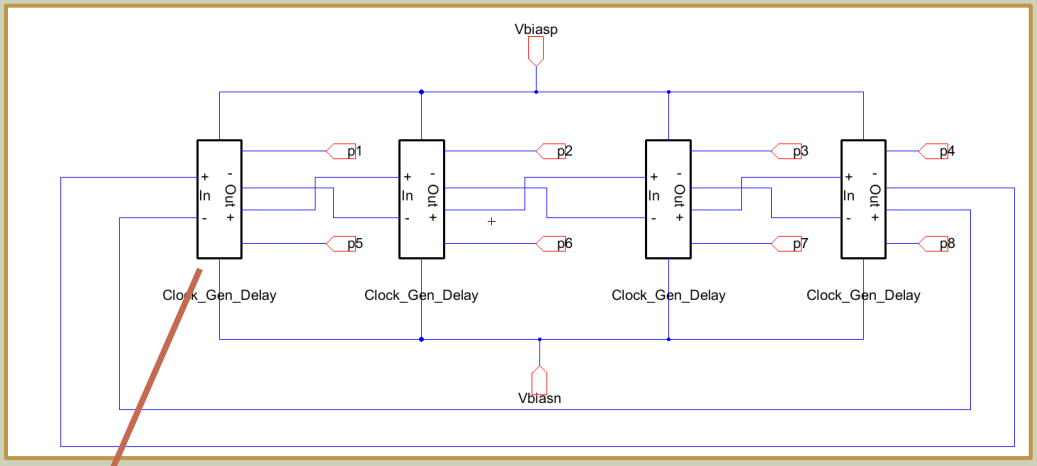

Vinvco
Vin
P
N
Bias_Circuit_Clock_Gen
Vp
Vn
p1
p2
p3
p4
p5
p6
p7
p8
Ring_VCO

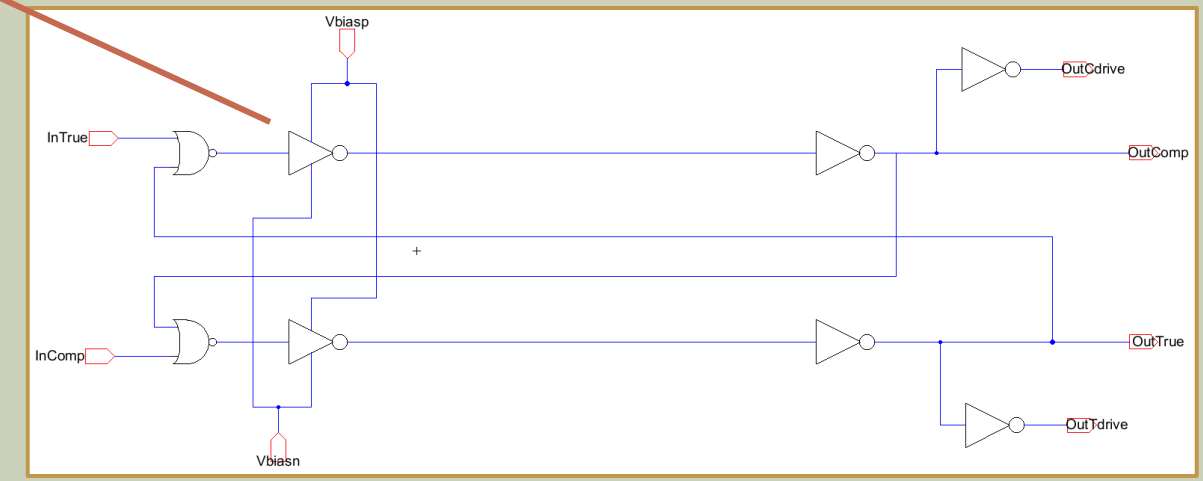

PMOS
20
2
PMOS
20
2
VbiasP
VbiasN
Vinvco
100
2
NMOS
10
2
NMOS
50K_RES


Vbiasp
In
Out
p1
p2
p3
p4
p5
p6
p7
p8
Clock_Gen_Delay
Clock_Gen_Delay
Clock_Gen_Delay
Clock_Gen_Delay
Vbiasn

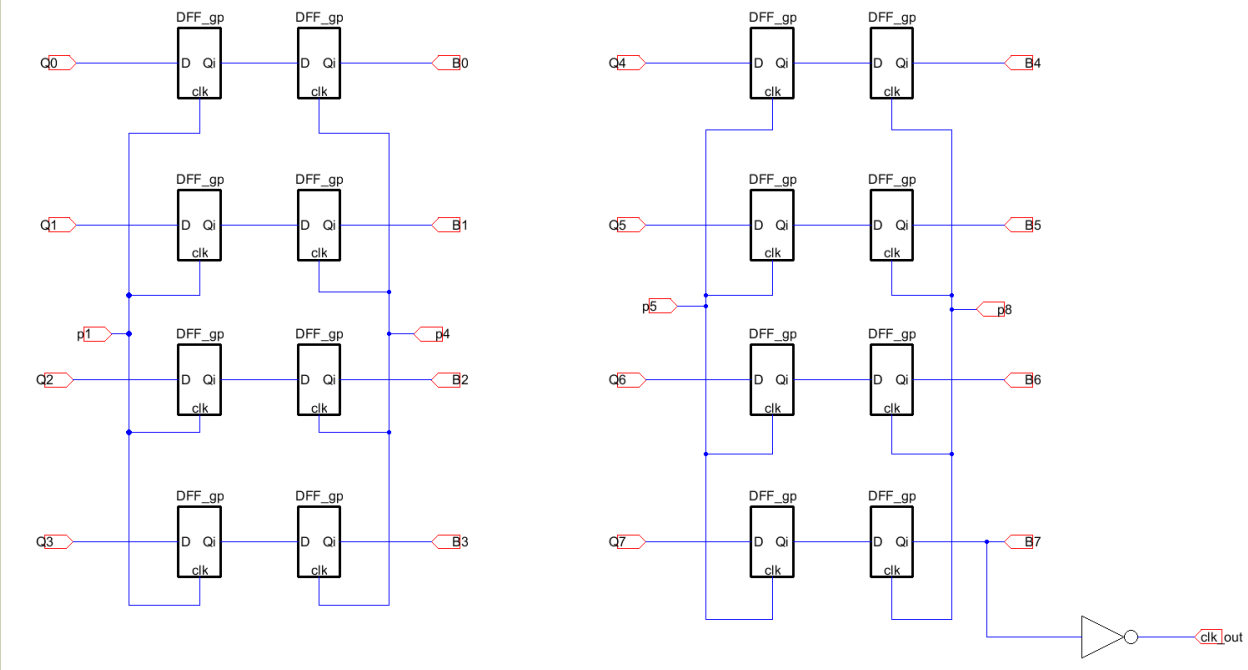
DELAY UNITS


PMOS
VbiasP
6
2
PMOS
6
2
In
Out
6
2
NMOS
VbiasN
6
2
NMOS

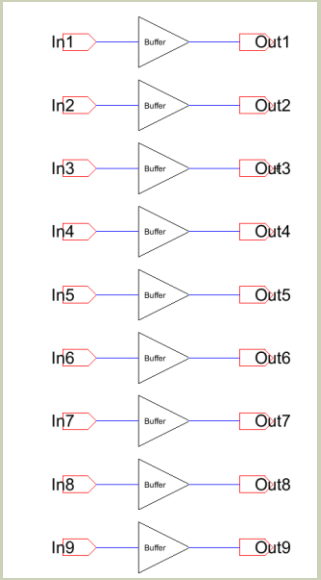

Vbiasp
p1
p2
p3
p4
In
Out
p5
p6
p7
p8
Clock_Gen_Delay
Clock_Gen_Delay
Clock_Gen_Delay
Clock_Gen_Delay
Vbiasn


Vbiasp
InTrue
InComp
OutCdrive
OutComp
OutTrue
OutTdrive
Vbiasn

REGISTERS AND BUFFERS



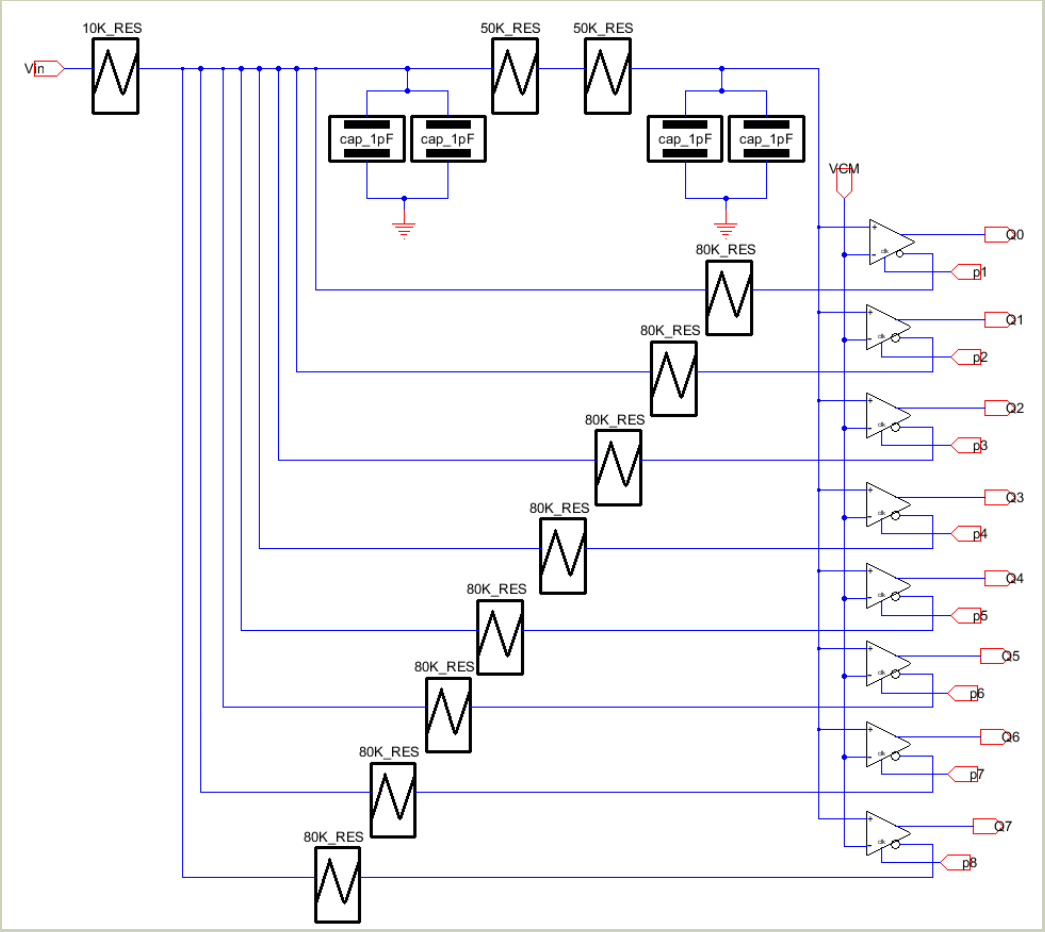
8-bit Register



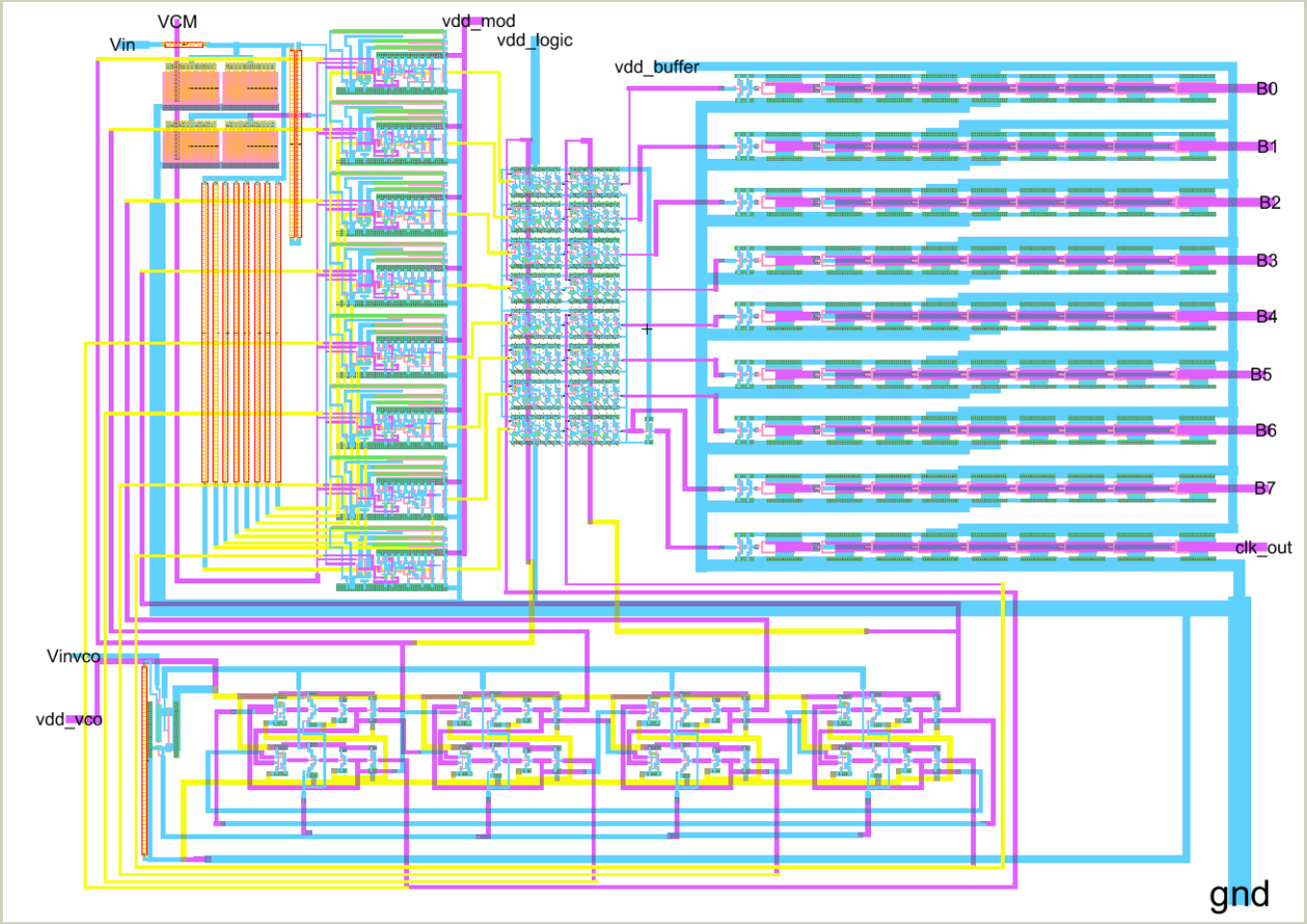
8-bit Buffer

Register is needed to reclock and resynchronize data for further processing.

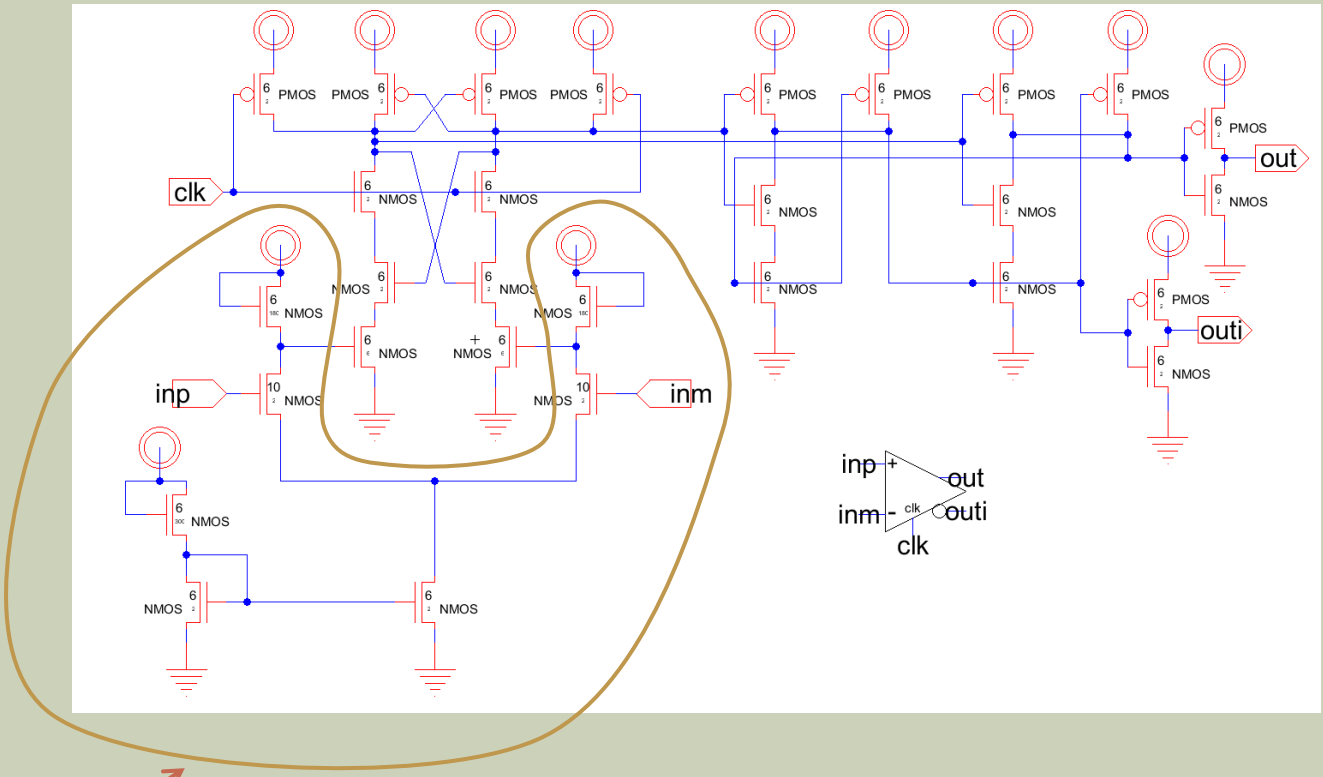
KD1S MODULATOR



LAYOUT IN ELECTRIC VLSI



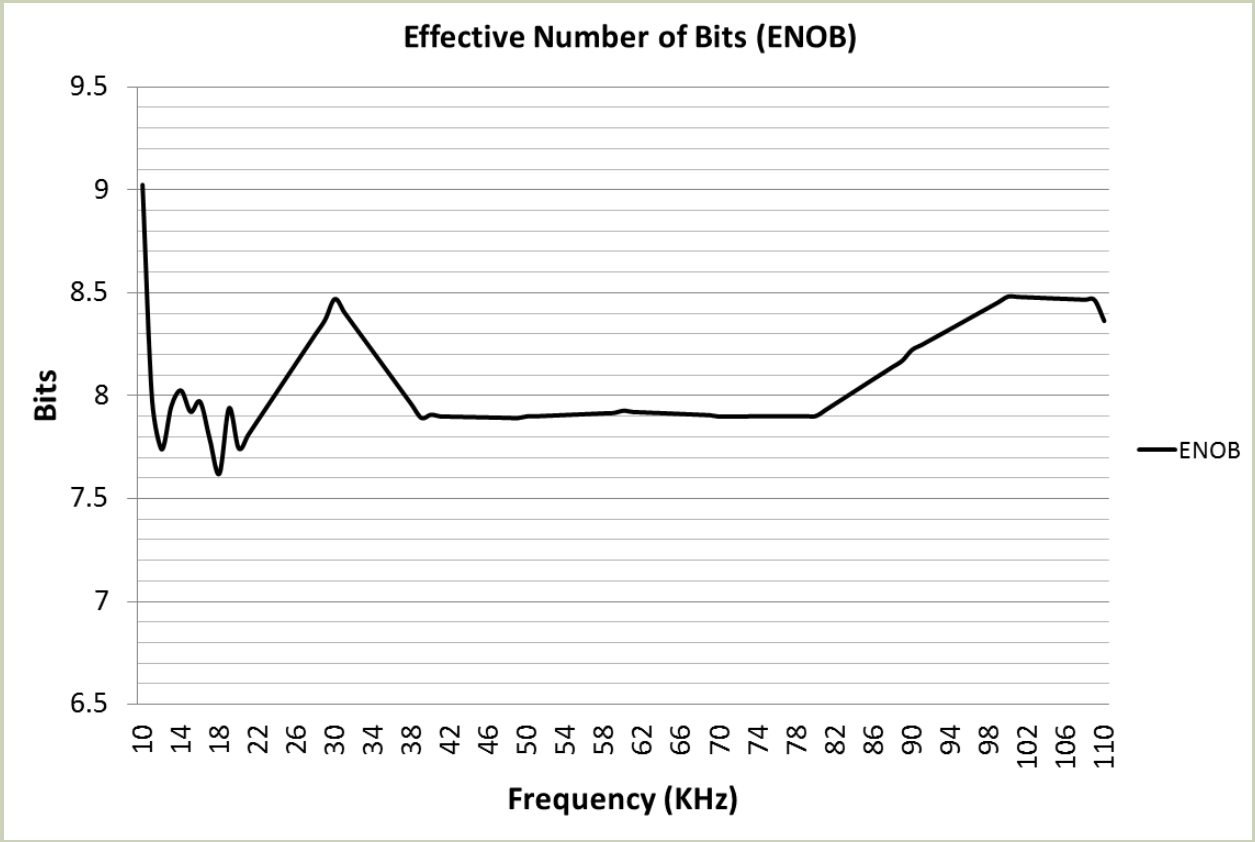
PREAMPED-COMPARATOR



Preamplifier

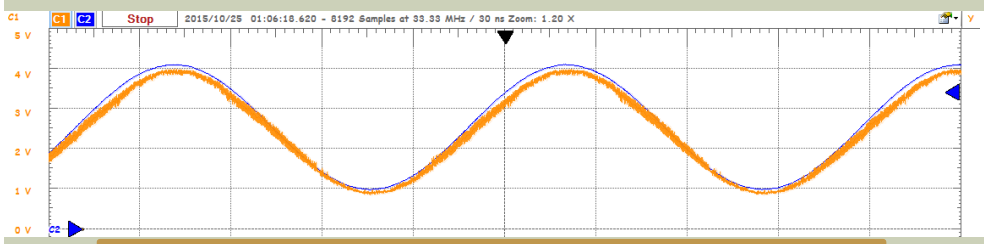
Preamplifier was added to try to increase resolution.

MEASUREMENT RESULTS

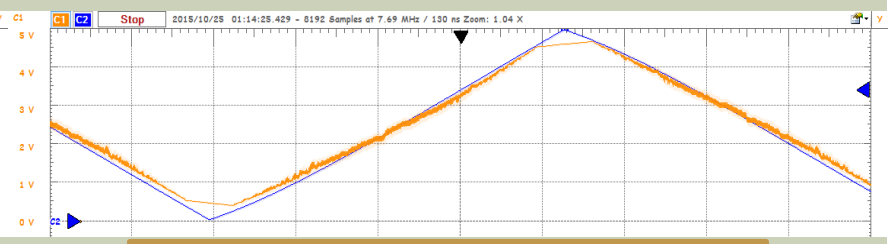


ENOB is derived from SNDR measurements.

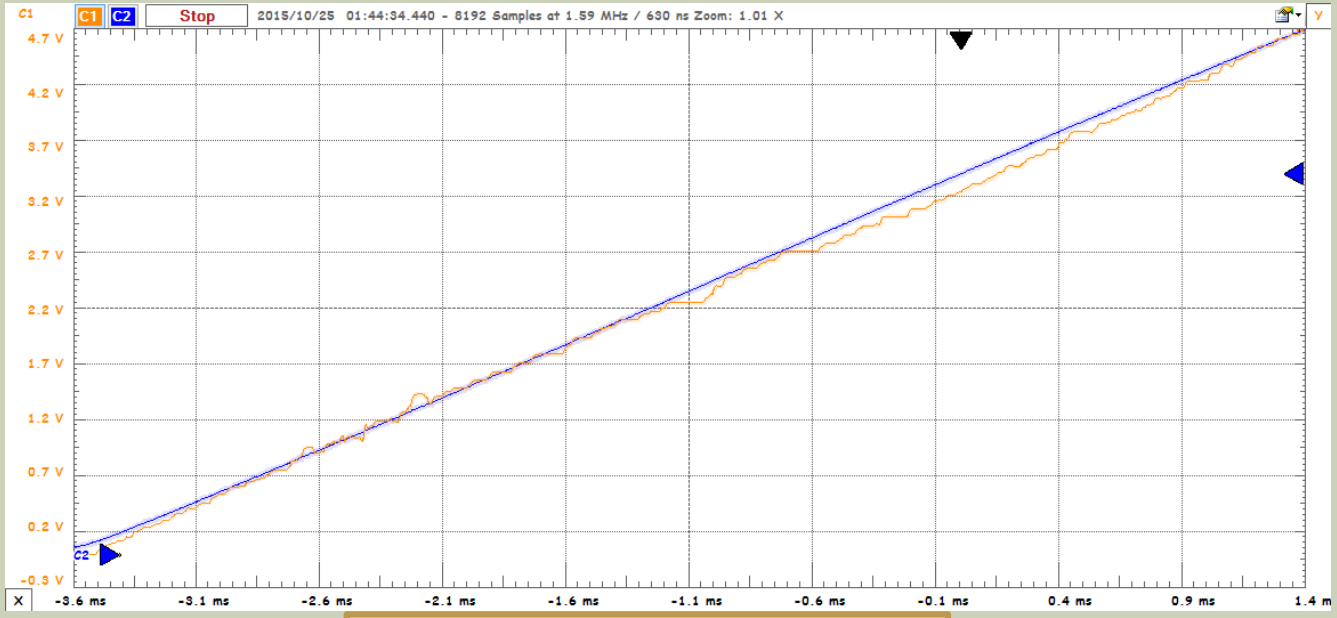
SCOPE TRACES



Sine input and reconstructed output



Ramp for testing input range



Measured transfer function

CONCLUSION

Good topology for older CMOS processes

Topology well-suited for low-power applications

Proposed topology should scale well to nm CMOS processes

Passive KD1S shows promise for future high-speed ADCs

PUBLICATIONS FROM THIS WORK

Roy, A. and Baker, R. J., "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion"
IEEE 57th Midwest Symposium on Circuits and Systems 2014

Roy, A., Meza, M., Yurgelon, J. and Baker, R.J. "An FPGA Based Passive K-Delta-1-Sigma Modulator"
IEEE 58th Midwest Symposium on Circuits and Systems 2015

Roy, A. and Baker, R. J., "A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator"
IEEE Dallas Circuits and Systems 2015