Area-Efficient Implementation of Heterogeneous Adder and its Application in FIR Filter

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Abstract **-** Arithmetic operations are widely used in various digital systems and in general arithmetic operation module such as adder is one of the significant hardware block in most digital applications which consumes much circuit area. Therefore implementation of adder with optimized area is the need of present digital applications. This paper proposes a new heterogeneous adder for reducing the complexity of hardware in the FIR filters. FIR filters are widely used in various Digital Signal Processing applications. The existing adder with varying area requirement make designers to pay a high cost ,therefore we proposed a new adder architecture, named heterogeneous adder which is further decomposed in three sub-adders consisting of ripple carry adder, carry select adder, carry look ahead adder architecture respectively. In this paper various adders performances are analyzed and then we have optimized the design of the sub-adders to form a heterogeneous adder. The proposed adder architecture is then used in FIR filters to optimize the design. The implementation and simulation results are carried out using Xilinx 14.2 software and Modelsim 10.1b.

Keywords*—DSP,FIR,Ripple carry adder(RCA), carry look ahead adder(CLA),carry save adder(CSA),VHDL simulation.*

I. INTRODUCTION

The design of area-efficient VLSI architectures need efficient arithmetic processing units which optimizes the performance parameters such as area. Adders are the key components in digital signal processing applications and and therefore it should be optimized in area as much as possible[1].The important reason for the development of area-efficient design is that many portable devices demands for smaller size due to complex hardware circuitry. Area-efficient design also plays an important role in high performance integrated circuits, by making the chip size smaller and reducing the cost and weight making the devices handy[1].In this paper we have proposed a cost effective optimization of various adder architectures[2].Addition is an important part in digital hardware systems and various adders like Ripple carry adder, carry select adder and carry look ahead adder has been concatenated to form the heterogeneous adder which is efficient in area as compared to the carry look ahead adders [2].

Then we have used this heterogeneous adder in the FIR filters. FIR filters are widely used in digital signal processing applications. Various research has previously lined out the efficient architectures for DSP functions such as finite impulse response filters which are extensively used in digital communications biomedical signal processing and many other due to its linearity and stability. Only limitation offer by it is large amount of area required to cover the number of taps to get the desired frequency response which leads to area complexit.[3]In some research multipliers are replaced by adders in preprocessing and post-processing blocks because adders weigh less in terms of area therefore length of filter is reduced[4][5].We have made the FIR filter area efficient by replacing existing adder with the heterogeneous adder and therefore area is optimized.

II. PROPOSED HETEROGENEOUS ADDER

The proposed 18-bit heterogeneous adder has been formed by concatenating sub-adders[6] , namely

1. 4-bit ripple carry adder(RCA) Architecture
2. 4-bit Carry select adder(CSA) Architecture
3. 10-bit carry look ahead adder(CLA) Architecture

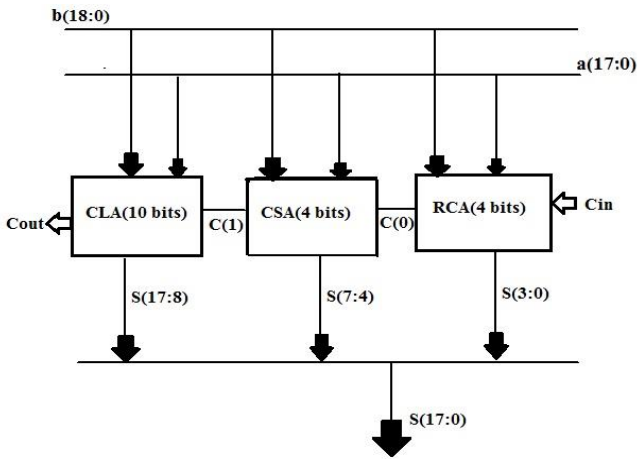


Fig. 1: 18-bit Heterogeneous adder

The order of all the sub-adders has an impact on the performance of a heterogeneous adder. The proposed adder architecture named heterogeneous adder decomposes an adder into sub-adders which makes use of carry propagation schemes of different types and for different precision [2]. The flexibility in selecting the features of sub-adders is the basis in achieving adder designs with desirable characteristics. The heterogeneous adder can be described as an n-bit adder where

various bit width blocks of carry propagation adders such as RCA, CSA and CLA are connected iteratively using carry-in and carry-out signals.

We shall now discuss each sub-adder in detail.

A. Ripple Carry Adder (RCA)

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is a **Ripple Carry Adder**, since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder. The block diagram of 4-bit Ripple Carry Adder is shown here below -

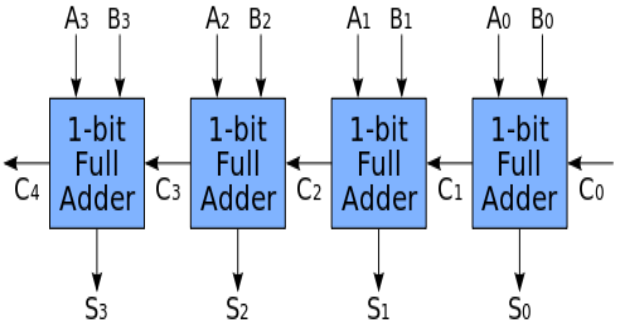


Fig. 2 4-bit Ripple Carry Adder

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

B. Carry Select Adder(CSA)

The carry-select adder generally consists of two ripple carry adder and multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform or variable. Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

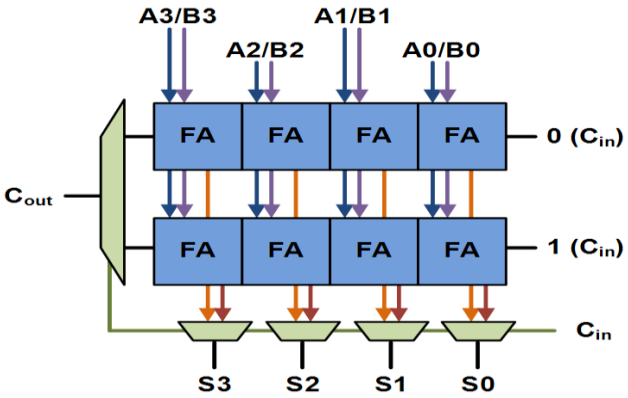


Fig. 3: 4-bit Carry Select Adder

C. Carry Look Ahead adder(CLA)

Carry look ahead logic uses the concepts of generate and propagate carry. In the context of a carry lookahead adder, it generate and propagate a binary addition. There will be a carry propagation if OR operation is performed for that either one of the input is one or input carry also be 1. For carry generation there should be AND operation for that both the inputs should be 1.

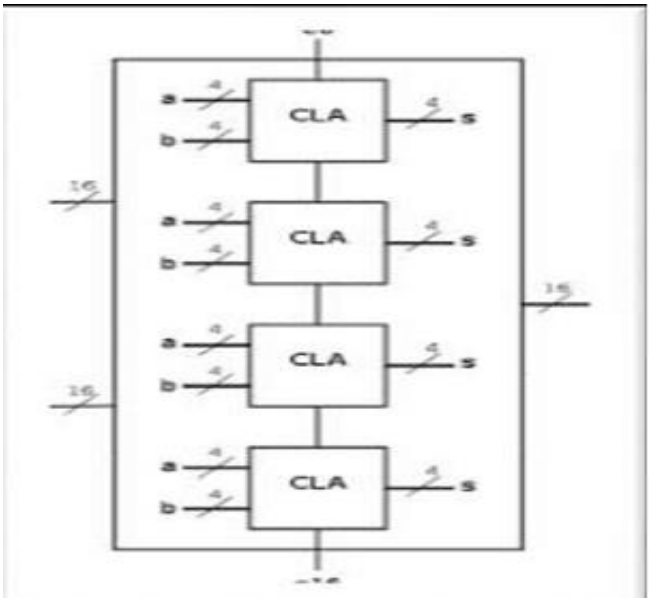


Fig.4: Design of multiple bit CLA section

Generate and propagate can be represented by the following Boolean equation:
Pi = xi or yi --Carry Propagation
Gi = xi and yi --Carry Generate
Ci+1 = Gi or (Pi and Ci)--Next Carry

$$Cout = A \bullet B + A \bullet C + B \bullet C$$

$$Cout = \underbrace{A \bullet B}_{\text{Carry Generate}} + \underbrace{(A + B) \bullet C}_{\text{Carry Propagate}}$$

Fig.5: Equations for carry generate and carry propagate

In order to get optimized result in terms of area utilization these three adders are combined to form a single adder of different bit size. The ripple carry adder, the most basic of flavors, is at the one extreme of this spectrum with the least amount of CLBs but the highest delay. The carry select adder on the other hand, is at the opposite corner since it has the lowest delay (half that of the ripple carry's) but with a larger area required to compensate for this time gain. Finally, the carry look-ahead is middle ground.

III. IMPLENTATION OF FIR FILTER USING HETEROGENEOUS ADDER

The implementation of FIR filter is then done using this area- efficient heterogeneous adder in which the three sub-adders are used. FIR filter makes use of this optimized design of heterogeneous adder in order to reduce the complexity of the hardware circuit. The issue of high cost has been solved by the newly generated heterogeneous adder and thus add up more flexibility [7].

The adders studied have their own benefits and limitations with respect to the performance parameters e.g. implementing ripple carry adder utilizes less area but at the cost of large delay, whereas carry-look ahead adder gives delay efficient design but at the cost of large amount of chip area requirement [6].therefore for efficient design various hybrid architectures were proposed by adopting a carry and sum generating scheme.

In this paper we have proposed a new heterogeneous adder which is then implemented in FIR filter to make the circuitry area efficient. FIR filter using simple convolution technique gives the output in terms of n-bits [8].

Digital filters are typically used to modify or alter the attributes of a signal in the time or frequency domain. The most common digital filter is the linear time-invariant (LTI) filter. An LTI interacts with its input signal through a process called linear convolution, denoted by y = f * x where f is the filter's impulse response, x is the input signal, and y is the convolved output. The linear convolution process is formally defined by:

$$\mathbf{Y[n] = x[n] * f[n] = \Sigma_{k=0}\, x[n]f\,[n-k] = \Sigma_{k=0}\, f[k]x\,[n-k].}$$

LTI digital filters are generally classified as being finite impulse response (i.e., FIR), or infinite impulse response (i.e., IIR). As the name implies, an FIR filter consists of a finite number of sample values, reducing the above convolution sum to a finite sum per output sample instant. An FIR with constant coefficients is an LTI digital filter. The output of an FIR of order or length L, to an input time-series x[n], is given by a finite version of the convolution sum given in above equation.

$$y[n]=x[n]*f[n]=\sum_{k=0}^{L-1} f[k]x[n-k]$$

where f [0] ≠ 0 through f [L-1] ≠ 0 are the filter's L coefficients. They also correspond to the FIR's impulse response.[9] For LTI systems it is sometimes more convenient to express in the z-domain with

$$\mathbf{Y(z) = F(z)\, X(z),}$$

where F (z) is the FIR's transfer function defined in the z-domain by

$$F(z)=\sum_{k=0} f[z]z^{-k}$$

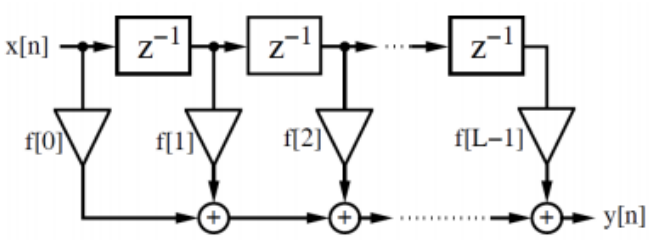


Fig.6: FIR filter in the transposed structure

The L_{th}-order LTI FIR filter is graphically interpreted in Fig.6. It can be seen to consist of a collection of a "tapped delay line," adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure [10].Thus implemented FIR filter results are shown in the simulation part.

IV. SIMULATION RESULTS

The implementation results for the heterogeneous adder are shown below with the RTL view of the heterogeneous adder. The simulation result for FIR filter using 18-bit heterogeneous adder is also shown in this paper. The implementation and simulation results are carried out using Xilinx 14.2 software and Modelsim 10.1b.

We have compared carry look ahead adder with the new 18-bit Heterogeneous adder and the simulation results shows that heterogeneous adder is more efficient in terms of area in terms of the LUTs. The proposed FIR implementation uses low cost and area efficient heterogeneous adder thereby reducing overall cost.

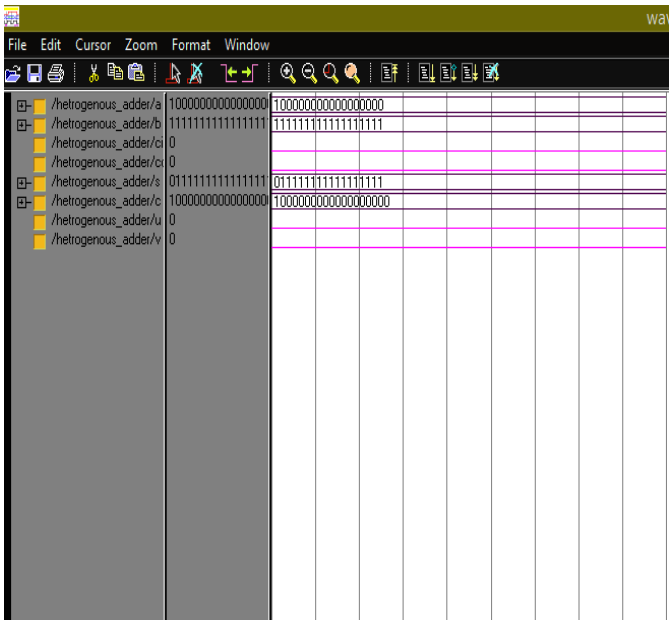


Fig. 8 Simulation Result for 18-bit Heterogeneous adder

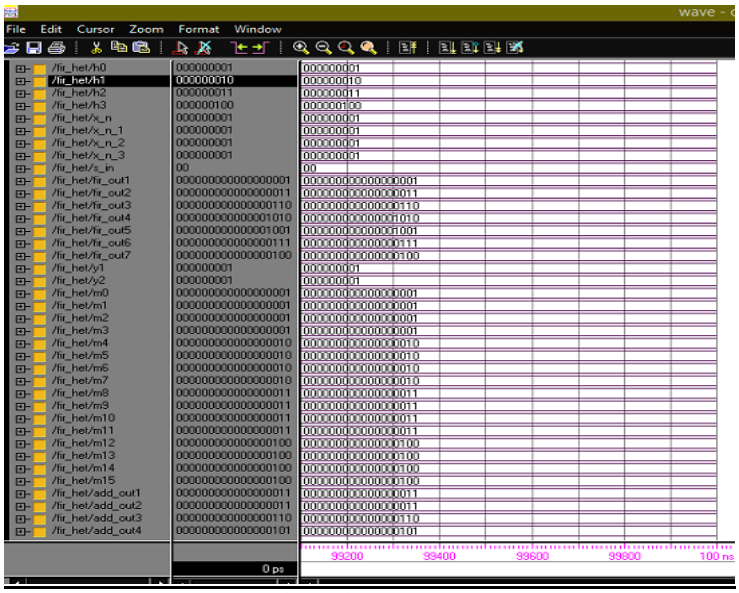
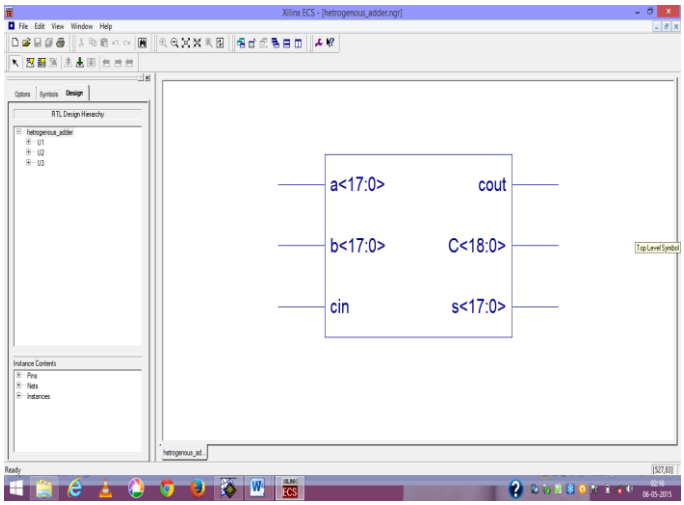
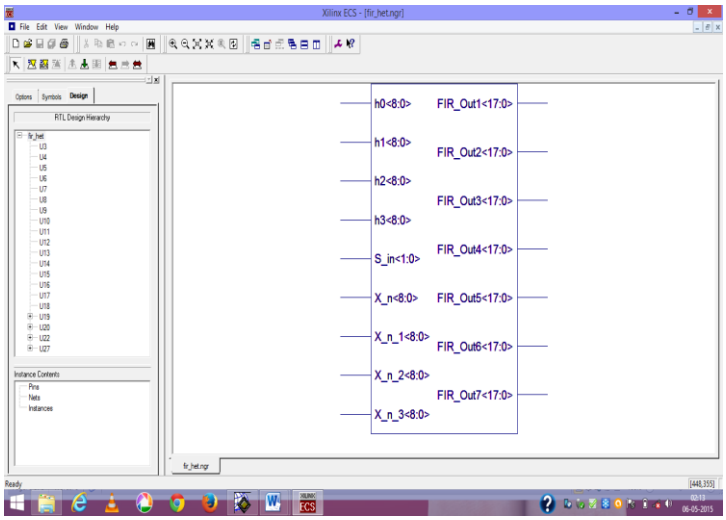


Fig. 10 Simulation result for FIR filter using Heterogeneous adder





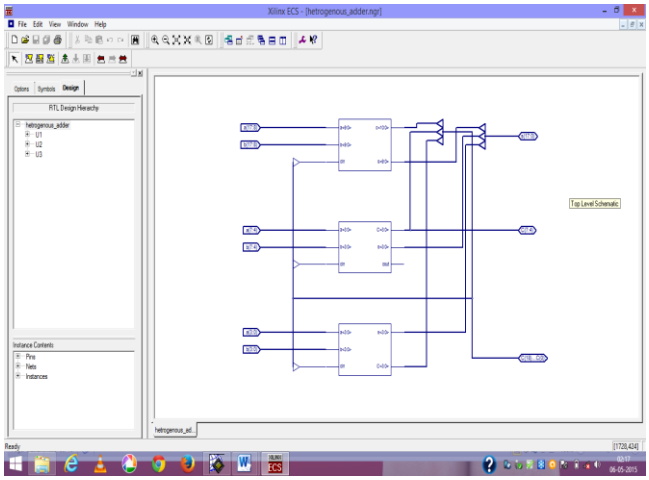


Fig. 9:RTL View for 18-bit heterogeneous adder

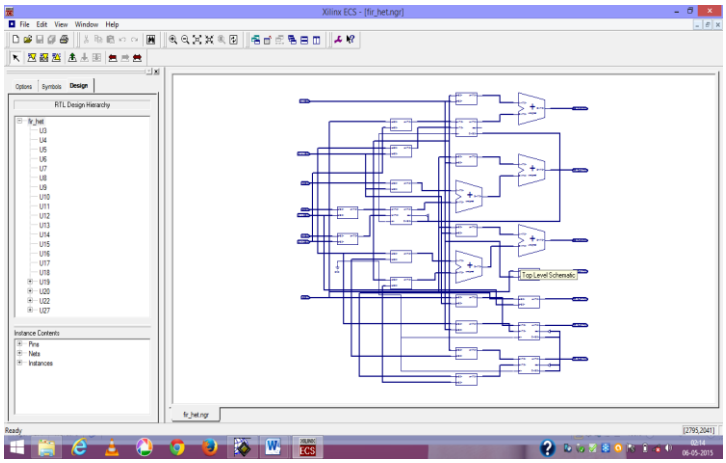


Fig. 11:RTL View for FIR Filter implementation using Heterogeneous Adder

TABLE 1: Comparison between carry look ahead and heterogeneous adder

Logic utilization	*Carry Look Ahead adder*	*Heterogeneous adder*
Number of LUTs	36	31
Number of input buffers	37	36

V. CONCLUSION

We have here proposed a heterogeneous adder which is area efficient as adders are the major portion of hardware consumption. Adders are first compared for area and it demonstrated that our approach is most effective for implementation with the constraint of low hardware cost. The area of proposed Heterogeneous adder is less when compared to Carry Look Ahead adder. To analyze trade-offs in designing digital adder, we have proposed this Heterogeneous adder architecture, which consist of sub-adders of various sizes and propagation schemes. The proposed architecture i.e Heterogeneous adder are used in FIR Filter structure which results in reducing area and cost.

ACKNOWLEDGEMENT

I, Purnima Sharma would like to thank Mrs. Monika Gupta, Assistant Professor ECE department who had been guiding me throughout the work and supporting me by giving technical and innovative ideas. I would like to thank her for motivating me to complete the work efficiently and successfully.

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