A Novel Optimization Methodology for CMOS Operational Amplifiers

[1]E.Srinivas,[2]Dr. N.Balaji,[3]Dr.L.Padma Sree
[1]Professor,Dept.of E.C.E,VNRVJIET,T.S
[2]Professor,Dept.of.E.C.E,JNTU Hyd,T.S
[3]Research Scholar,JNTUK-UCEN,A.P
([1]edem.srinivas@gmail.com)

Abstract-The main aim of the automated design methodology is to improve the design process in terms of cost, robustness and performance. An automatic design method based on a swarm intelligence approach for CMOS analog integrated circuit (IC) design is presented. The hybrid meta-heuristics optimization technique, namely, the modified particle swarm optimization algorithm (MPSO), is applied to the optimal sizing of a CMOS Two-stage op-amp , folded cascode op-amp and Telescopic op-amp. The hybrid MPSO is applied to optimize the circuit design parameters and to minimize the MOS transistor sizes which will further minimize the circuit area. The computation of the MPSO-design methodology is performed using MATLAB and CADENCE tool with 0.18µm parameters technology to verify the MPSO based design methodology.

Keywords-*MPSO;Two-stage operational amplifier;Folded operational amplifier and Telescopic operational amplifie; Circuit area Optimization.*

I. INTRODUCTION

There is an increasing need for the VLSI system to implement mixed analog-digital systems on the same chip as the complexity of the applications increases. However, despite its importance, automated design of analog component lags behind to its digital counterpart. And without the automated design, analog circuit suffers from high cost and high execution time. The automated design of analog circuit can be broadly classified into: (i) Knowledge-based and (ii) Optimization-based design. The knowledge-based design involves skill of designer to formulate design rule. The knowledge-based design takes a long time, tedious job and is only suitable to few circuit topologies. The optimization-based design involves introducing a design methodology which considered the circuit performance specifications as objective function considering various constraints. This method is highly reliable and give accurate results. Examples:- DELIGHT.SPICE [7], ASTRX/OBLX [8], IDAC [9], etc The manual design of the analog section is a more time consuming and cumbersome task; it is necessary to automate an analog circuit design. Design automation of an analog circuit increases the accuracy and reduces the design cost for final SoC design. The analog computer-aided design (CAD) tools consist of the following parts:[2]

A. circuit topology selection,
B. transistor sizing,
C. layout design.

Due to the significant attention of transistor sizing toward the chip area, this paper concentrates on circuit sizing. The analog circuit sizing tools consist of synthesis and optimization parts which are integrated. The optimization part is the crucial one compared to the synthesis part. Optimization techniques are connected with circuit design automation areas, for example, gate sizing,[3] integrated circuit yield enhancement,[4] and intellectual property (IP) core development.[5] Many previous studies for analog circuit sizing using optimization techniques focus on improving the performance of algorithms.[6] In general, an optimization algorithm can solve complex design automation problems.

The goodness and effective characteristics of the algorithm achieve the optimum solution of the Problems. A conventional optimization algorithm could not be suitable for circuit design automation because its optimum solution moves toward the local optima.[7] To overcome this issue, the simulated annealing (SA) and evolutionary algorithm (EA) were introduced to escape from the local optima. The effectiveness and goodness of these algorithms depend on the input parameters. In the case of SA, the starting point and temperature valves are carefully selected to avoid the local optima.[8] EAs depend on a heuristic evolution and the diversity of the population. In EAs, the iterative operation has been applied to improve the fitness function of the problem. Genetic algorithm [9-10] generates the optimal solution (offspring) by using crossover and mutation operators. Differential evolution algorithms also generate the offspring by using mutation and recombination operators.[11].The remaining part of this paper is organized as follows: Sec. II describes a Analog Integrated Circuit Structure and its design specifications. Sec. III presents the Proposed Modified PSO Technique For Analog Circuit Sizing method. Section IV describes the simulation results and discussion. Finally, Sec. V is the conclusion of work.

II. ANALOG INTEGRATED CIRCUIT STRUCTURE

The analog circuits consist of the transistor, parasitic capacitance, and resistor. These components are nonlinear and also more sensitive to higher order effects.[19] The main part of the analog circuit design is transistor sizing, which is more complex design step in the simulation for analog circuit is cadence tool. The simulation of integrated circuit is a powerful circuit simulation tool. Mostly the analog and mixed-signal circuit designs are verified by the cadence virtuoso simulator and also used to predict the circuit performance.[20] In the analog sizing procedure, the circuit specifications are translated into objective functions and constraint of the optimization problem. The circuit design parameters such as the transistor size and bias current are obtained from the optimization method.[21] Here, we presented an optimal design of a CMOS operational amplifiers . The hybrid MPSO used to provide the design parameters for a Operational amplifiers Circuits. These parameters should satisfy the design specifications. An optimal design of CMOS circuits has a large number of design parameters. This special kind of design procedure is required to handle the design variables. The circuit design specifications of CMOS amplifiers are considered as follows: DC Gain, Slew Rate, Transistor Area, Power Consumption,etc. For CMOS circuit design, input bias current and the transistor length and width are considered as the design variables. An objective function is developed to optimize the design variables for the circuit design. The objective function of the proposed CMOS circuits is to minimize the total size of the chip.

A. CMOS Two-Stage Operational amplifier design criteria

Two-stage circuit architecture has historically been the most popular approach for both bipolar and CMOS op-amps, where a complementary process that has reasonable n-type and p-type devices is available. When properly designed, the two-stage op-amp has a performance very close to more modern designs and is somewhat more suitable when resistive loads need to be driven. Fig 1 shows the two stage op-amp circuit as we can observe in the circuit two stages refer to the number of gain stages in the op-amp. For this we can also add a buffer stage with unity gain if needed. The output buffer is normally present only when resistive loads need to be driven. If the load is purely capacitive, then it is seldom included. The first gain stage is a differential input single ended output stage. The second gain stage is normally a common source gain stage that has an active load. Capacitor C_C is included to ensure stability when the op-amp is used with feedback. Because C_C is between the input and the output of the high gain second stage, it is often called a Miller capacitance since its effective capacitance load on the first stage is larger than its physical value. It should be noted that the first stage has an N-channel differential input pair with an N-channel current mirror active load. Two-stage Op-Amps are used for their ability to provide more gain and swing. Basically, the second stage provides about 5-15 dB gain, which is not very high. But the higher output swing provided by the second stage is crucial to some applications, especially with lower supply voltages in today's technologies. So, the second stage is a simple amplifier like a CS stage, as shown in Fig 1 below:

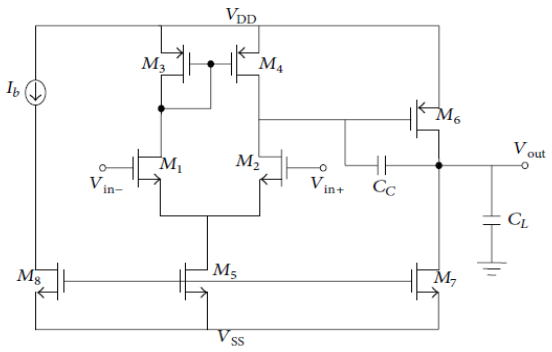

Fig.1:Two- Stage Op-Amp

Design procedure:

1) Determine I_5 from slew rate(given) and Cc(assume) I_5 = SR*(C_c)
2) Determine $V_{SD5(SAT)} = V_{SG5} - |V_{TP}| = V_{DD} - V_{G5} - |V_{TP}|$
3) Find (W/L)5 from Vsd5 and I_5, use K_n (Given)
4) Determine I_1 and I_2 which are half of I_5
5) Calculate gm1 using gm1=Cc * GBW (given)
6) Determine (W/L)1 from gm1 using standard formula $g_{m1} = \sqrt{k_n \times (\mathrm{W/L})_1 \times I_5}$ by cross multiplying
7) Calculate (W/L)1 again from positive CMR (max Vg1) and applying KVL to M1 and M5 we get $V_{SG1} = V_{DD} - V_{SD5(SAT)} - V_{G1}$ find Vsd1 (sat) and ultimately (W/L)1. Select the maximum value from step6 and step7 for (W/L)1. Now for symmetry (W/L)2 = (W/L)1
8) Determine (W/L)3 from positive ICMR spec using

$$(\mathrm{W/L})_3 = \frac{2 \times I_3}{k_n \times (V_{DS3SAT})^2} = \frac{2 \times I_3}{k_n \times (V_{G1min} - V_{SS})^2}$$

9) (W/L)3=(W/L)4 for symmetry
10) Determine (W/L)6 using Phase Margin (given) formula is

PM = 90 - $2\tan^{-1}\left(\frac{g_{m2}}{g_{m6}}\right)$ to get gm6 and from gm6 calculate (W/L)6

11) Determine I6 using I6= ((W/L)6/(W/L)3) I3 once obtained I7=I6. Using I7 and I5 calculate (W/L)7 as (W/L)7 = (I7/I5)(W/L)5

NOTE: we know (W/L)1, (W/L)2, (W/L)3, (W/L)4 (Diff amp), (W/L)5, (W/L)6, (W/L)7 (CSA) and

overall gain of op-amp is decided by these two stages. The second stage's gain is multiplied by the gain of the first stage:

$$A_{v-total} = AV1 \times AV2$$
$$= AV1 \times [g_{m1}(r_{01}//r_{03})]$$

12) Overall Gain is given as $A_{v0} = g_{m2}R_1g_{m6}R_2$

$= \frac{g_{m2}g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds7}+g_{ds6})}$

$= \frac{g_{m2}g_{m6}}{(\lambda_2+\lambda_4)I_{SD2}(\lambda_6+\lambda_7)I_{DS6}}$

Use value of Lambda. Check whether the obtained gain is same as required gain. It should be close if not equal otherwise redesign.

13) Consider that current flowing through M7 (bias transistor) is same as current flowing through M8 and six times Ids5. i.e., Ids10=30µA.

14) Calculate (W/L)8 from Ro using the formula

$$R_O = \frac{1}{g_{m8}} = \sqrt{\frac{1}{2 \times k_p \times \left(\frac{W}{L}\right)_8 \times I_{SD8}}}$$

The output stage's current should be high for the sake of speed, but, not that high to damage MOSFET devices or produce too much thermal noise. Obviously power dissipation should be kept under control too.

Parameters	Specifications
Open Loop gain	86dB
Unity Gain Frequency	5MHz
Slew rate	>5V/µs
Phase Margin	60deg
Power Consumption	≤50µW
MOS Transistor Area	100µm^2
No of iterations	20

Table 1: Specifications of Two stage opamp

B. CMOS Folded Cascode Operational Amplifier design criteria

Folded cascode amplifier offer more freedom to choose the DC input voltage at Vin, higher voltage swing, convenience in shorting the input and the output in feedback configurations. Figure 2 shows the architecture of an op-amp called folded cascode opamp. This opamp uses cascoding in the output stage combined with an unusual implementation of differential amplifier to achieve good input common mode range. Thus the folded cascode opamp exhibits self-compensation, good input common mode range and gain of two stage opamp. Figure 2 presents a basic fully differential folded cascode operational amplifier. The input stage is a differential output differential folded cascode amplifier with the transistors M1-M2. The high gain of this stage is a result of the cascode current mirrors M4-M7 and M8-M11. The NMOS devices M1 and M2 are chosen as the input differential pair because of larger transconductance compared to PMOS devices. The swing of this design is constrained by its cascoded output stage. Although only Vds,sat is needed to saturate the bottom most load transistors and the top most current source transistors, in order to allow for process variations, a small safety margin Vmargin is often added to Vds to ensure saturation. Since its second pole frequency is higher than the non dominant pole of a typical two stage topology, this design has correspondingly superior frequency response. Also because the compensation for this amplifier terminates to ground in contrast to the two stage compensation style, it has better high frequency power supply rejection ratio (PSRR).

Although, this topology consumes more power than telescopic topology due to its need for another current source (M10 and M11 act as a current source). This topology can be implemented either employing PMOS input devices or NMOS input devices. Each one has its advantages and disadvantages.

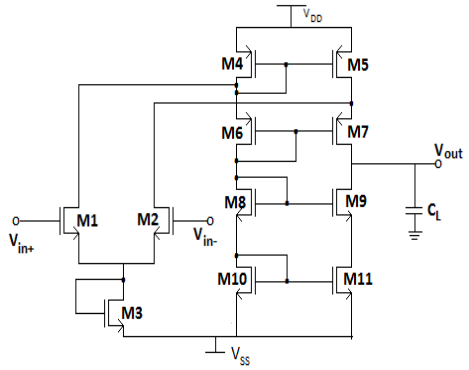

Fig.2:Folded-Cascode op-amp Using NMOS Input Devices

Design Procedure:

Step1: Calculate bias current I_{ss} and transconductance g_m

$g_m=2\pi\omega\times C_l$

$I_{ss}=S.R\times C_l$

Step2: Calculate $(w/l)_0$ from I_{ss}

$$Iss = \frac{kp}{2}(w/l)_1 (Vgs - Vt)^2$$

$(w/l)_1=(2\times I_{ss})/k_p$

Step 3: Calculate $(w/l)_7$ and $(w/l)_9$

$I_7=I_9= I_{ss}/2$

$(w/l)_7$ and $(w/l)_9=2 \times \frac{I_7}{K_p \times V_{ds}^2}$

Step 4: Calculate I_8 & I_{10} from I_{ss} and derive $(w/l)_8$ and $(w/l)_{10}$

$I_8 = I_{10}= 1.2I_{ss}$ to $1.5I_{ss}$

$V_{ds5}=V_{ds7}=(V_{dd} - V_{o(min)})/2$

$(w/l)_8 = (w/l)_{10}=2 \times \frac{I_8}{K_n \times V_{ds5}^2}$

Step 5: Calculate $(w/l)_3$& $(w/l)_6$

$$V_{ds9}=(V_{o(min)} - V_{ss})/2$$

$$(w/l)_3= (w/l)_6=2 \times \frac{I_6}{K_n \times V_{ds9}^2}$$

Step 6: Calculate $(w/l)_3$& $(w/l)_6$

$$(w/l)_3\text{& } (w/l)_6=2 \times \frac{I_5}{K_n \times V_{ds5}^2}$$

Step 7: Calculate $(w/l)_1$& $(w/l)_4$

$$(w/l)_1\text{& } (w/l)_4=\frac{gm^2}{2 \times k_n \times I_4}$$

It can be seen that voltage swing in folded-cascode topology is higher than telescopic topology by one overdrive voltage across current source (V_{Iss}). So in the circuit of Figure 2.

Parametrers	Specifications
Open Loop gain	70dB
Unity Gain Frequency	100MHz
Slew rate	>100V/µs
Phase Margin	60deg
Power Consumption	≤100µW
MOS Transistor Area	100µm^2
No of iterations	20

Table 2: Specifications of folded cascode opamp

C. CMOS Telescopic Operational Amplifier design criteria

The simplest version of a single stage Op-Amp is the telescopic architecture. The input differential pair injects the signal currents into common gate stages. Then, the circuit achieves the differential to single ended conversion with a cascode current mirror. We note that the transistors are placed one on the top of the other to create a sort of telescopic composition. Telescopic topologies are used to achieve high gain. They increase the gain by boosting output impedance of the amplifier. This structure is also called telescopic cascode configuration.

Fig 3 shows a fully differential implementation of a cascode Op-Amp. To achieve fully differential configuration current-source loads are used which at the same time will help with high gain requirement as well. It is informative to mention that diode-connected loads are used in single-ended output Operational Amplifiers' implementations and they exhibit a mirror pole introduced to the transfer function. Telescopic cascode configuration typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices, as in the case of a folded cascode. Also, the parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption.

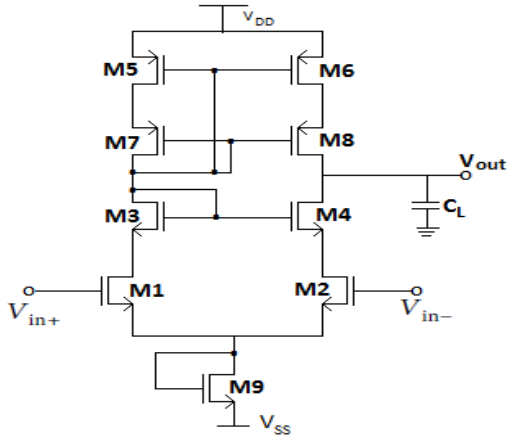

Fig 3.: Telescopic Amplifier Topology

The disadvantage of a telescopic op-amp is severely limited output swing. It is smaller than that of the folded cascode because the tail transistor directly cuts into the output swing from both sides of the output. In the telescopic op-amp shown in source M9 must have at least $V_{ds(sat)}$ to offer good common mode rejection, frequency response, Fig.3 all transistors are biased in the saturation region. Transistors M1-M2, M7-M8, and the tail current and gain.

Design Procedure:

STEP1: The first step of the design gives the estimation of the bias current,

$$2\pi f_T = \frac{2I_{ss}}{(V_{GS} - V_{TH})} \frac{1}{C_L}$$

where $I_{ss}$is the tail current.

STEP2: Design Tail transistor M9 and calculate W and L of this transistor by using the transistor in saturation .The equation used is

$$I_{ss} = \frac{\mu C_{ox}}{2} (\frac{W}{L})_9 (V_{GS} - V_{TH})^2$$

STEP 3: Calculate the bias VB2 of transistor M9 using the equation

Vb2=Vgs9-Vth

STEP 4: Design the differential pair of the circuit, by assuming both of them to be working in saturation mode. Their aspect ratios could be calculated using bias current Iss. The equation used is

$$I_{ss} = \mu C_{ox} (\frac{W}{L})_1 (V_{GS} - V_{TH})^2$$

STEP 5: Calculate the common mode voltage that allows M9 to be in saturation

$$V_{in,\,cm} >= V_{sat\,9} + V_{GS1}$$

STEP 6: Design the High Compliance Current mirror and calculate the Bias voltage that is applied to both the gates by the following equation$V_{B1} - V_2 - V_{Thn} = V_{sat3}$Where V_{B1} is the bias voltage that is applied to High Compliance current mirror, V2 is the voltage at node 2 and V_{Thn} is the threshold voltage. The aspect ratios of transistors M3 and M4can be calculated by assuming both the transistors in saturation and both are matching. The current equation is

$$I_{ss} = \mu C_{ox}(\frac{W}{L})_{3,4}(V_{GS} - V_{TH})^2$$

Where VGS = VB1 – Vsat, 2 – VTh,n

STEP 7: Design the Cascode Current Mirror stage where there are four PMOS transistors, which are identical, and the current passing through them is same as the drain and gate are tied to each other. They all are in saturation mode. The current flowing is same that was in High Compliance Current Mirror stage. The aspect ratios can be calculated by the following current equation

$$I_{ss} = \mu C_{ox}(\frac{W}{L})_{5,6,7,8}(V_{GS} - |V_{TH}|)^2$$

Where VGS = VDD – 3VTh,p

The output impedance seen from each single output node is equal to:

$$R_{out} = \left(\left[1+\left(g_{m3}+g_{mb3}\right)r_{03}\right]\times r_{01} + r_{03}\right) // \left(\left[1+\left(g_{m5}+g_{mb5}\right)r_{05}\right]\times r_{07} + r_{05}\right)$$

$$A_v = G_m \times R_{out} \approx g_{m1} \times \left[\left(g_{m3}r_{03}r_{01}\right) // \left(g_{m5}r_{05}r_{07}\right)\right]$$

As $G_m \approx g_{m1}$, then the gain can be calculated using

One of the drawbacks of this implementation is the limited output swing. Each transistor cascaded on top of another one, adds an overdrive voltage to the headroom of output branch which will limit

parameters	Specifications
Open Loop gain	50dB
Unity Gain Frequency	1000MHz
Slew rate	>100V/μs
Phase Margin	60deg
Power Consumption	≤100μW
MOS Transistor Area	100μm^2
No of iterations	20

Table 2:Specifications of telescopic opamp

III. PROPOSED MODIFIED PSO TECHNIQUE FOR ANALOG CIRCUIT SIZING

A. Particle Swarm Optimization

Particle swarm optimization is a metaheuristic optimization technique given by Doctor Kennedy and Eberhart in 1995[1].It iteratively improves a solution by keeping track of its quality for optimizing a problem. The basic idea behind this algorithm is behavior of flock of birds and school of fish and their movement. Like other optimization techniques such as Genetic Algorithm (GA), Ant Colony Optimization (ACO) etc [2] [3],PSO is also a swarm intelligence algorithm in which the entire focus is given on the swarm instead of simply looking for a single creature. Birds or fish usually move either in a scattered way on in a group in search of their pray. It is well known that birds are very much perceptible of the places where they can find their food. Birds can smell their food from a far place. So, while movement every bird smells regarding the food. The moment a bird gets smell of food, it will move towards that direction while communicating about this to the other members of their flock especially when they got some good information regarding the place and direction of food. Higher the number of birds moving towards any specific direction tells about higher probability of a food item in that direction. Using this method bird finds their food. Same method is being used for the implementation of PSO. In place of a swarm of birds we are assuming a population of particles or swarm of solution. Movement of a bird is assumed as moving a particle or solution in the given boundary using some factors. Bird share their information locally as well as globally same is implemented using a position updating equation given in equation 2. It is not necessary that all the birds moving in the space will surely get a food particle hence every bird's information is not of same importance so the most optimist information will be their food. In PSO also, each iterations leads to some information regarding the solution to the given problem but those are not the most appropriate one. Among those solutions the most optimist solution is searched using co-operation from other particles or solutions socially as well as globally to get the overall solution of the problem. This method can be used to solve many complex problems such as Travelling Salesman Problem (TSP) [4], for training Artificial Neural Networks (ANN) [5], etc.

The Particle Swarm Optimization (PSO) is a kind of multiagent parallel search algorithm for searching optimized solution by simulating the movement of birds in their swarm in to computational environment. This algorithm assumes that each bird which is simulated as a particle has a potential solution for solving the given problem. Each particle is allowed to fly through the entire search space. For changing their position a velocity is given to the particle and their new

position is updated using their previous position and velocity using equation 1 and 2. The algorithms starts with initialization of particles in the given search space randomly. After initialization all particles are allowed to roam in the search space with a velocity assigned to them. This velocity is being used by the particle to update its position and for finding their personal best position (***pbest***) and the global best position (***gbest***) of entire swarm. As this is their first iteration so their current position will be their pbest position whereas the best of all *pbest* will be their *gbest.* After getting their pbest and gbest values all particle will calculate their new velocity using equation 1 and with new velocity they will update their position using equation 2.

$$V_i^{n+1} = w \cdot V_i^n + c_1 \cdot r_{i1}^n \cdot (P_i^n - X_i^n) + c_2 \cdot r_{i2}^n \cdot (P_g^n - X_i^n) \quad (1)$$

$$X_i^{n+1} = X_i^n + V_i^{n+1} \quad (2)$$

Here Vi n+1 is the velocity of ith particle for (n+1)th iteration. *W* is inertia weight [6], used for controlling the velocity. c1 and c2 are two constant values where c1 is cognitive coefficient which quantifies how much trust that particle has on its own experience, and c2 is social coefficient which quantifies how much trust that particle has on its best neighbor. Studies show that if c1 and c2 values are too small then particle may stay far behind than the targeted field and if it is too big then they may fly away from the target field [7]. Hence to overcome this problem c1 is equal to c2 is equal to 2 [1, 7] which also makes an average weight for "social" and "cognition'' parts to be 1. *r1* and *r2* are two random numbers and are kept between 0 and 1. Pin and Pgn are particle best (*pbest*) and global best (*gbest*) respectively. Using eq. 1 a new velocity is generated and then this velocity is added to the current position (*Xi*) of the particle to update its location using eq. 2. Flowchart of PSO is depicted below in fig4. 1.

A. Weighted Particle Swarm Optimization (WPSO)

PSO algorithm is to find the optimization solution and doesn't find the most importance best position. The most important in the WPSO algorithm is to giving weight value for each particle. In order to balance the (Gbest) global and (Pbest) local searching abilities, introduce a weight parameter by calculating the mean best position and how to evaluate its importance in calculate the value of m. It is natural, as in other evolutionary algorithms that associate best with the particle' s fitness value in WPSO. The mean best position is introduced to evaluate the value, making the algorithm more efficient and finds that the mean best position is simply the average on the best position of all particles. The mean best position, determines the search scope or creativity of the particle. The greater fitness value is the most important particle. Each target method defines some weight function to the each parameter. Describing it formally, the particles can rank in descendent order according to their fitness value first. Then assign each particle a weight linearly decreasing with the particle' s rank, that is, the nearer the best solution, the larger its weight coefficient.

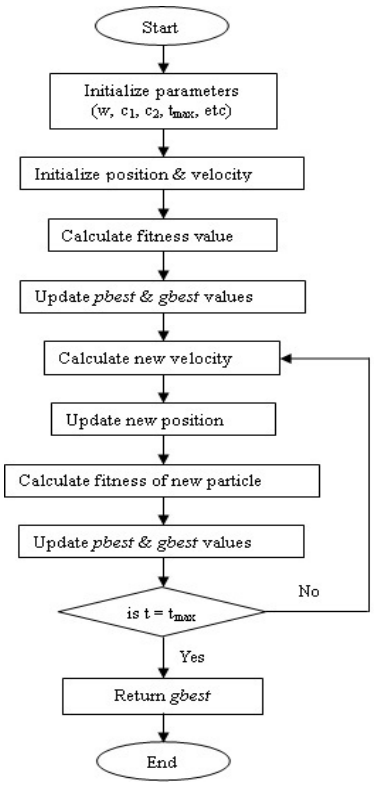

Fig.4: Flowchart of PSO algorithm

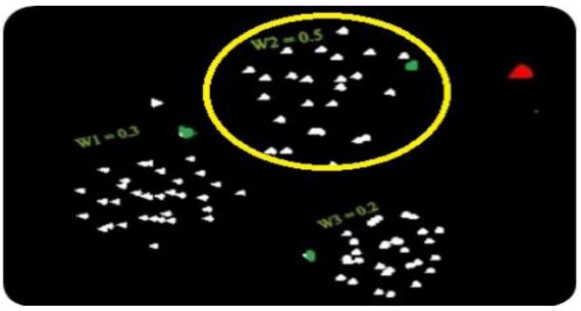

Fig.5:Weighted Particle Swarm Optimization Algorithm

Fig.5, shows the process of WPSO, here each single particle gas its own weighted values. The conditional value for weight is equal to 1. The weighed value will be dividing to all the particles and each and every particle. That is every particle assigned with the weighed value by the use of mean best position.

$$\sum_{i=1}^{n} W_i = 1 \quad (1)$$

Eq (1) denotes the weighted value which is equal to value one. In order to balance the global and local searching abilities, introduce a weight parameter in
calculating the mean best position and how to evaluate its importance in calculate the value for each particle. It is natural, as in other evolutionary algorithm that associate best with the particles' fitness value in WPSO. [16] The weighted value of the particle, determines the search scope or creativity of the particle. The greater fitness value is the most important particle, can rank the particle in descendent order according to their fitness value first. The weighted Particle swarm optimization is calculated as

$$WPSO = \frac{w_1 * P_{best} + w_2 * P_{best} + w_3 * P_{best}}{n} \rightarrow (2)$$

n = no: of particle

Eq (2) calculated the WPSO. Every particle is randomly selected with its weighted mean value. The weighted mean value is taken to reduce the particle the high priority or heavy weighed particle is select for the process of finding an optimal solution for randomized unit testing.

IV. SIMULATION RESULTS AND DISCUSSIONS

A. Simulation Results For WPSO For Two Stage Amplifier:

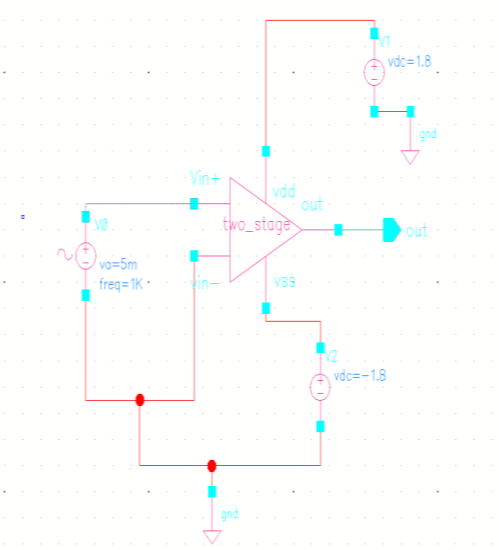

Fig.6: Test circuit of two stage Op-amp

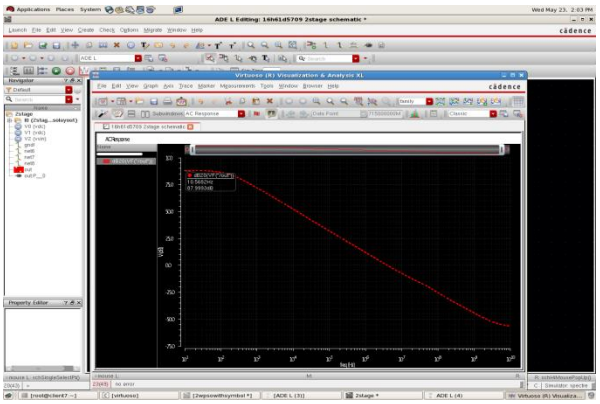

Fig.7: Simulation result of Gain for two stage Op-amp

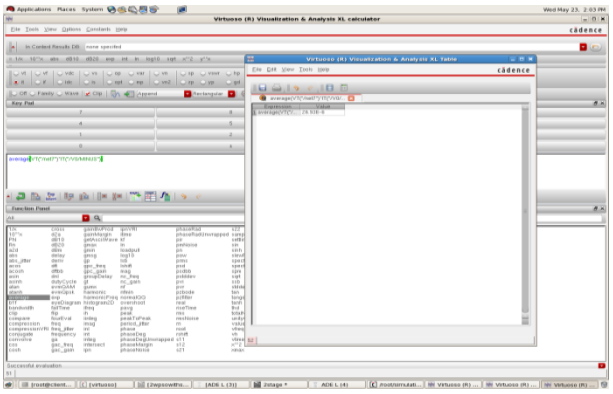

Fig .8:Power calculation of two stage Op-amp

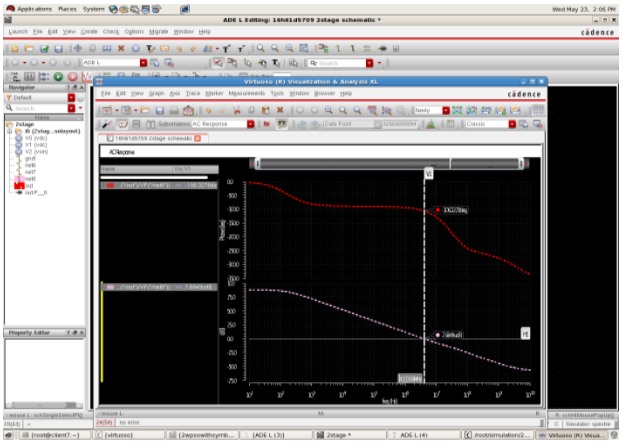

Fig .9: Simulation result of Phase Margin for two stage Op-amp

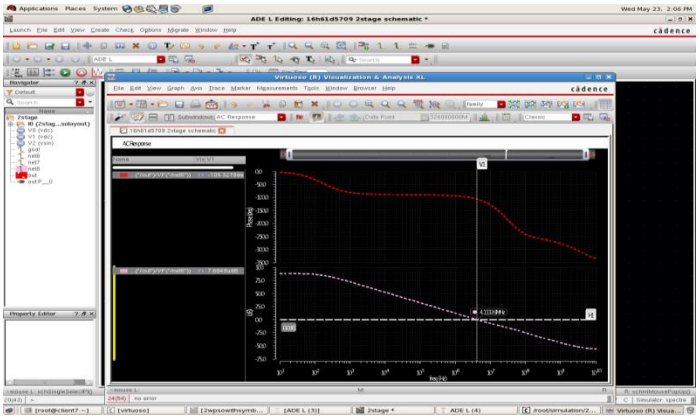

Fig .10:Simulation result of UGF for two stage Op-amp

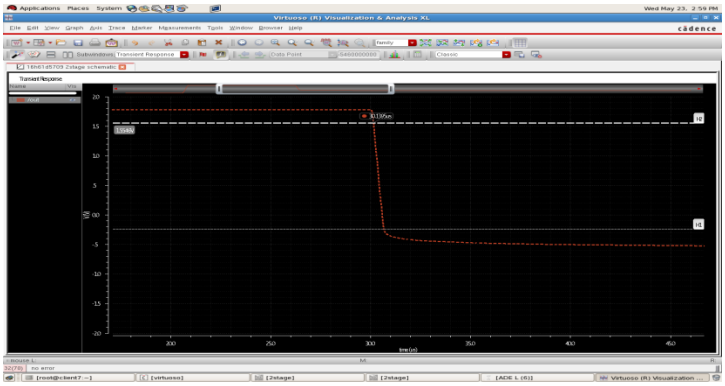

Fig .11: Negative Slew Rate plot of two stage Op-amp

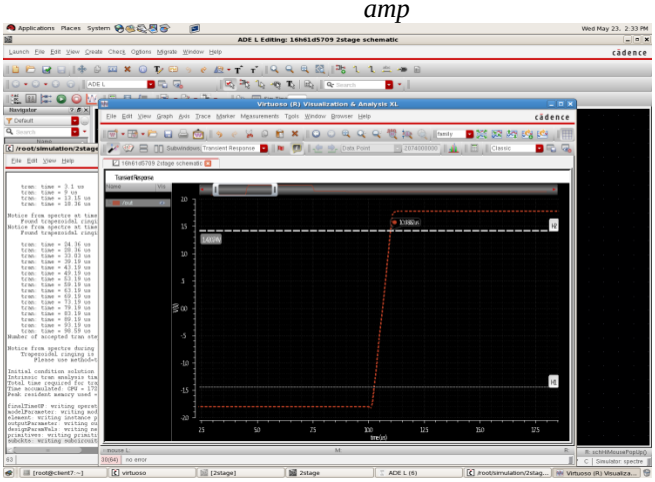

Fig.12: Positive Slew Rate plot of two stage Op-amp

B. Simulation Results Of WPSO For Folded Cascode Amplifier

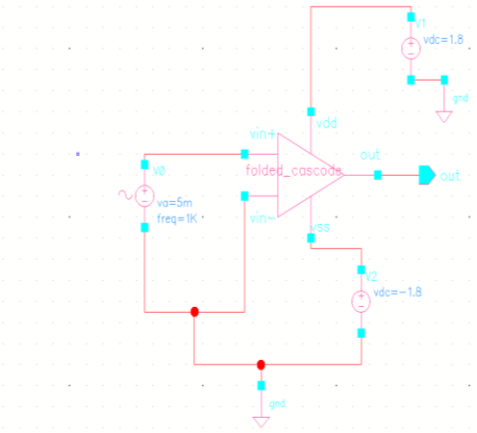

Fig .13: Test circuit of folded cascode Op-amp

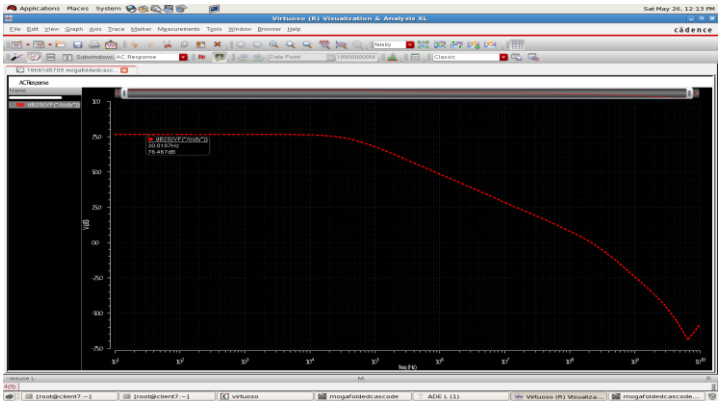

Fig 14. Simulation result of Gain for folded cascode Op-amp

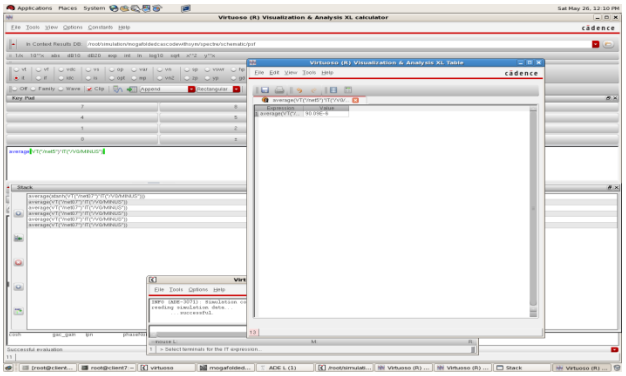

Fig 15. Power calculation of folded cascode Op-amp

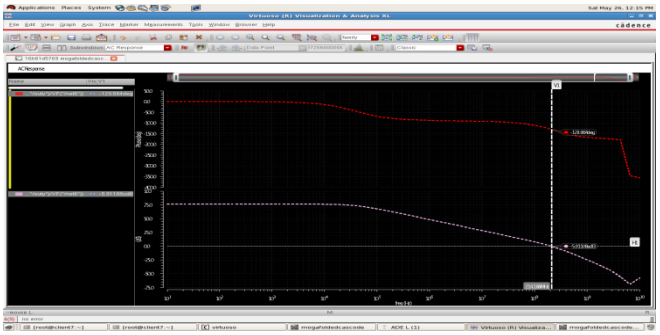

Fig 16.Simulation result of Phase Margin and UGF for folded cascode Op-amp

Fig 17. Positive Slew Rate plot of folded cascode Op-amp

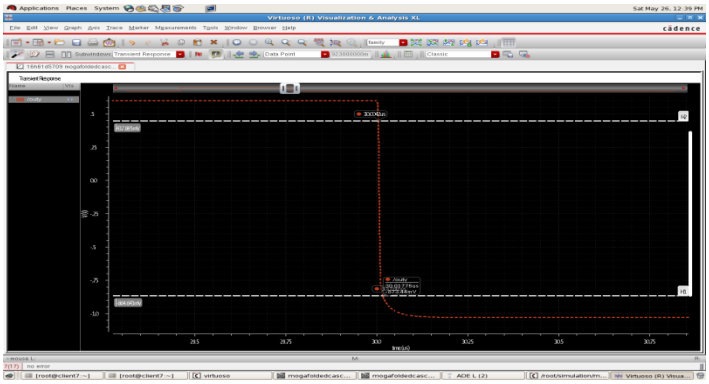

Fig 18. Negative Slew Rate plot of folded cascode Op-amp

C. Simulation Results Of WPSO For Telescopic Amplifier:

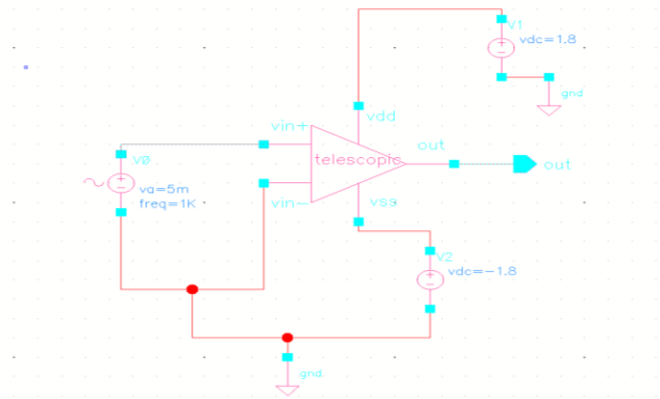

Fig.19: Test circuit for Telescopic Op-amp

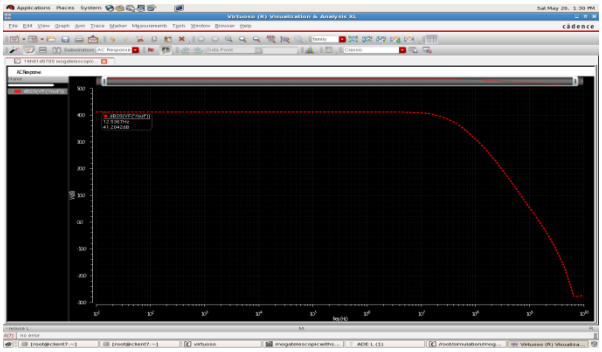

Fig .20:Simulation result of Gain for Telescopic Op-amp

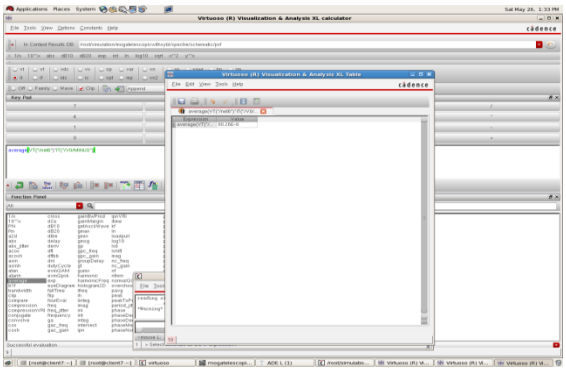

Fig.21: Power calculation of telescopic Op-amp

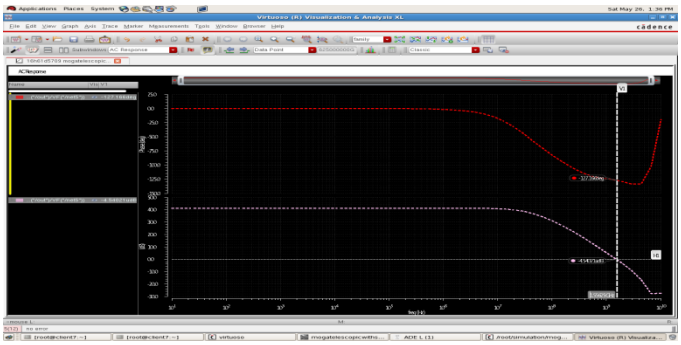

Fig .22: Simulation result of Phase Margin and UGF for Telescopic Op-amp

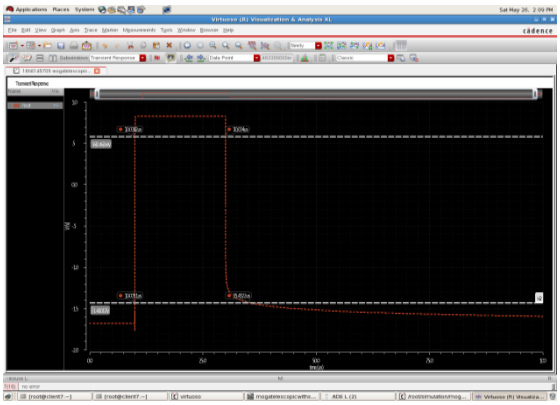

Fig .23:Positive Slew Rate plot of Telescopic Op-amp

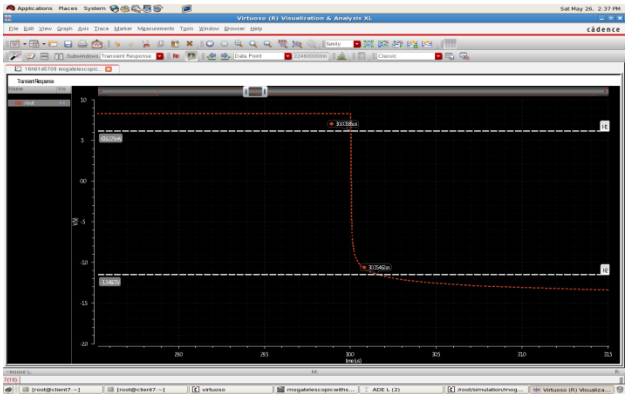

Fig.24: Negative Slew Rate plot of Telescopic Op-amp

Table 1 Design Variable of Attained for CMOS Two-Stage operational amplifier circuit

Design Variables	PSO[4]	Proposed MPSO
Ibias(µA)	40.39	10
W1/L1(µm/µm)	4.9/2	1.51/1.59
W2/L2(µm/µm)	4.9/2	1.51/1.59
W3/L3(µm/µm)	5.9/2	8.05/1.32
W4/L4(µm/µm)	5.9/2	8.05/0.46
W5/L5(µm/µm)	2.1/2	1.23/1.1
W6/L6(µm/µm)	90.9/2	5.6/0.72
W7/L7(µm/µm)	16.3/2	5.94/0.64
W8/L8(µm/µm)	2.1/2	3.4/0.64
C_L(pF)	10	5
C_c(PF)	3	3

Table 2 Design Variable of Attained for CMOS Folded cascode operational amplifier circuit

Design Variables	PSO[4]	Proposed MPSO
W1/L1(µm/µm)	0.5/0.69	0.6/1.08
W2/L2(µm/µm)	0.5/0.69	0.6/1.08
W3/L3(µm/µm)	1.02/1.02	1.0/1.0
W4/L4(µm/µm)	0.84/0.58	0.74/0.74
W5/L5(µm/µm)	0.84/0.58	0.74/0.74
W6/L6(µm/µm)	1.02/0.62	1.22/0.51
W7/L7(µm/µm)	1.02/0.62	1.22/0.51
W8/L8(µm/µm)	1/0.87	0.51/0.91
W9/L9(µm/µm)	1/0.87	0.51/0.91
W10/L10(µm/µm)	1/0.87	0.51/0.91
W11/L11(µm/µm)	1/0.87	0.51/0.91

Table 3 Design Variable attained for CMOS Telescopic operational amplifier circuit

Design Variables	PSO[4]	Proposed MPSO
W1/L1(µm/µm)	1.10/0.53	1.06/0.54
W2/L2(µm/µm)	1.10/0.53	1.06/0.54
W3/L3(µm/µm)	1.32/0.72	1.28/0.49
W4/L4(µm/µm)	1.32/0.72	1.28/0.49
W5/L5(µm/µm)	1.89/0.78	1.24/0.45
W6/L6(µm/µm)	1.89/0.78	1.24/0.45
W7/L7(µm/µm)	1/0.92	1/1
W8/L8(µm/µm)	1/0.92	1/1
W9/L9(µm/µm)	1.10/0.67	1.10/0.89

Parameters	Two stage		Folded cascode		Telescopic	
	Specifications	results	Specifications	results	specifications	Results
Gain	86dB	86.6dB	70dB	76.47dB	50dB	41.2dB
Unity Gain Bandwidth	5MHz	6.45MHz	100MHz	14 MHz	1GHz	1.53GHz
Phase margin	60deg	60deg	60deg	62 Deg	60deg	53 Deg
Slew rate	5V/us	10V/us	>100 V/us	258 V/us	>100 V/us	424 V/us
Power	<=50uW	63uW	<100uW	90.1uW	<=100uW	80.26uW
Area	<100um^2	97um^2	100um^2	96um^2	100um^2	92um^2

Table 4 Comparison of input specifications and final simulation results of three topologies

V. CONCLUSION

In this paper, a MPSO based approach is employed for the optimal design of a CMOS amplifiers. The hybrid version of the particle swarm optimization algorithm and weighted approach, is proposed to optimize the design variables such as MOS transistor size, power and meet the given specification. The design objectives of the CMOS circuits are considered as the cost function of the Modified Particle swarm optimization algorithm. The simulation results prove that the proposed method successfully meets the circuit design specifications and also minimize the chip size. In addition to the simulation-based method, the cadence virtuoso simulations were carried out to validate the CMOS circuit specifications. It has been shown that the design of the CMOS circuit using the MPSO method is very effective compared with other design methods. The proposed design technique has the ability to optimize the CMOS circuit performances. Hence the MPSO algorithm is an efficient technique for complex analog IC design.

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Mr.E. Srinivas received the B.Tech degree in Electronics and Communication Engineering from Anurag Engineering College, in 2007 and M.Tech degree in VLSI System Design from Anurag Group of Institutions (Formally CVSR College of Engineering), in 2010. He is Currently Pursuing his Ph.D degree in Electronics and Communication Engineering at JNTU Hyd. His Doctrol research is directed towards the design a low voltage, low power VLSI Analog circuits.

Dr.N.Balaji obtained his B.Tech degree from Andhra University. He received Masters and Ph.D degree from Osmania University, Hyderabad. Presently he is working as a professor in the department of ECE, JNTU Vijayanagaram, and A.P. He has authored more than 25 Research papers in national and international conferences and journals. He is a life time member of ISTE and Member, Treasurer of VLSI Society of India Local Chapter. His areas of research interest are VLSI, Signal Processing Radar and Embedded Systems.

Dr.L Padma sree, presently she is working as a professor in the Department of ECE VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad.She as authored more than 20 research papers in National and International Conferences and Journals. Her areas of research interest are VLSI, Neural Networks and Embedded systems