8 - Bit Multiplier using Lector Technique to reduce Leakage Current

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Abstract **–** In this paper we propose a new technique for implementing low leakage current of 8-bit multiplier using lector technique in which a p-type and an n-type leakage control transistor (LCT) are inserted between the pull-up and pull-down network, and the gate of one transister is controlled by the source of the other. For any combination of inputs, one of the LCTs will operate near its cut-off region and will increase the resistance between supply voltage and ground, resulting in reduced leakage current.

Keywords – *lector, multiplier, leakage current*

I. INTRODUCTION

In digital devices, multiplier is the most commonly used circuit. Multiplication is one of the arithmetic operations performed by multiplier in the various analog and digital circuits. Design targets of multiplier are high speed, low power consumption, regularity of layout and therefore less area required or even combination of them in one multiplier are required in that way making them suitable for various VLSI implementations. Multiplication is one of the basic functions used in digital signal processing same as addition, substraction, division.

To reduce leakage current so many techniques are available sleep transistor technique, Forced stack technique, Sleepy stack technique and the latest technique named as LECTOR technique. These techniques listed above reduces the leakage by stacking leakage path using the off transistors. In LECTOR technique the leakage control transistors are used in between pull-up and pull-down network [1]. here, we use lector technique to reduce leakage current of 8-bit multiplier circuit. In this lector technique, two leakage control transistors (a p-type and a n-type) within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other transistor. In this arrangement, one of the LCTs is always "near its cutoff voltage" for any of the input combination. This increases the resistance of the path from to ground, leading to significant decrease in leakage currents. The gate-level net list of the circuit is first converted into a static CMOS complex gate implementation and then LCTs are introduced to obtain a leakage-controlled circuit. The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit, and it results in better leakage reduction compared to other techniques.

II. RELATED WORK

CMOS is the universally used technology to construct integrated circuits. Static CMOS is the most commonly used logic style which consists of pull down network (PDN) and pull up network (PUN). It is truly an advanced version of the static CMOS inverter with multiple inputs. There are so many methods for leakage power or leakage current control. In paper [2], the leakage current is dependent on the input vector to the gate. With additional control logic, when circuit is idle, it is put into a low leakage standby state and when it is reactivated, it restored to the original state. Reactivation state forces the need to remember the original state information before going to low-leakage standby state. This requires special latches, therefore increasing the area of the circuit by about five times in the case [3]. Another technique for leakage power control is power gating, which turns off the devices by cutting off their supply voltage [4], [5]. This technique makes use of a NMOS and/or PMOS device (sleep transistor) in between the supply voltage and ground. when the circuit is active the sleep transistor is turned on and when the circuit is in idle state then the sleep

transistor is turned off with the help of sleep signal. This creates virtual power and ground barriers in the circuit. Hence, there is a significant destructive effect on the switching speed when the circuit is active. In [6] and [7], the use of multiple threshold voltage CMOS (MTCMOS) technology for leakage control is described. The transistors of gates are at low threshold voltage and ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is same as to that of a sleep transistor. The existence of reverse conduction paths tend to reduce the noise margin or in the worst case may result in complete failure of the gate [8]. Moreover, there is a performance fine since high-threshold transistors appear in series with all the switching current paths. A variation of MTCMOS technique is the Dual V_t technique, which uses the transistors with two different threshold voltages.

In [9], the authors use the concept of forced stacks for leakage control. Forced stacking introduces an additional transistor for every input of the gate in both N- and P-networks.This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current. However, the loading requirements for each input introduced by the forced stacking reduces the drive current of the gate automatically. This results in a detrimental impact on the speed of the circuit.

III. LECTOR TECHNIQUE

Lector technique is a technique in which two leakage control transisters (one p-type and one n-type) are connected between pull-up and pull-down circuit within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other transistor. The path from Vdd to ground leads to significant decrease in leakage currents in this arrangements. The arrangements are shown in fig.1. The basic idea behind LECTOR technique is that "a state with more than one transistor OFF in a path from supply voltage to ground is less leaky than a state with only one transistor OFF in any supply to the ground path."

Leakage loss occurs when the output is stable means low output or high output. In this paper we implemented 8-bit multiplier circuit using lector technique. This 8-bit multiplier is made with using basic cmos gates as Inverter, AND, OR, Half Adder and Full Adder. Each circuit is made using lector technique means leakage control transisters are inserted in pull up and pull down network of each of the circuit used in 8-bit multiplier circuit.

LCT's are introduced between two nodes N1 and N2. The gate of the LCT's is controlled by the source of the other. Since LCTs are self-controlled so there is no need of external circuit. These two LCTs increases the resistance between VDD and ground, and therefore reduces the leakage current. The topology of a LECTOR CMOS gate is shown in Fig.1. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

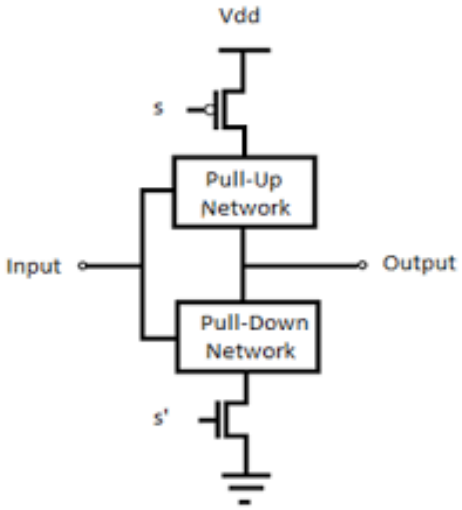

Fig. 1 Generalised structure for leakage controlled gates

IV. 8-BIT MULTIPLIER USING LECTOR TECHNIQUE

8-bit multiplier circuit is made by using basic cmos gates as Inverter, AND, X-OR, OR, Half Adder and Full Adder. Here, we used 45 nm technology because the multipliers using 45 nm CMOS technology is better in terms of power and surface area as compare to 65 nm and 90 nm CMOS technologies. In tanner tool we made the gate inverter in schematic then converted it into a symbolic form same as this we implemented the gates OR, AND, X-OR also and circuits of half adder and full adder also. When implementing these gates leakage control transistors are also inserted in the circuits for getting an output which shows minimum leakage current. Each and every circuit which is used in 8-bit multiplier consists of two leakage control transistors between pull-up and pull-down circuit of the circuit. The block diagram of the 8 bit multiplier using half adder and full adder is shown in fig.2.

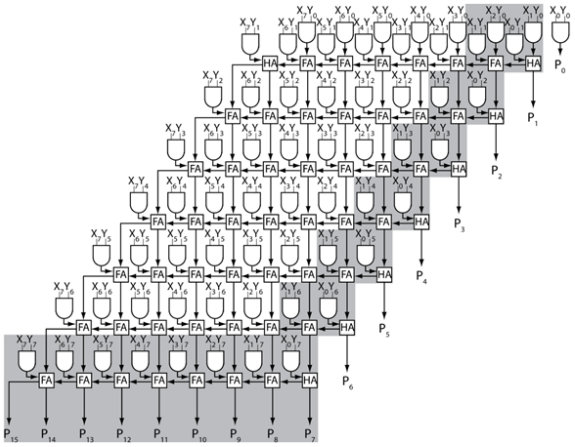

Fig.2 Block diagram of 8 bit multiplier using half adder and full adder

Above figure is a block diagram of 8 bit multiplier using half adder and full adder. Fig.3 shows schematic representation of 8 bit multiplier using half adder and full adder in which the circuits are represented in a symbolic form. 8 bit multiplier consists of 8 bit input and gives 16 bit output. Therefore the output waveforms and leakage current waveforms are shown in fig.4 and fig 5 respectively. Leakage current is less in the circuit in which we use the lector technique and therefore fig 6 shows the leakage current of the circuit in which we did not use the lector technique. Then we can compare the result of both the circuits.

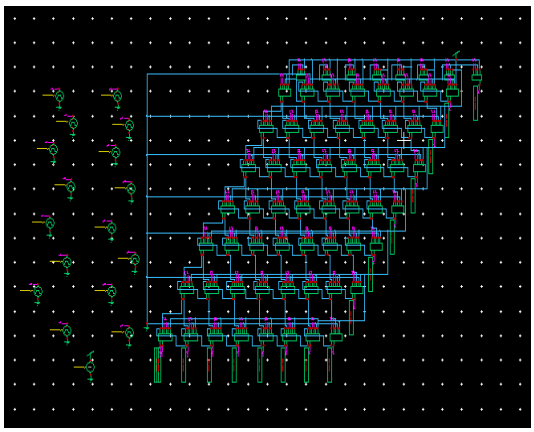

Fig.3 Schematic representation of 8 bit multiplier using half adder and full adder

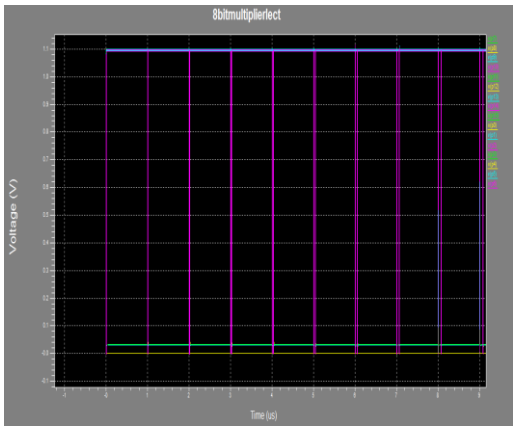

Fig.4 Output waveforms of 8 bit multiplier

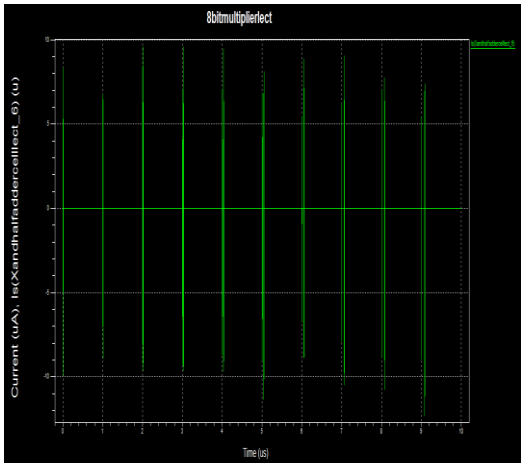

Fig 5 Leakage current waveforms of 8 bit multiplier using lector technique

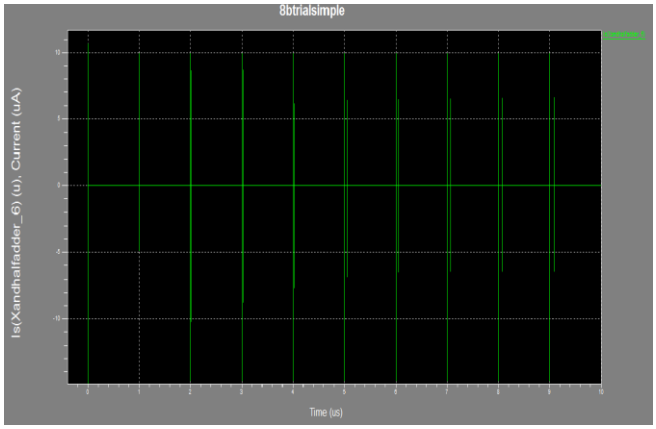

Fig 6 Leakage current waveforms of 8 bit multiplier without Lector technique

RESULT

TABLE I. Result

Parameter	8-bit multiplier	8-bit multiplier using lector technique
Leakage current	*11uA*	*8.5uA*
Delay	2.6883e-010	4.0535e-011

CONCLUSION

It is clear from the table that while using simple circuit, leakage current is 11uA and while using the circuit using lector technique, leakage current is 8uA. But the circuit using lector technique delays the output more as compared to the simple circuit as shown in the table.

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