Test Time Efficient Design of 6t Dual Port SRAM Cell

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Abstract- Test time is rapidly increasing for Static Random Access Memory. Low test time is a need of the hour. With decreasing, technology node, new failure mechanisms are emerging in CMOS circuits, which need novel techniques of testing. These increased testing techniques create difficulties, especially the area-constrained dual port SRAM cells. March algorithm is the most widely used efficient testing technique for SRAM cells. In this paper, a novel March testing methodology has been proposed to reduce the test time for dual port SRAM cells.. Using the novel March test implementation proposed,for dual port SRAM, an appreciable test time reduction is being achieved, compared to the existing test techniques with the same fault coverage.

Index Terms- Test time, March test, Dual port SRAM

I. INTRODUCTION

March algorithm is a widely used testing algorithm because of it's high fault coverage, but it has a very high computational time. A complete March test is given in the "{….}" and each March element is specified in "(…)". represents either an upward addressing order or a downward addressing order. The March test modification for dual port SRAMs has been covered in this work

A. PROBLEM FORMULATION-MECHANISMS OF FAILURE AND THEIR CORRESPONDING FAULT MODELS:

Intra-die variations, resulting from mismatches in parameters of similar transistors (threshold voltage V_t and geometry L or W), may lead to new failures in memories.[14,15] The threshold voltage shift of each transistor is considered to be a zero mean Gaussian distribution. Due to its area constraint, a 6-T SRAM[7] is particularly vulnerable to process variations[13]. Mismatch in the six transistors of SRAM cells may result in one of the following conditions.

1) During read operations, comparatively strong access transistors or weak pull-down transistors lead to an increase in the internal node voltage that stores "0" in theSRAM cell. If the pull-up transistor of the cross-coupled inverter is weak, the SRAM cell may flip during the read operation[21]. This is referred as flipping read failure.

2)Comparatively strong pull-up transistors or weak pulldown transistors shift the trip point of the cross-coupled inverters to a higher voltage. This may lead to an unsuccessful write operation of the SRAM cell. This failure is referred to as write failure.

3). Due to excessive mismatch in the cross-coupled inverters,a SRAM cell may lose its value without the cell being accessed by any operations, especially when the supply voltage is lowered to save leakage. This failure is referred to as hold failure.[17]

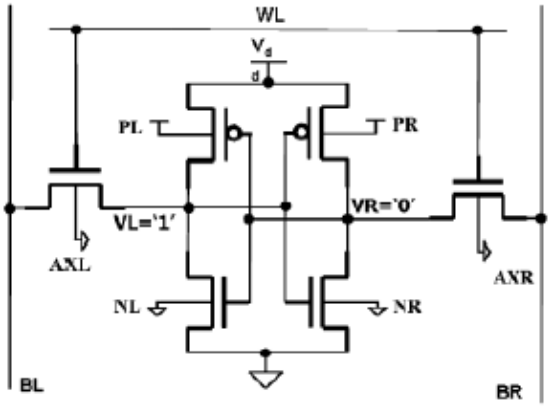


Fig.1: The 6-T SRAM cell

II. MARCH ALGORITHM FOR TESTING OF DUAL PORT SRAM

March sequence[9] is used widely for memory testing. It involves applying(writing and reading) patterns to each cell in memory before proceeding to the next cell and the same pattern must be applied to all the cells. This is done in either increasing or decreasing memory address order. March test[15] basically involves the following steps:

1. In increasing order of address of the memory cells, write 0s to the cells.
2. In decreasing order of address of the memory cells, read the cells (expected value 0) and write 1 to the cells.
3. In increasing order of address of the memory cells, read the cells (expected value 1) and write 0 to the cells.
4. In decreasing order of address of the memory cells, read the cells (expected value 0)

Dual port SRAM cells have their corresponding fault models. They have a higher fault ratio due to the interaction of the aggressor and the victim cell. Two port faults cannot be sensitized using single port fault sensitizations operations. As dual port faults are considered to be a combination of two weak faults. They are divided as faults involving just the

victim cell or aggressor cell and the faults involving both aggressor and victim cells. Their broad classification is as shown here in the figure below.

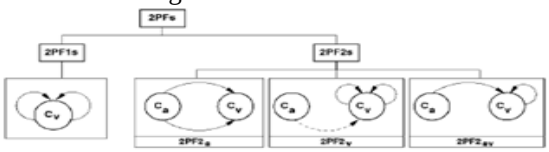


Fig.2 Classification of 2PFs.

A better understanding of the 2PF faults can be obtained from the nomenclature shown in the following diagram.

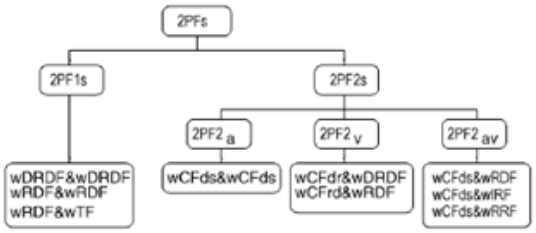


Fig.3 A taxonomy of 2PFs.

A detail of the dual port SRAM faults , along with the ideal march sequence, is presented in the figure below.

TABLE 1
List of 2PFs; $x \in \{0,1\}$ and $d = \text{don't care}$

FFM	Fault primitives
wDRDF&wDRDF	$< r0 : r0/\uparrow/0 >, < r1 : r1/\downarrow/1 >$
wRDF&wRDF	$< r0 : r0/\uparrow/1 >, < r1 : r1/\downarrow/0 >$
wRDF&wTF	$< r0 : w\uparrow/0/- >, < r1 : w\downarrow/1/- >$
wCF_{ds}&wCF_{ds}	$< w0 : rd; 0/\uparrow/- >, < w0 : rd; 1/\downarrow/- >$ $< w1 : rd; 0/\uparrow/- >, < w1 : rd; 1/\downarrow/- >$ $< rx : rx; 0/\uparrow/- >, < rx : rx; 1/\downarrow/- >$
wCF_{dr}&wDRDF	$< 0; r0 : r0/\uparrow/0 >, < 0; r1 : r1/\downarrow/1 >,$ $< 1; r0 : r0/\uparrow/0 >, < 1; r1 : r1/\downarrow/1 >,$
wCF_{rd}&wRDF	$< 0; r0 : r0/\uparrow/1 >, < 0; r1 : r1/\downarrow/0 >,$ $< 1; r0 : r0/\uparrow/1 >, < 1; r1 : r1/\downarrow/0 >$
wCF_{ds}&wRDF	$< w0 : r0/\uparrow/1 >, < w0 : r1/\downarrow/0 >,$ $< w1 : r0/\uparrow/1 >, < w1 : r1/\downarrow/0 >$
wCF_{ds}&wIRF	$< w0 : r0/0/1 >, < w0 : r1/1/0 >,$ $< w1 : r0/0/1 >, < w1 : r1/1/0 >$
wCF_{ds}&wRRF	$< w0 : r0/0/? >, < w0 : r1/1/? >,$ $< w1 : r0/0/? >, < w1 : r1/1/? >$

Here CF(coupling faults), RDF(read destructive faults), DRDF(deceptive read destructive faults) have been explained already.The optimum march test sequence for dual port SRAM that has been used for the modification proposed is given here:

$$\{ \underset{M_0}{\Updownarrow (w0 : n)} ; \underset{M_1}{\Updownarrow (r0 : r0, r0 : -)} ; \underset{M_2}{\Updownarrow (w1 : -)} ; \underset{M_3}{\Updownarrow (r1 : r1, r1 : -)} \}$$

Fig.4 . March 2PF1-. (optimal version) for Dual Port SRAM

This is the March sequence for maximum fault coverage for detecting two port faults involving single cell with maximum. The corresponding March sequence with maximum fault coverage for two port faults involving 2 cells is given below:

$$\{ \underset{M_0}{\Updownarrow (w0 : n)} ; \underset{M_1}{\uparrow_{c=0}^{C-1} (\uparrow_{r=0}^{R-1} (w|_{r,c} ; r0|_{r+1,c}, r|_{r,c} ; w|_{r+1,c}, w0|_{r,c} ; r|_{r+1,c}, r0|_{r,c} ; w0|_{r+1,c}))} ; \underset{M_2}{\uparrow_{r=0}^{C-1} (\uparrow_{r=0}^{R-1} (w|_{r,c} ; r0|_{r,c+1}, r|_{r,c} ; w|_{r,c+1}, w0|_{r,c} ; r|_{r,c+1}, r0|_{r,c} ; w0|_{r,c+1}))} \}$$

Fig.5 . March $2PF2_{av}$ – (optimal version). for Dual Port SRAM

III. PROPOSED MODIFICATION IN MARCH SEQUENCE

The prime focus of this work has been to decrease the computation time for testing the dual port 6-T SRAM cell using March Algorithm. In order to solve this problem of high computation time, the march elements mentioned in the figure above have been taken up and the following novel approaches have been implemented in them.

1)A single March element has been divided into a set of distinct operations that are applied on two different memory addresses simultaneously.

2)The simultaneous application is the innovative part that gives a reduction in computation time.

3) To better understand this, let us consider one of the optimized March elements studied above

$\Updownarrow \{ \Updownarrow$ (w0 : n) ; $\Uparrow$ (r0 : r0, w1 : r0) ; $\Uparrow$ (r1 : r1, w0 : r1)

In order to reduce the computation time, the proposed approach simultaneously implements the two operations by targeting two different memory locations at the same time, one for r0 operation and one for w1 operation. The two different memory locations that are accessed from the topmost and bottommost memory location of the dual port sram, that is there are two loops running to apply the two memory operations; one loop starts from the highest memory location and proceeds towards lower memory locations and one loop starts from the smallest memory location and proceeds towards the higher memory locations. One loop applies (say, in this example) r0 and the other loop applies w1. According to the base paper,[15] the aggressor cell can stimulate a fault in a weak victim cell only if the 2 cells are at immediate neighbouring memory locations. Thus, the 2 memory locations chosen here for simultaneous application of the operations of the march element, do not infringe any basic criteria for detection of faults as neither the aggressor cell nor the victim cell constitute a pair of neighbouring memory locations. The operation stops when the 2 simultaneous loops meet at the center of the memory array. This is the novelty proposed in this thesis work. Codes have been written for performing a march operation and detecting faults if any. A signal "test_complete" turns active high, when the march operation

has been performed on the entire dual port SRAM. The test time at which the test_complete signal goes high, is much reduced using this proposed approach , than the conventional approach to implement the March algorithm. After implementing the design above, the circuit is simulated. The RTL schematic of the circuit is generated. It is shown in the figures below. The timing waveforms of the circuit have been generated. The timing waveforms have been generated for 2 cases-

1) Implementing the standard design of 6-T SRAM cell without the modifications proposed above and

2) Implementing the above proposed computation time efficient 6T SRAM cell.

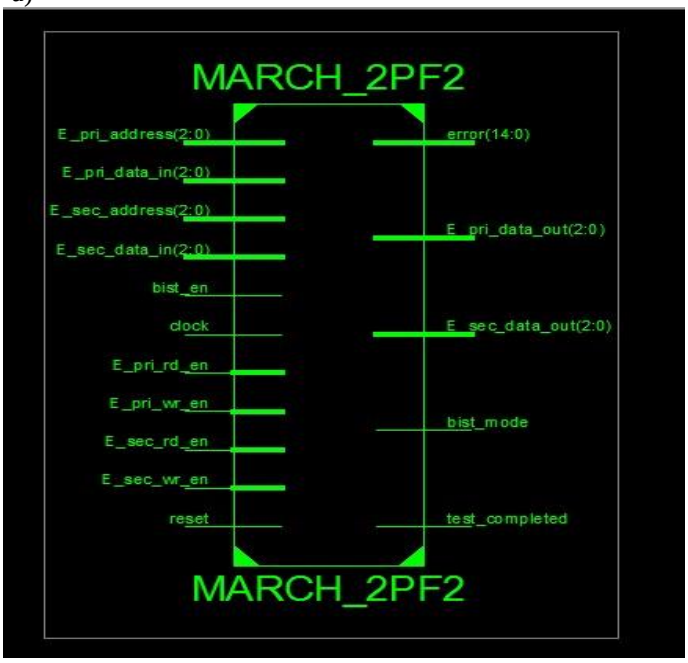
The signal "test_comp" clearly depicts an appreciable improvement in the computation time. An improvement of 16.2% is achieved with the design proposed above

IV. SIMULATIONS AND RESULTS

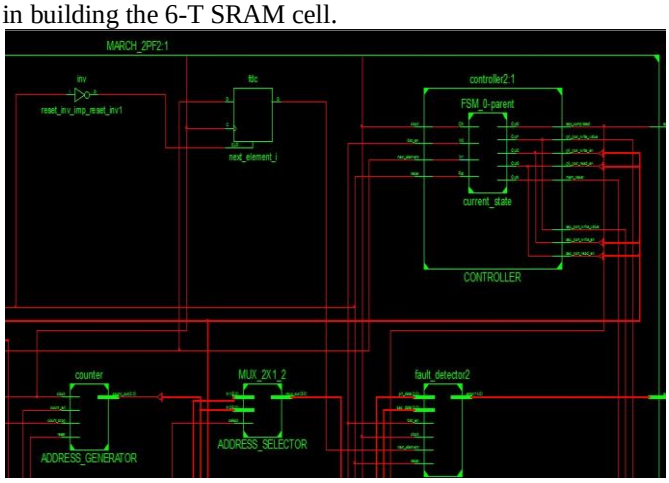
Based on the approach given above, the design has been implemented on the Xilinx ISE 14.2 and the results are as presented below. Codes have been written for performing a march operation and and detecting faults if any. A signal "test_complete" turns high, when the march operation for dualport SRAM has been performed on the entire dual port SRAM. The test time at which the test_complete signal goes high, is much reduced using this proposed approach , than the conventional approach to implement the March algorithm. The results have been shown in the next chapter.

1)The RTL diagram of the SRAM cell is given here:

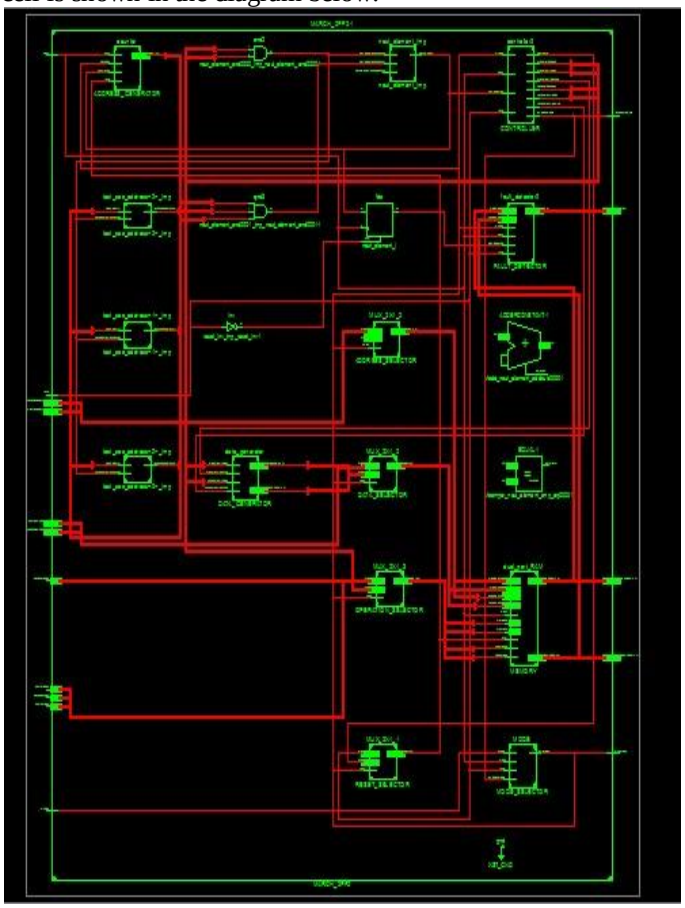
a)



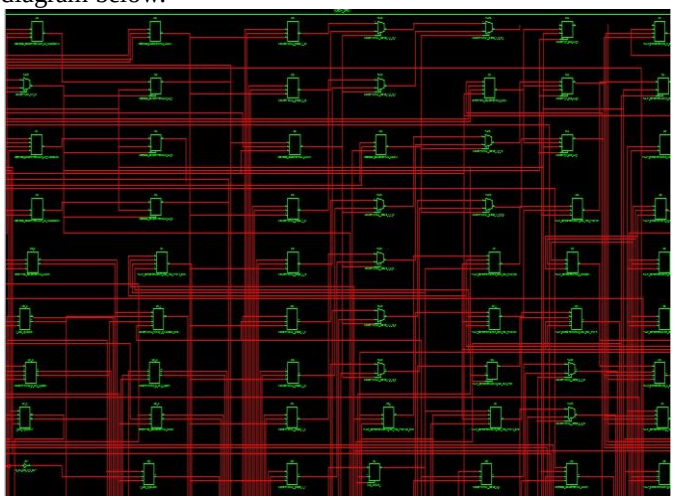
b)The detailed RTL of any part of RTL diagram is obtained by double clicking on it as shown in the diagram below. The following diagram shows the modules that have been used up in building the 6-T SRAM cell.



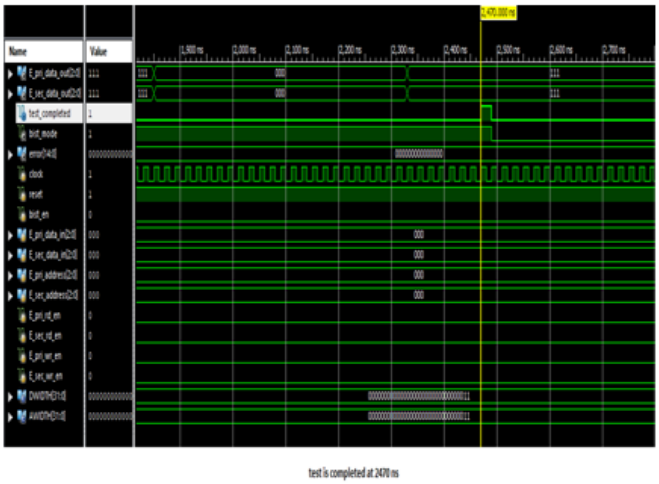
c)The detailed RTL diagram, showing all the individual modules, that have been used in the program to make up the cell is shown in the diagram below.



d)The detailed RTL showing the LUTs has been shown in the diagram below.

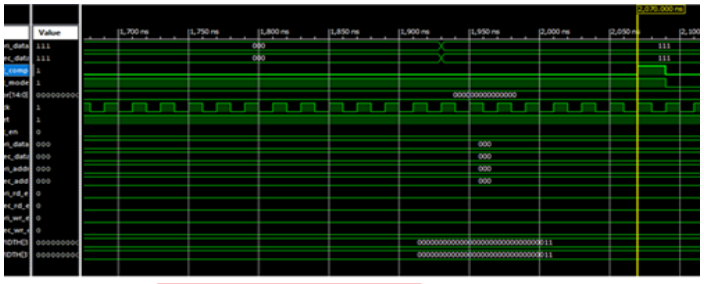


1) a)The following diagram shows the timing waveform of the 6-T SRAM cell, simulated with the conventional approach to implement March algorithm.



test is completed at 2470 ns

b) The following diagram shows the timing waveform obtained by simulating the 6-T SRAM cell with the proposed implementation of the March algorithm.



Test is completed at 2070ns which is 400ns less than the previous result (without the proposed March implementation)

As can be seen from the results above, the proposed implementation of march algorithm reduces the test time by 16.9 %, which is an appreciable improvement in reducing the total test time. This increases the overall efficiency of the circuit.

Table 2: Experimental Results

Test time with the existing March sequence fordualport SRAM	Test time with the proposed approach for March sequence for dualport SRAM	Percentage improvement
2470 ns	2070ns	16.9%

V. CONCLUSION AND FUTURE SCOPE

With technology scaling, process variations result in functional failures in memory systems. This leads to novel testing techniques, which cause an increased test time. In this work, March test sequence for dual port SRAM has been taken up and modifications have been proposed in the same, to reduce the test time of the SRAM memory cell. Implementing the optimized March test sequence with the approach proposed above, of simultaneously applying the different dual port March elements in ascending and descending order, greatly reduces the test time, as is evident in the results. So this technique is efficient for a reduction in the test time. This also increases the cost effectiveness. Thus, this technique can be efficiently implemented to obtain a high fault coverage with a reduced test time. The results reflect a 16.9 % improvement, using the proposed approach.

Further scope of work in this research work , lies in some domains. Some of them are mentioned here. To reduce the test time, further optimizations in the march test sequence can be done. In this thesis, an optimized March sequence has been used. Optimizations used account both for high faut coverage and reduced test time. Similarly alternative optimizations can be proposed to reduce the test time, like observing the redundancy in some elements and phasing it out. Thus , the topic is promising for future research. The paper showed that the approach generates, 16.9 % improvement that is, efficient results.

VI. REFERENCES

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