Design of High Performance Mixed Logic 4-16 Decoder using GDI Technique

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***Abstract*—** In every wireless communication, data security is the main concern. The decoders are designed primarily to provide security for data communication by designing standard encryption and decryption algorithms. Decoders are used in audio systems to convert analog audio into digital data. It is used as a decompressor to convert compressed data such as images and videos into uncompressed form. Decoders use electronic circuits that converts computer instructions into CPU control signals. Existed 4-16 line decoder design having two 2-4 decoders and outputs of those decoders given to the inputs of the 15 CMOS based NAND gates. 2-4 decoders are designed by using TGL and DVL logics. Now we modify these CMOS NAND gates replaced with GDI (Gate Diffusion Induced) logic and remaining logics are taken as same. Present design can be implemented using PYXIS GDK 130nm technology (MENTORGRAPHICS). The decoder enhances the performance in terms of switching energy, delay and power-delay product than existed decoder.

Index Terms—CMOS NAND, 2-4 decoder, TGL (Transmission Gate Logic), DVL (Dual Value Logic), GDI Gate Diffusion Induced).

I. INTRODUCTION

A binary decoder is a multi-input, multi-output combinational circuit that converts a binary code of n input lines into a one out of 2^n output code. These are used when there is need to activate exactly one of 2^n output based on an n-bit input value. Generally, decoders are provided with enable inputs so as to activate the decoded output based on data inputs. The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power saving exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power consumption, delay and area are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. Investigations of low-power logic styles reported in the literature so far, however, mainly focused on particular logic cells such as Decoders, which are used in some data transfer techniques.

In this paper, these investigations are extended to a much wider set of logic gates, and with that, to arbitrary decoders. The power consumption characteristics of various existing logic styles are compared qualitatively and quantitatively by actual logic gate implementations and simulations under realistic circuit arrangements and operating conditions. Investigations of sequential elements, such as latches and flip-flops, not included in this work, but can be found elsewhere in the literature.

Different logic styles are available for implementing logic circuits. In that one of the logic is complementary CMOS logic style to implement combinational circuits if low power consumption and small power delay product is concern [3]. The CPL is twice as fast as conventional CMOS due to lower input capacitance and higher logic functionality. Other logic style is Complementary pass transistor which delay is reduced to half when compared with conventional CMOS logic [4]. Double pass transistor based ALU is designed to increase the performance of the entire design in [5].

Switching states of MOS transistors and signals in combinational circuits can be described by using switching and binary signal algebra in [6]. The new pass transistor logic calls DVL which contains fewer transistors than its DPL counterpart, but maintains comparable performance. This logic is characterized by better delay and power parameters [7].A method for synthesis of such networks is also developed and demonstrated in this paper. The new logic is characterized by good speed and low power.

GDI based technique (transmission port) for the design of the low-power combinational logic circuit was discussed in detail and the advantage of this style of design on static CMOS (SC) implementation and pass transistor logic (PTL), with respect to energy consumption, delay. The complexity of the area is also described in [1].

In existed design implemented using DVL, Transmission gate logics and CMOS logic styles. The modified decoder design can be used to implement using Dual Value Logic, Transmission gate logic and Gate Diffusion Induced logic which enhance the constraints of the design. GDI logic style reduces the power and delay than existed design and conventional CMOS design.

II. MODIFIED DECODER ARCHITECTURE

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the $m = 2^n$ minterms of n input variables.

Below we observed a 4-16 low level decoder which consists of two 2-4 decoders and 15 NAND gates. This decoder generates the 16 minterms d0-d15 of 4 input variables a, b, c and d. In this approach the design can be divided into two levels. Level1 represents upto outputs of the two 2-4 line decoder i.e total 8 output lines. In level 2, level1 outputs are given to the 16 NAND gates input as shown in figure below.

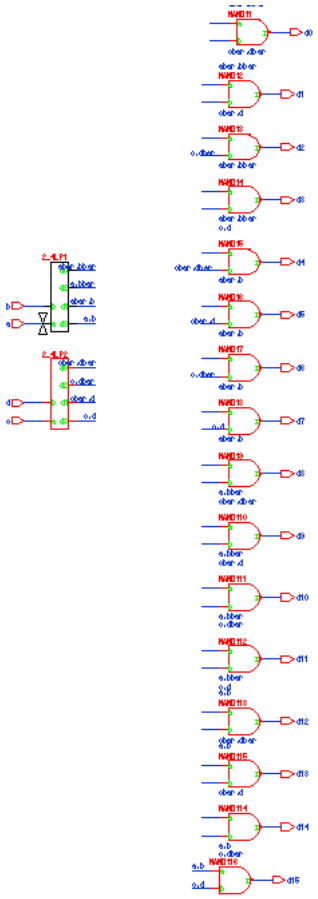


Figure 1: Modified decoder design using DVL, TG and GDI

A) 2-4 decoder:

A 2-4 line decoder generates the 4 minterms D0-D3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination; one of the 4 outputs is selected and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the complementary minterms I0-I3, thus the selected output is set to 0 and the rest are set to 1, as shown in Table.

Truth tables: 2-4 DECODER

a)High-level decoder

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

b) Low-level decoder

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

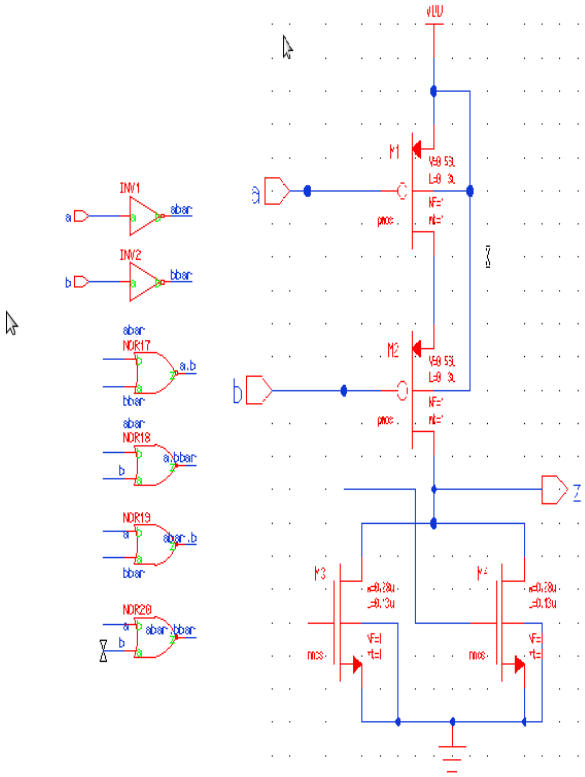


Figure 2: CMOS based 2-4 DECODER

Figure 2 represents 2-4 decoder design based on CMOS logic which is existed design in figure1. This can be modified [1] by using DVL, Transmission gate logic shown in figure 3. These logic styles enhances the design parameters like delay, energy consumption and area also. In CMOS decoder utilizes 20 transistors this block is replaced with DVL and TG based logic [1] which consists of 14 transistors shown in below figure. We already known about transistor count is directly proportional to power consumption. So now we used same 2-4 decoder in our modified design. Total two 2-4 decodes generates total eight output lines. These two decoders are performed same operation but input ports are different. Here we observe 4 different inputs have 16 different combinations. Those combinations are given to the inputs of the 16 NAND gates. In modified design we mainly focused on the NAND gates. Existed design has CMOS based NAND gate which is modified by Gate Diffusion Induced [GDI] logic style. The design enhances the constraints in a best manner. CMOS and GDI based NAND gates are shown in below figures 4 and 5 respectively.

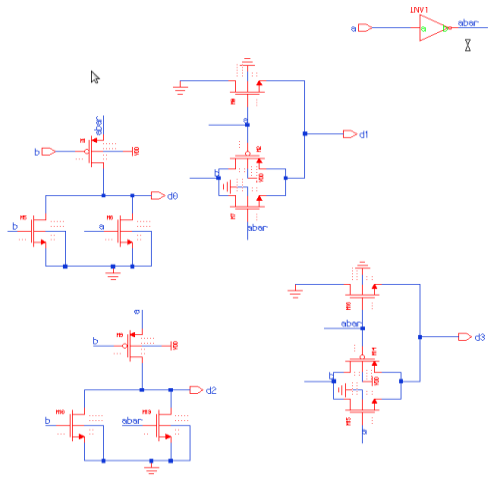


Figure 3: DVL, TG based 2-4 DECODER Design

B) NAND gate:

Total four transistors are used in two different NAND gates but the difference is the way to establish the connection between PMOS and NMOS transistors. First one is connected as pull-up to pull down setup and second one has two cascaded blocks. Output of the first block is connected to source of the second block NMOS transistor which gives better performance than previous.

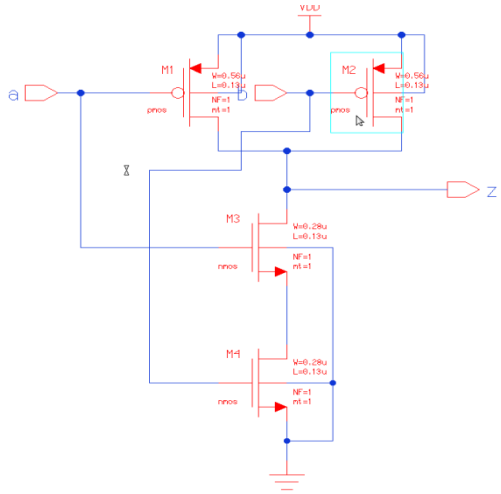
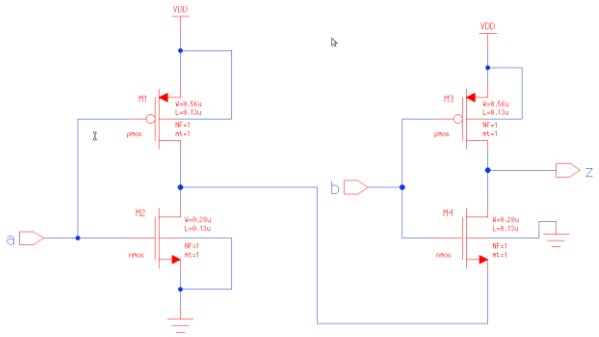


Figure 4: CMOS based NAND gate



(ii) GDI based NAND

III. PERFORMANCE EVALUTION

The present NAND gate is replaced with CMOS NAND in figure1 i.e 4-16 existed decoder. Existed design1 is implemented using CMOS logic style in entire design. In second existed design is implemented using DVL, TG logics in 2-4 decoders remaining NAND gates are implemented with CMOS logic style. In modified design, 2-4 decoders are implementing with DVL and TG logic styles but NAND gates are implemented by using GDI logic style. We observe total three designs of delay, power consumptions and power delay products at different supply and input voltages. The ranges of voltages are in between 0.4-0.8V. 16 different data outputs are observed when 16 different combinations of inputs shown in figure 6. The modified design has better results observed from below tables.

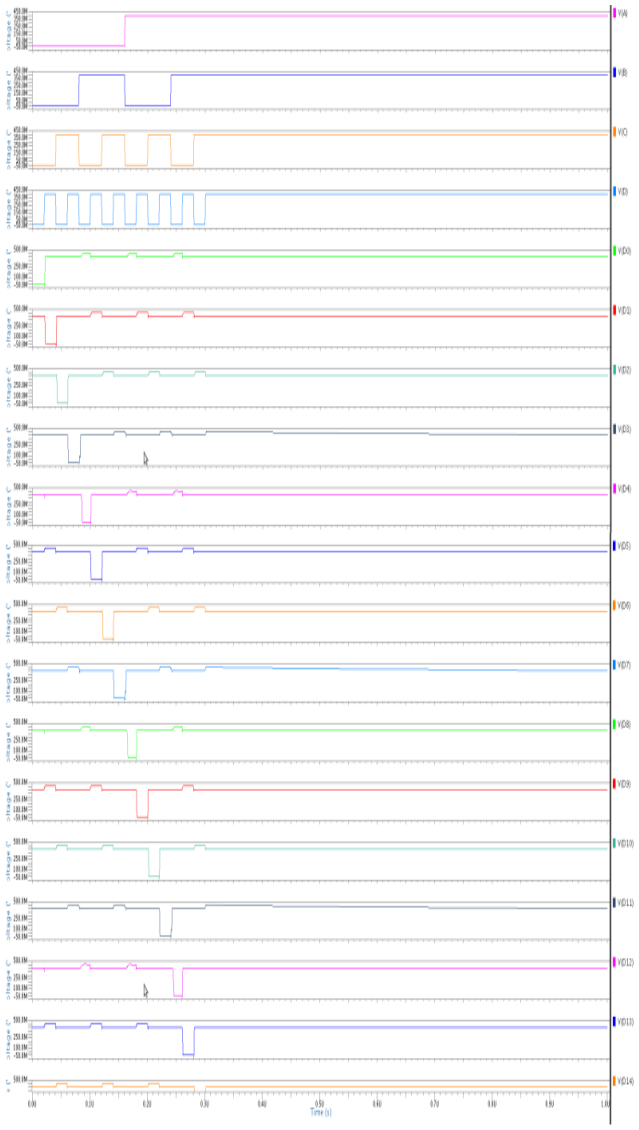


Figure 6: output waveform of modified 4-16 decoder

TABLE 1: Power consumption analysis between modified and existed 4-16 line Decoders

Designs	Vdd=Vgs=0.8V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified (TGL,DVL,GDI)	112.31nW	82.523nW	61.368nW	42.768nW	28.974nW
Existed (TGL, DVL, CMOS)	112.96nW	84.664nW	62.417nW	43.419nW	29.092nW
CMOS	23.297uW	12.198uW	5.529uW	1.780uW	386.69uW

TABLE 2: Delay analysis between modified and existed 4-16 line Decoders

Designs	Vdd=Vgs=0.8V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified (TGL,DVL,GDI)	532.11Ps	591.77Ps	705.78Ps	1.0139ns	2.2855ns
Existed (TGL, DVL, CMOS)	564.14Ps	633.44Ps	774.21Ps	1.1503ns	2.7170ns
CMOS	540.27Ps	716.06Ps	1.0316ns	1.7951ns	4.2008ns

TABLE 3: Power-Delay Product analysis between modified and existed 4-16 line Decoders

Designs	Vdd=Vgs=0.8V	Vdd=Vgs=0.7V	Vdd=Vgs=0.6V	Vdd=Vgs=0.5V	Vdd=Vgs=0.4V
Modified (TGL,DVL,GDI)	59.761×10-24	48.834×10-24	43.312×10-24	43.363×10-18	66.22×10-18
Existed (TGL, DVL, CMOS)	63.725×10-24	53.630×10-24	48.324×10-24	50.028 ×10-18	79.043×10-24
CMOS	12.587 ×10-21	8.949×10-21	5.70×10-15	3.196×10-15	1.624×10-24

IV. CONCLUSION

In this particular work 4-16 low level line decoder design is evaluated to improve the speed and power consumption as represented in the above tables. Total parameters of the design are enhanced with the help of [1] which is done by using MENTORGRAPHICS 130nm GDK technology. The GDI NAND based decoder can increase the performance than CMOS NAND based 4-16 decoder design. Modified design has 1nW less power than DVL, TG and CMOS based decoder design and 386uw less power than CMOS based decoder design at 0.4v. In terms of delay modified design reduces the 0.5ns than DVL, TG and CMOS based design and reduces 2ns delay than total CMOS based decoder. Due to these reason modified design gives better performance than remaining two.

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