

Extending the Reliability Scaling Limit of SiO₂ through Plasma Nitridation

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Abstract

We demonstrate a manufacturable remote plasma nitridation process that significantly extends the reliability scaling limit of SiO₂ based gate dielectrics.

Introduction

The reliability of aggressively scaled SiO₂ is a critical technology issue. It has been shown that 2.4 nm is the minimum SiO₂ thickness for reliable 1 V operation [1]. One aspect leading to this apparent limit is the thickness scaling behavior of the Weibull slope. The Weibull slope, used for area scaling and to project the lifetime to ppm fail fractions corresponding to low failure rates, decreases with oxide thickness and saturates at a value of 1, as shown in Figure 1. It was subsequently proposed that through extremely tight oxide thickness control, the resultant improvement in Weibull slope can extend the reliability scaling limit of SiO₂ [2]. The effectiveness of this approach is under debate [3].

The TDDB voltage model is given as $t_{50\%} = t_0 e^{-B \cdot V_G}$ [4,5], where $t_{50\%}$ is the mean time to fail, t_0 is the pre-factor, B is the voltage acceleration factor, and V_G is the gate voltage. One scaling trend that is favorable for reliability is the increase in the acceleration factor as gate voltage is reduced [6]. An investment in long stress times is required to take advantage of this entitlement.

In this work, we will demonstrate a manufacturable remote plasma nitridation process that significantly extends the reliability scaling limit of SiO₂, without requiring extremely tight thickness control or resorting to extended stress times. These improvements arise from reduced leakage, increased

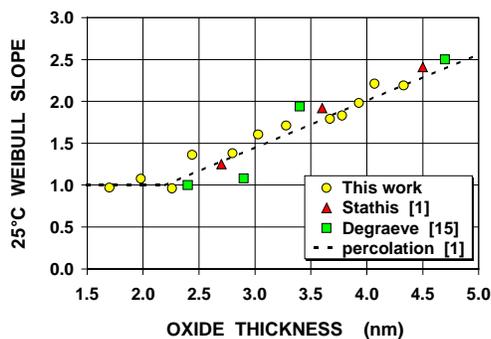


Figure 1. Weibull slope vs. oxide thickness. The Weibull slope saturates at 1 for tox < 2.4 nm.

Weibull slope, and higher voltage acceleration factor at elevated temperature due to the changes in film properties resulting from nitrogen incorporation.

Experiment

The gate dielectrics are 1.7 nm – 4.3 nm thick thermally grown SiO₂ films and remote plasma nitrided oxides (RPNO) [7]. RPNO films are fabricated by exposing oxides to a low energy nitrogen plasma. The advantage of this nitridation technique is that a relatively high level of nitrogen incorporation can be achieved without the deleterious effects of hydrogen. The plasma nitridation does not degrade channel mobility [8,9], while fully suppressing boron penetration from pMOS poly [7-9].

Constant voltage stress is performed on nMOS devices fabricated using a dual-poly full-flow CMOS process. Equivalent oxide thickness is determined from C-V matched quantum simulations [10]. Oxide areas range from 1×10^{-7} cm² to 4×10^{-4} cm². Failure is defined as the onset of soft breakdown. Lifetime is projected using the voltage model for TDDB [4,5]. Average failure rate (AFR) is calculated using Weibull statistics [11].

Results

A. Charge-to-breakdown and leakage current

Q_{BD} vs. gate voltage is shown for RPNO and oxide films in Figure 2 for equivalent oxide thickness (EOT) ≤ 2.7 nm, in the range where Q_{BD} does not vary significantly with thickness [1]. In Figure 2, it can be seen that Q_{BD} is generally the same or better for oxide. As shown in Figure 3, this is due to the higher trap generation rates per injected electron fluence (P_{gen}) in RPNO dielectrics, which is a consequence of exposing these films to a plasma during the nitridation process. It would seem that the reliability of RPNO is inferior to oxide. However, at a given EOT, the gate leakage current is significantly lower for RPNO films, as shown in Figure 4. The leakage reduction in RPNO occurs because 1) the incorporation of nitrogen is sufficiently high to increase the dielectric constant, allowing a physically thicker film for a given EOT, and 2) the presence of interfacial nitrogen increases the width of the sub-oxide transition region [12]. Since $t_{BD} = Q_{BD}/J_G$, the lower leakage in RPNO will make it possible to attain $t_{50\%}$ comparable to oxide.

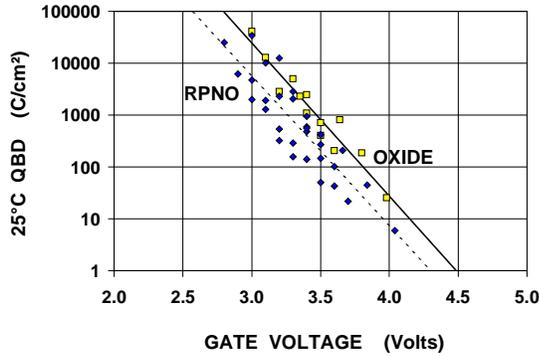


Figure 2. Q_{BD} vs. V_G for $t_{ox} < 2.7$ nm. Q_{BD} is generally the same or better for oxide.

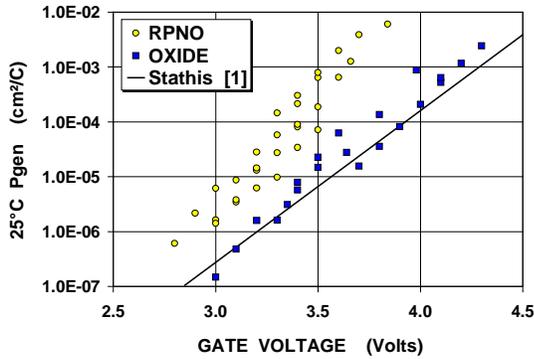


Figure 3. Bulk trap generation rates. P_{gen} is higher for RPNO. The solid line from [1] is shown for comparison.

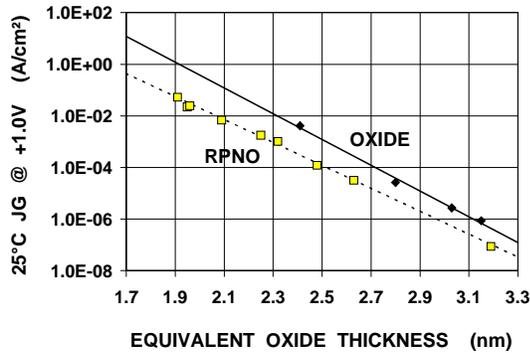


Figure 4. nMOS gate leakage current density at +1.0V. RPNO films have lower leakage at a given EOT.

B. Optimizing RPNO reliability

TDDDB data are shown in Figure 5. For $EOT > 2.4$ nm, $t_{50\%}$ is higher for oxide, but is comparable between oxide and RPNO for $EOT < 2.4$ nm. Inspection of Figure 5 shows that

the voltage model pre-factor t_0 is affected by plasma nitridation, whereas the acceleration factor at 25°C is relatively insensitive to RPNO processing.

It has been reported that non-uniform nitrogen profiles resulting from thermal N_2O treatments of oxide films give rise to spatially non-uniform trap generation, causing polarity asymmetry in the Weibull slope [13]. We will show that a similar effect is observed in RPNO, and utilize this result to optimize RPNO reliability. The stress polarity dependence of the RPNO critical bulk trap density at breakdown (N_{BD}), extracted from SILC measurements [14], is shown in Figure 6. N_{BD} becomes polarity independent below 2.4 nm thickness, where the nitrogen profile is uniform (confirmed by ToF-SIMS). Concurrently, the RPNO Weibull slope also becomes independent of stress polarity below about 2.4 nm, as shown in Figure 7. Bulk trap generation rates for RPNO are shown in Figure 8. The generation rate is sharply lower when the nitrogen profile is uniform. Since $t_{BD} = N_{BD}/P_{gen} * J_G$ [1], the reduction in generation rate accounts for the increase in the TDDDB pre-factor for EOT < 2.4 nm shown in Figure 5. From Figures 5-8, it can be concluded that mean time to failure comparable to oxide is attained (and RPNO reliability is optimized) when the nitrogen profile is uniform.

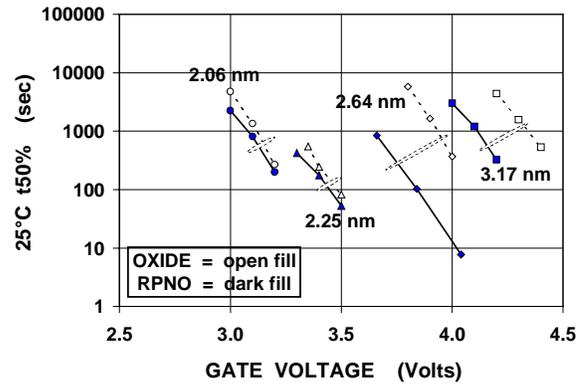


Figure 5. Oxide and RPNO $t_{50\%}$ vs. gate voltage. RPNO and oxide TDDDB data are comparable for EOT < 2.4 nm.

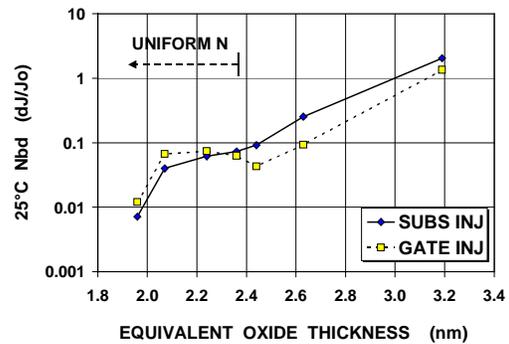


Figure 6. Polarity dependence of RPNO critical trap density at breakdown. N_{BD} is polarity independent below 2.4 nm.

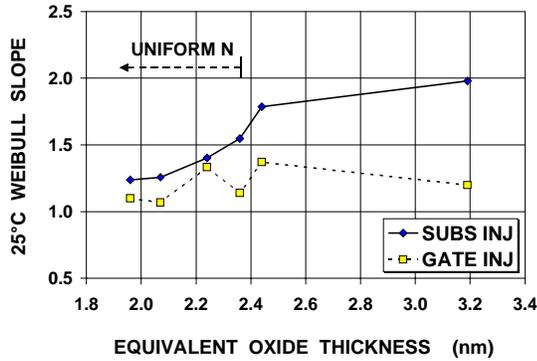


Figure 7. Polarity dependence of RPNO Weibull slope. The Weibull slope is polarity independent below about 2.4 nm.

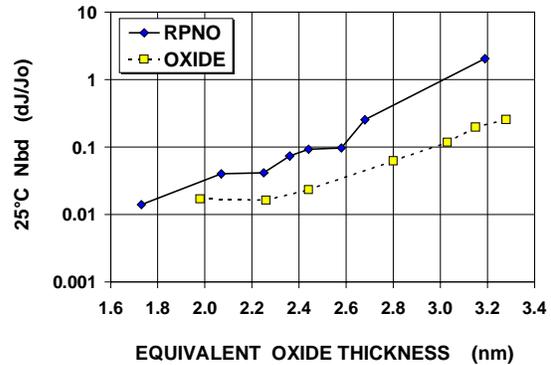


Figure 9. Oxide and RPNO critical trap densities at breakdown. At a given EOT, N_{BD} is higher for RPNO.

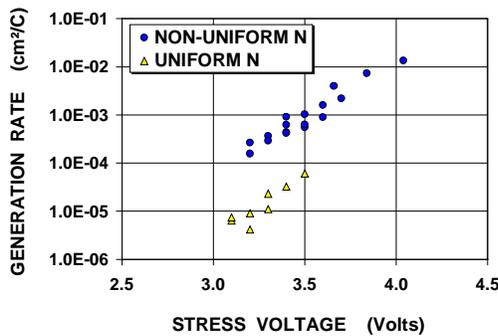


Figure 8. 25°C bulk trap generation rate after 10 C/cm² fluence. The trap generation rate drops abruptly when the RPNO nitrogen profile becomes uniform.

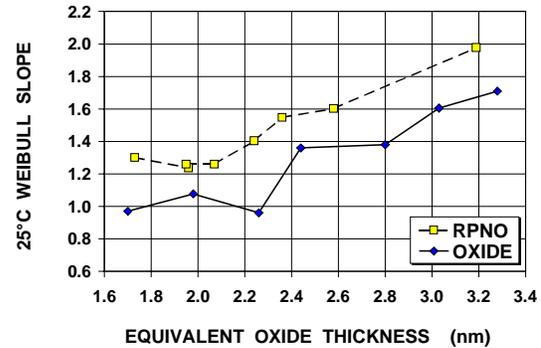


Figure 10. Oxide and RPNO Weibull slopes. RPNO processing increases the Weibull slope.

C. Critical trap density and Weibull slope

N_{BD} for oxide and RPNO films is shown in Figure 9. At a given EOT, the trap density required to cause breakdown is higher for RPNO. This is partially due to the larger physical thickness for RPNO at a given EOT. Similarly, at a given EOT, the Weibull slope is also higher for RPNO, as shown in Figure 10. Below about 2.1 nm EOT, the RPNO Weibull slope saturates at a value of about 1.3, representing a significant improvement over oxide. Although the RPNO Weibull slope saturates at a 0.2 - 0.3 nm thinner EOT than oxide, the physical thickness at saturation is about the same (2.4 nm). Therefore, to first order, the lower EOT at saturation does not appear to be due to a reduction in trap radius in RPNO. A possible interpretation of the higher RPNO Weibull slope at saturation, inferred from percolation theory [1,15,16], is that a smaller fraction of the generated trap states in RPNO participate in breakdown compared to oxide.

D. Behavior at elevated temperature

It has been reported that thin oxide acceleration factors are weakly dependent on temperature [17]. Our findings are similar, as shown in Figure 11. It can also be seen that RPNO and oxide acceleration factors are comparable at 25°C. However, in contrast to oxide, the acceleration factors of RPNO films increase at 105°C. Additional work is needed to relate the microscopic trap properties to the observed TDDB temperature dependence of RPNO films.

For optimized RPNO films with uniform nitrogen profiles, the higher Weibull slopes and 105°C acceleration factors result in a significant improvement in product reliability under worse case conditions. The maximum safe supply voltage using a reliability criteria of 10 FIT AFR for 100,000 hours operation at 105°C for 0.1 cm² area is shown in Figure 12. The oxide data, appropriately normalized, are comparable to the results reported in [1]. For 1.2 V worse case operation, the RPNO EOT can be safely scaled about 0.6 nm thinner than oxide for the reliability criteria specified.

References

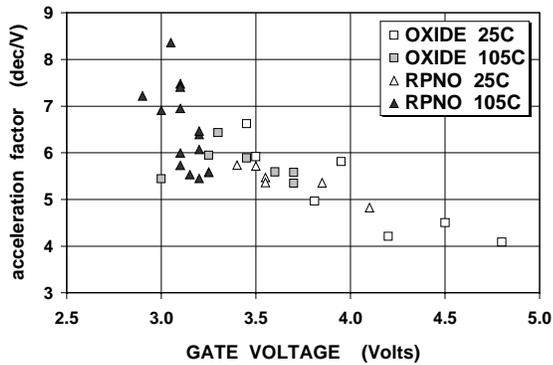


Figure 11. Voltage model acceleration factors vs. gate voltage. RPNO acceleration factors are higher than oxide at 105°C.

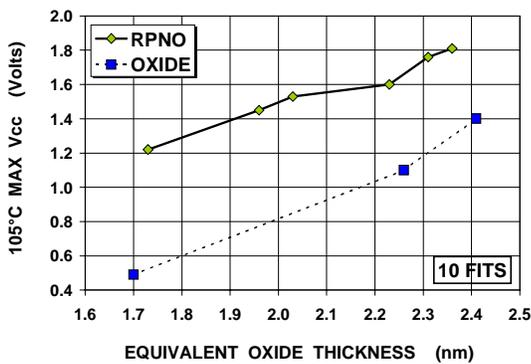


Figure 12. Maximum safe operating voltage for 10 fit AFR for 100,000 hours operation at 105°C for 0.1 cm² gate area. For RPNO, data are shown only for films with uniform nitrogen profiles. RPNO significantly improves the reliability of SiO₂.

Conclusions

An RPNO process, optimized by obtaining a uniform nitrogen profile, overcomes the reliability scaling limitations of SiO₂ without requiring extremely tight thickness control or resorting to extended stress times. These benefits result from reduced gate leakage, increased Weibull slope, and higher voltage acceleration factor at elevated temperature. For the conditions specified, the RPNO thickness can be safely scaled about 0.6 nm thinner than pure oxide at 1.2V worst case operation. Further studies at lower gate voltages and thinner EOT will be needed to evaluate how far this trend extends.

- [1] J. H. Stathis and D. J. DiMaria, "Reliability Projection for Ultra-Thin Oxides at Low Voltage," in *IEDM Tech. Digest*, 1998, pp. 167-170.
- [2] B. E. Weir, et. al., "Gate Oxides in 50 nm Devices: Thickness Uniformity Improves Reliability," in *IEDM Tech. Digest*, 1999, pp. 437-440.
- [3] E. Y. Wu, E. J. Nowak, R. P. Vollertsen, "Can Macroscopic Oxide Thickness Uniformity Improve Oxide Reliability?," *Elec. Dev. Lett.*, Vol. 21, No. 8, pp. 402-404, Aug. 2000.
- [4] R. Degraeve, et. al., "Temperature Acceleration of Oxide Breakdown and its Impact on Ultrathin Gate Oxide Reliability," in *Proc. VLSI*, 1999, pp. 59-60.
- [5] P. E. Nicollian, W. R. Hunter, J. C. Hu, "Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides," in *Proc. IRPS*, 2000, pp. 7-15.
- [6] M. A. Alam, J. Bude, A. Ghetti, "Field Acceleration for Oxide Breakdown – Can An Accurate Anode Hole Injection Model Resolve the E vs. 1/E Controversy?," in *Proc. IRPS*, 2000, pp. 21-26.
- [7] S.V. Hattangady, et. al., "Ultrathin Nitrogen Profile Engineered Gate Dielectric Films," in *IEDM Tech. Digest*, 1996, pp. 495-497.
- [8] D.T. Grider, et. al., "A 0.18 μm CMOS Process Using Nitrogen Profile Engineered Gate Dielectrics," in *Proc. VLSI*, 1997, pp. 47-48.
- [9] M. Rodder, et. al., "A 1.2V, 0.1μm Gate Length CMOS Technology: Design and Process Issues," in *IEDM Tech. Digest*, 1998, pp. 623-626.
- [10] C. Bowen, et al., "Physical Oxide Thickness Extraction and Verification Using Quantum Mechanical Simulation," in *IEDM Tech. Digest*, 1997, pp. 869-872.
- [11] W. R. Hunter, "A Failure Rate Based Methodology for Determining the Maximum Operating Gate Electric Field, Comprehending Defect Density and Burn-in," in *Proc. IRPS*, 1996, pp. 37-43.
- [12] H. Yang, H. Niimi, J. W. Keister, G. Lucovsky, J. E. Rowe, "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices," *Elec. Dev. Lett.*, Vol. 21, No. 2, pp. 76-78, Feb. 2000.
- [13] R. Degraeve, et. al., "A New Polarity Dependence of the Reduced Trap Generation During High-Field Degradation of Nitrided Oxides," in *IEDM Tech. Digest*, 1996, pp. 327-330.
- [14] D. J. DiMaria and E. Cartier, "Mechanism for Stress-Induced Leakage Currents in Thin Silicon Dioxide Films," *J. Appl. Phys.*, Vol. 78, No. 6, pp. 3883-3894, 15 Sept. 1995.
- [15] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, H. E. Maes, "A consistent Model for the Thickness Dependence of Intrinsic Breakdown in Ultra-thin Oxides," in *IEDM Tech. Digest*, 1995, pp. 863-866.
- [16] D. J. DiMaria, "Ultimate Limit for Defect Generation in Ultra-Thin Silicon Dioxide," *Appl. Phys. Lett.*, Vol. 71, No. 22, pp. 3230-3232, 1 Dec. 1997.
- [17] E. Y. Wu, W. W. Abadeer, L-K. Han, S-H. Lo, G. R. Hueckel, "Challenges for Accurate Reliability Projections in the Ultra-Thin Oxide Regime," in *Proc. IRPS*, 1999, pp. 57-65.