International Journal of Modern Science and Technology, 2021;6(10-11):171-174.
ISSN: 2456-0235.
www.ijmst.co

Research Article

A High Speed and Low Leakage 12-T SRAM for Truncated Power Applications

P. S. Vinishya*, K. Solangkili

Department of Electronics and Communication Engineering,
Arasu Engineering College, Chennai Main Road, Kumbakonam, India.

*Corresponding author's e-mail: er.vinishya@gmail.com

Abstract

High speed and low leakage constraints are put on the 12-T SRAM cell. Truncated power integrated circuits are massively fascinating for portable and wearable applications. A twelve-transistor SRAM circuit is proposed in this paper. The SRAM cells are designed with dual gate transistor for every column in order to achieve low leakage and high speed operation. An error margin is reduced up to 10% based on device size and capacitive load during read-out scheme. The data stability as well as read /write ability is based on standard topology which in turn reduces read /write delay.

Keywords: System on Chip; 12T SRAM; Integrated circuits; Wireless sensor application.

Introduction

In this modern world, the demand of ultra-low power consuming devices near threshold operation is growing exponentially. These devices have to be compact as well as perform multiple functions [1]. In digital system there is need for storing and retrieving large amount of data at high speeds without dissipating too much power. If there is less area there will be more compactness and low power consumption.

The factors like portability, battery life as well as performance have directed the research efforts towards decreasing power using power gated. Earlier speed and size were the design goals. But nowadays, the prime objective has included reducing the size as well as power [2]. Device scaling is the technique used to achieve the above two objectives. For this device scaling, the two parameters that are treated the size of the transistor and the operating voltage. The dimension reductions directly have an impact on the data stability. The knowledge and analysis about the stability of the SRAM cells is a research on circuit techniques which operates with low power supply.

Memories are used to store the program code, data and also references like Look Up Table (LUT). Bandwidth and memory of the system controls the application performance. So, the performance of the memory should be equal to the performance of the processor. This can be achieved by using various improved memory techniques. System on Chip (SOC) is mainly occupied by the memory blocks [3]. High performance can be achieved by a single memory cell. There are Cache memory- which consist of very fast SRAM integrated with the processor and Main memory- which consist of DRAM chips on DIMM packaged in various ways.

The memories are generally classified based on data storage and data access. These memories exhibit two stable states, either a '1' or a '0'. The volatile and non-volatile memories are the two types of CMOS memories [4]. If the power is switched off, the information will be erased in volatile memory. If the power is switched off, the information will be restored in non-volatile memory.

The 12-T SRAM memory cell contains two cross coupled inverter circuits, it has 2 stable states they are logical "0" and "1". Totally six transistors are needed to access the memory cell throughout the scan and write operations. This creates 6T memory cells. Sometimes further transistors are used to give either 1oT or 12T memory cells. These additional transistors are used to give additional ports in a register file of the SRAM memory cell. Though associate 3 terminal switch devices may be utilized in an SRAM, CMOS and MOSFET's technology is generally wont to make sure that terribly low levels of power consumption and low leakage is

Received: 05.10.2021; Received after Revision: 20.10.2021; Accepted: 21.10.2021; Published: 01.11.2021.

achieved with high speed in read and write operations of SRAM memory cells [5]. With semiconductor recollections of 12-T SRAM memory cells every cell should win a really low leakage ultra-low level of power consumption. These extra transistors square measure won't to offer either such implementing extra ports during a register file, etc. for the SRAM memory.

HVT cross-coupled inverters are used to store the data in the proposed 12-T SRAM cell. Stacking technique which is used in tri-buff SCM cell is not employed for the inverter. Data is warehoused in the cross-coupled inverters. The write enable signal WEN is maintained at 0V. The proposed 12T SCM based SRAM circuit is shown in fig. 1. The write bit line signal WBL generates WBL_P and WBL_N signals, which are used to govern the two column- wise shared transistors PT and NT respectively. Sharing PT and NT by the whole column, the WBL load is reduced intensely.[6] Furthermore, by placing PT and NT outside the memory array, the area efficiency of the memory array is enhanced as compared to the tri-buff SCM circuit. The read delay and read power consumption are thereby reduced due to PT and NT.

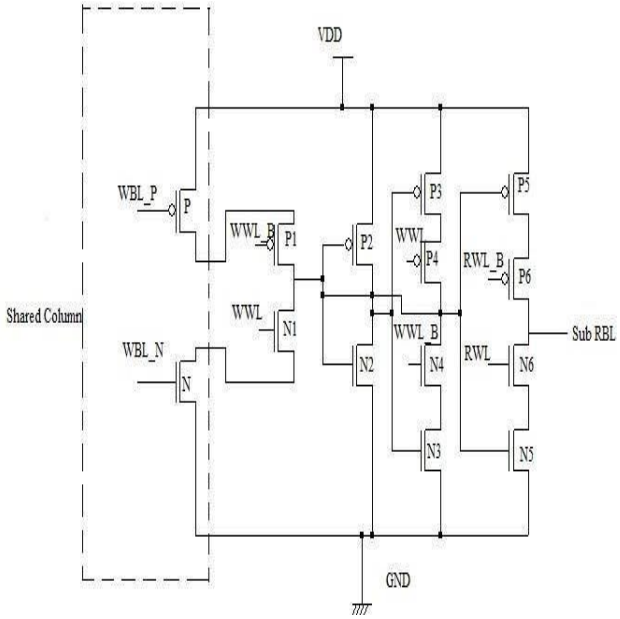

Fig. 1. 12-T SCM SRAM circuit

The write operation

During the write operation, WEN and WWL state transitions are high "1". The data transfers are all enabled by NAND, NOR logic cells and P1 and N1 signals. When the input is "1" and both WBL_P and WBL_N transition are low then WBL is charged to VDD and PT is turned on, while NT is turned off. The transistor Q is charged through PT and P1, when logic "1" is moved into the SRAM cell [7]. Alternatively, when the input data is "0", WBL_P and WBL_N transitions are high then WBL is discharged to ground and NT is turned on, while PT is turned off. The transistor Q is discharged through NT and N1 when logic "0" is moved into the SRAM cell. WBL drives the NAND and NOR logic cells.

The read operation

During the read operation, RWL transitions is enabled high "1". P5, P6, N5 and N6 in the read buffer are enabled. The transistor Q in which the data is stored propagates to Sub-RBL. Address selection method activates the tri-state buffer which lies between the Sub-RBL and the Global-RBL [8]. The data successively transferred to the Global- RBL. The proposed SRAM cell drives a single Sub-RBL and Global-RBL when compared to tri buff SCM, which prompts ultra-low power consumption, high speed read operation. A high read static noise margin is maintained when the data storage nodes are isolated from the read bit line RBL.

The hold mode

The signals WWL, WEN and RWL are maintained at 0V initially. The cross-coupled inverters will store the data during hold mode. WBL_P and WBL_N are therefore maintained at VDD and 0V, respectively [9]. PT, NT, P1 and N1 are turned off, since the SRAM cell suppresses the leakage current through PT, P1, N1 and NT. On the read port, all the tri-state buffers are switched off to isolate the data access and guarantee low leakage currents on the read port.

Leakage power estimation

The device width is determined first in order to calculate the active power estimation and leakages in SRAMs. The device widths are calculated by the operative sizes of PMOS and NMOS transistors. The PMOS transistor operative sizes are assumed to be twice the operative size of NMOS transistors [10]. The size the dimensions of the memory cell are known. The active power, leakage power and speed of operation are designed by the user.

The fig. 2 shows the flow diagram for leakage power estimation which is calculated using capacitive width. The methodology starts by calculating the capacitive loads on the SRAM cell, because the size of the cell depends on the capacitive loads driven by them. The set of analytical models in this methodology are used for determining the cell sizes.

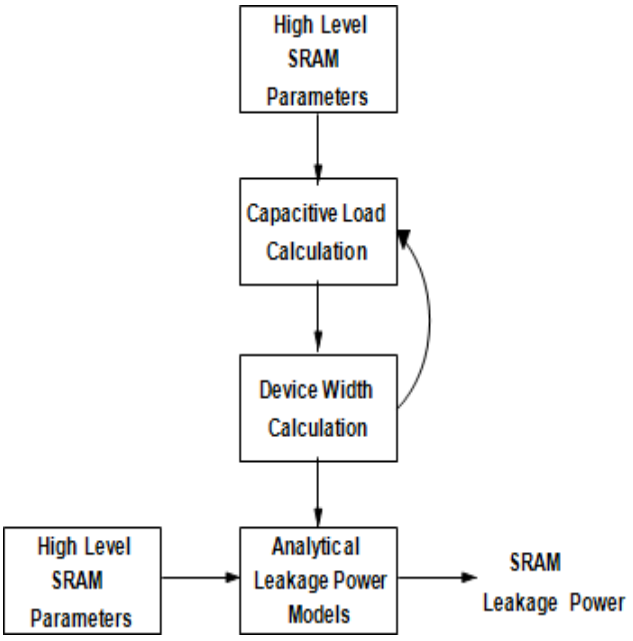

Fig. 2. Block diagram for truncated power calculation

Since the capacitive load calculation is an iterative process that continues until the transistor widths are determined [5]. For example, for calculation of the width of the bit line pre charge logic, the capacitive load on the bit line needs to be calculated as shown in equation given below, The width of the PMOS charges the transistor, then biplane capacitance (*CBP*) and charging time, which is derived from a fraction of the frequency of operation were calculated. Calculation of device sizes of the pre-charge driver in the read control logic is done by finding the capacitive load which is derived from pre charge transistor width.

$$C_{BP}=N(Mc+Mh)+3.C_d$$

Where, *Mc* indicates the metal capacitance per unit microns, *Mh* indicates the height of the memory cell in microns, *Cd* indicates the drain capacitance per unit microns [7]. After obtaining the required transistor widths the analytical models are illustrated for estimating leakage power in SRAMs.

The cadence EDA tool

Purpose of cadence design systems

Cadence *EDA* tool is designed have a shared structure which consists of public library, opinions, and illustrations. The design data in Cadence EDA tools are organized in public library. The steps involved in cadence EDA tools are (1) engender the design, (2) investigate the design, (3) to make a layout, (4) authentication. The simulator offers a wide range of results that can be saved. Cadence EDA Tool product offers various platforms for design and functional verification task which include: (i) Virtuoso Platform - Tools for operating IC's [4]. It is mainly for continuous Radio Frequency signals, and to design the layout. (ii) Encounter Platform - Digital IC's creation tool that includes floor planning, synthesis, test, and place and route. (iii) Perceptive – Verilog and VHDL Tools for simulation and functional verification of RTL using (iv) Palladium verification Platform – Hardware and software co-design are performed by accelerators and emulators. (v) Internet Protocol design – IP is designed for DRAM'S, Wide I/O non-volatile memory, high-performance interface protocols. (vi) Internet Protocol Verification - Broadest set of Internet Protocol Verification are available including USB, AMBA, PCI , MIPI, SATA, OCP, SAS, and many.

Compliance Management System (vii) Internet Protocol optimization - Tools for Digital Controller and Device Driver. USB, DDR, PCI, 10G-40G Ethernet, and On Chip Bus Fabric are supported by optimization IP. (viii) Allegro Platform - Tools for hardwarwe and software co-design. (ix) OrCAD/PSpice – simulation software for PCB Design (x)Sigrity technologies - Tools for calculating the signal power for level sign off systems and interface amenability.

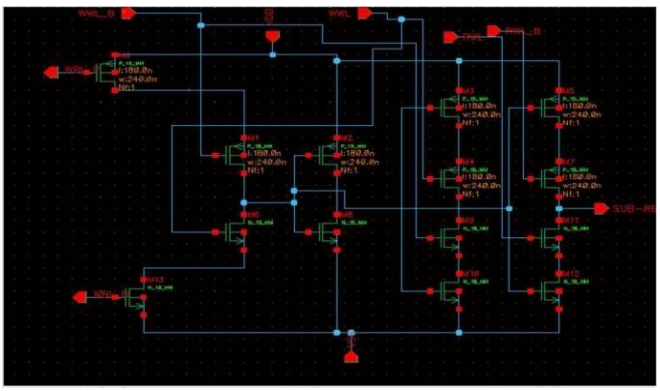

Fig. 3. Schematic of 12-T SRAM

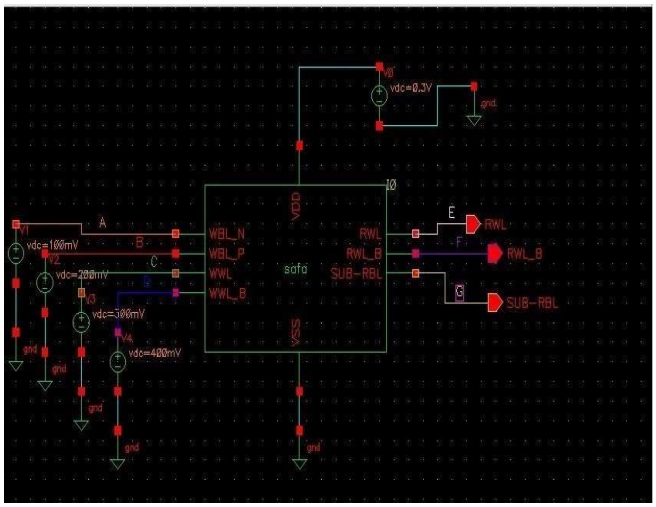

Fig. 4. Test circuit of 12-T SRAM

Conclusion

The 12-T SRAM cell is proposed for high speed read and writes operation and low leakage power is achieved during the operation performed by the memory. The read and write power utilization per operation is reduced up to 92% as compared to the existing circuit. The proposed 12-T SRAM cell circuit is mostly applicable for portable and wearable usage. This 12-T SRAM cell is now widely used in wireless sensor application in which the sensors need memory for storing their data in the memory.

Conflict of interest

The authors declare no conflict of interests.

References

[1] Upadhyay P, Nidhi A, Kar R, Mandal S, Ghoshal SP. Power and Stability Analysis of a Proposed 12T MTCMOS SRAM Cell for Low Power Devices"(2014).

[2] Upadhyay P, Sarthak G, Kar R, Mandal D, Ghoshal SP. Low Static and Dynamic Power MTCMOS Based 12T SRAM Cell for High Speed Memory System. 11th International joint Conference on Computer science & software engineering (JCSSE), 2014.

[3] Do AT, Jeremy YSL, Joshua YLL, Zhi-Hui K, Xiaoliang T, KiatSeng Y. An 8T Differential SRAM With Improved Noise Margin for Bit-Interleaving in 65 nm CMOS. IEEE Transactions on Circuits and Systems-I, 2011;58:1252-63.

[4] Nam SK, Stark CD, Shi TZ, Sumeet K, Hamid RG, Taejoon P. Analyzing the Impact of Joint Optimization of Cell Size, Redundancy, and ECC on Low-Voltage SRAM Array Total Area. IEEE Transactions on Very Large Scale Integration Systems 2012;20:2333-37.

[5] Sina H, Milad Z, Khosrow H. A 32kb 90nm 10T-cell Sub-threshold SRAM withImproved Read and Write SNM. 2013 21st Iranian Conference on Electrical Engineering (ICEE). 14-16 May 2013 Mashhad, Iran.

[6] Mohan S, Anitha A, Deepa R. Design of low power 8T SRAM cell. International Conference on Communication and Signal Processing, April 3-5, 2014.

[7] Basavaraj M, Kariyappa BS. Single Bit-line7T SRAM cell for Low Power and High SNM. 2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s). 22-23 March 2013. Kottayam, India.

[8] Abdul Halim ISA, Basemu NH, Hassan SLM, Rahim AAA. Comparative Study on CMOS SRAM Sense Amplifiers using 90nm Technology., 2013 International Conference on Technology, Informatics, Management, Engineering & Environment (TIME-E 2013). June 23-26, 2013. Bandung, Indonesia.

[9] Achiranshu G, Tony THK. SRAM Array Structures for Energy Efficiency Enhancement. IEEE Transactions On Circuits And Systems-II: Express Briefs 2012;60:351-5 .

[10] Prashant U. Rajesh M, Niveditta T. Low Power Design of an SRAM Cell for Portable Devices. International Conference on Computer and Communication Technology (ICCCT). 17-19 Sept. 2010. Allahabad, India.

****

