Device Characteristics and Equivalent Circuits for NMOS Gate-to-Drain Soft and Hard Breakdown in Polysilicon/SiON Gate Stacks

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***Abstract*—In state-of-the-art technologies, the currents in all n-channel field-effect transistor device terminals can be severely degraded when a soft or hard dielectric breakdown event occurs from gate-to-drain. The equivalent circuits that are commonly used for modeling gate-to-drain breakdown do not adequately capture all of the salient features of post breakdown device characteristics and can yield results that are overly optimistic. We present an equivalent circuit comprehending both soft and hard breakdown that can be used to accurately model gate, drain, and source currents following a breakdown event from gate-to-drain.**

***Index Terms*—Breakdown, dielectric, oxide, reliability, SiON, time-dependent dielectric breakdown (TDDB).**

I. Introduction

HISTORICALLY, the time to breakdown used to assess the reliability of gate dielectrics has been taken as the first breakdown event. However, it has been reported that some circuits remain operative after the first breakdown [1]–[4]. If the time to failure can be extended beyond the first breakdown, the corresponding relaxation in the reliability requirements can enable higher safe operating voltage to achieve higher performance. It is therefore desirable to have the capability to simulate the effects of breakdown on circuit functionality, which is often done using simulation program with integrated circuit emphasis (SPICE) modeling [1], [2], [5], [6]. To achieve this goal, an equivalent circuit that replicates post breakdown transistor electrical characteristics is needed.

This paper focuses on dielectric breakdown from gate-to-drain because the degradation in device characteristics can be particularly severe when it occurs, even when it is a soft breakdown (SBD), as shown in Fig. 1. For this device with a post-SBD effective resistance (R_{EFF}) of 50 KΩ, the linear region drain current (I_{DLIN}) changes polarity (from positive to negative) as a result of the SBD. This means that the post breakdown conductance between the gate and the drain has become sufficiently high that the net electron flow resulting in drain current is no longer from source-to-channel-to-drain but is rather due to electrons entering the drain from the external circuitry and flowing out the gate contact, as shown in Fig. 2.

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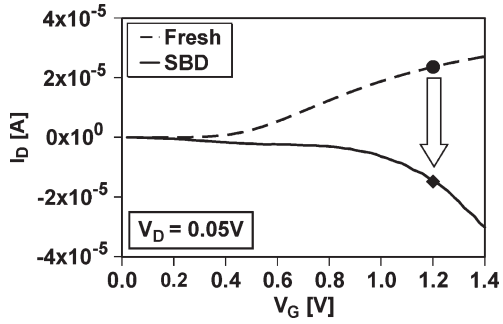

Fig. 1. I_D versus V_G before and after gate-to-drain SBD. The post-SBD R_{EFF}(1.0 V) is 50 KΩ. The degradation is so severe that I_{DLIN} (symbols) changes sign.

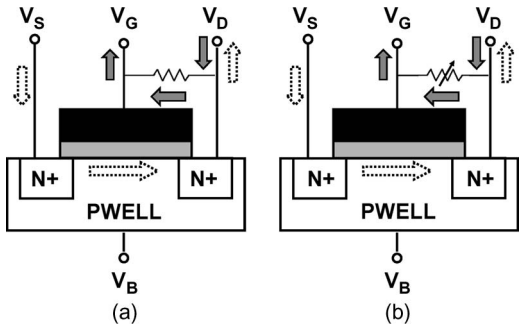

Fig. 2. Equivalent circuit diagrams for (a) the single gate-to-drain resistor (R_{EFF}) model. (b) The gate-to-drain conductor (G_{EXT}) model. In both drawings, the three open fill arrows show the direction of net electron flow that will result in $+I_D$ (fresh device) and the three gray fill arrows show the direction of net electron flow that will result in $-I_D$ (post breakdown).

The severity of gate-to-drain dielectric breakdown may be due to one or a combination of the following: 1) the low resistance of the drain extension region [7]; 2) the energy, which is proportional to the square of the charge, that is dissipated during the breakdown between the gate and the strongly accumulated drain extension; and 3) the microscopic details of gate-to-drain breakdown path [8]. Breakdown from gate-to-drain becomes more prevalent as channel length is reduced because the drain extension region becomes a larger fraction of the channel length. The fraction of the first breakdowns that are from gate-to-drain also depends on current compliance because the breakdown path rapidly evolves toward the source/drain as the current during the breakdown transient increases [8]. For our devices, all the breakdowns that we observe are from

gate-to-drain or from the gate-to-source when the current exceeds 4×10^{-4} A. Gate-to-drain breakdown is more problematic than a gate-to-body breakdown since an input/output node failure is more probable.

For gate-to-drain breakdown, equivalent circuits employing resistors [1], [5], [9], a combination of diodes and resistors [2], [10], and current sources [4], [6] are commonly employed in device simulators. In this paper, we will analyze the device characteristics after gate-to-drain breakdown and compare them with an *experimental investigation* of equivalent circuit models that incorporate device elements between the gate and the drain, as shown in Fig. 2. We will show that in the models where gate-to-drain breakdown includes components solely between the gate and drain terminals, the degradation in the drain current is severely underestimated, except when $|V_{GD}| \gg 0$. Moreover, the effects of the breakdown on the source current, which plays a critical role in inverter stability, are not captured. The "Potentiometer Model" [11], which incorporates three resistors: from gate-to-drain, gate-to-source, and gate-to-body, still does not adequately describe I_S after gate-to-drain SBD because the coupling between device terminals is more complicated than this configuration. Indeed, degradation in all terminal currents after gate-to-drain breakdown is still observed when $V_G = V_D$ (e.g., mid-voltage).

We present our equivalent circuit model for inverted n-channel field-effect transistors (NFETs) that correctly accounts for the gate, drain, and source currents for soft and hard breakdown across the entire range of drain and gate voltages that an NFET would experience in a circuit. The equivalent circuit is verified and tuned through BSIM4.4.0 simulations [12] and is suitable for insertion into SPICE modeling of circuit reliability.

II. Experiment

N-channel metal–oxide–semiconductor devices with polysilicon gate electrodes and 1.7-nm equivalent oxide thickness SiON gate dielectrics from a 65-nm process are subjected to constant voltage stress at 378 K until a pre-set compliance is reached. The compliance current is varied from 2×10^{-4} A to 2.0×10^{-3} A to obtain a distribution of post breakdown conductance. These current levels are commonly encountered in logic circuits. We define that a hard breakdown (HBD) has occurred when the slope of a log I_G versus log V_G curve is equal to one (ohmic behavior). In our devices, HBD is not observed for $R_{\mathrm{EFF}} >\sim 4$ KΩ. The transistor W/L is 0.5 μm/0.15 μm, and the breakdown position X_{BD}/L is determined using the ratio method [7].

The data from the actual broken down devices are compared to resistor (R_{EXT}) and conductor (G_{EXT}) models by characterizing fresh devices with a fixed or variable external resistor inserted between the gate and drain terminals, as shown in Fig. 2, where the G_{EXT} model emulates the actual I_G–V_G behavior of a broken down device. For the R_{EXT} model, the currents at a constant resistance are compared to the post breakdown data at a fixed V_G (e.g., 1.2 V for I_{DLIN}). For both R_{EXT} and G_{EXT} models, the degradation is taken as the percentage difference between the currents with and without the resistors attached.

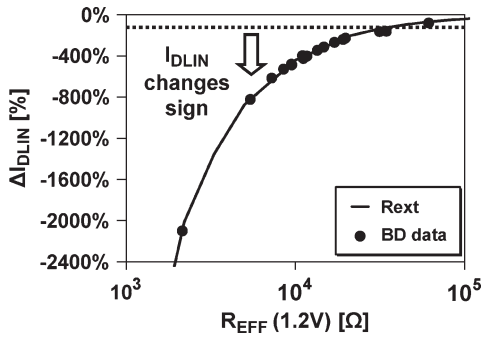

Fig. 3. ΔI_{DLIN} versus R_{EFF} comparing broken down devices to the single resistor model. When $-\Delta I_{\mathrm{DLIN}}$ exceeds 100%, I_{DLIN} has changed polarity.

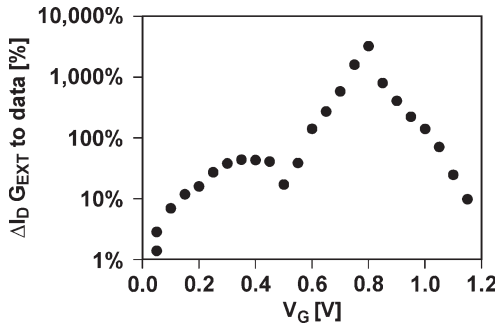

Fig. 4. Difference in I_D between SBD data ($R_{\mathrm{EFF}} = 10$ KΩ) and the G_{EXT} model. V_G is ramped from 0 V to 1.2 V while V_D is swept from 1.2 V to 0 V. The G_{EXT} model significantly underestimates the change in I_D for most of the voltage sweep.

III. Device Characteristics

In Fig. 3, ΔI_{DLIN} is compared between the SBD devices and the R_{EXT} model, as defined in Fig. 2(a). The R_{EXT} model is an excellent fit to the data for both SBD and HBD. Below about 60 KΩ, I_{DLIN} changes sign. While the collapse of I_{DSAT} (although it does not change sign) in narrow W devices has been published [13], we are unaware of any reports where breakdown changes the polarity of I_{DLIN}, which it does to extreme levels in our devices. Note that for the I_{DLIN} measurement, $V_{GD} \gg 0$. ΔI_{GLIN} is also in good agreement with the resistor model (not shown).

For SBD, the I_G–V_G relationship is nonlinear and either follows an exponential law [14] or a power law [15], [16]. The diode model [2], [10] simulates the exponential law, whereas the current source models [4], [6] simulate the power law. The G_{EXT} model configuration in Fig. 2(b) is used to emulate these nonlinear transport mechanisms. We will vary V_G and V_D in a manner similar to what would be experienced in a switching waveform, i.e., as V_G is ramped from 0 V to 1.2 V, V_D is ramped from 1.2 V to 0 V. The difference in I_D between an actual SBD device and the experimentally measured G_{EXT} model is shown in Fig. 4. Except when $|V_{GD}| \gg 0$, the G_{EXT} model significantly underestimates the degradation in I_D. The source current is compared between the G_{EXT} model and the SBD data in Fig. 5. The G_{EXT} model shows no change in I_S at any bias and remains up to 130% higher than the SBD data. The gate current of an SBD device with all terminals connected, and with the source floating, is shown in Fig. 6. After gate-to-drain breakdown, the source has a negligible effect ($< 2\%$) on the

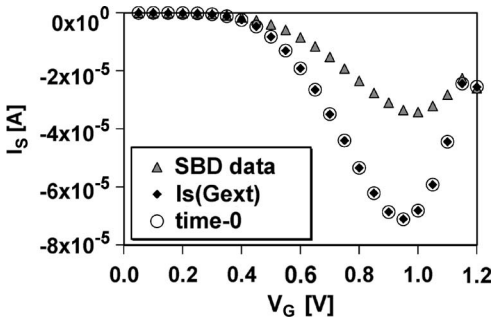

Fig. 5. Comparison of I_S between SBD data ($R_{\rm EFF} = 10$ KΩ) and the $G_{\rm EXT}$ model. V_G is ramped from 0 V to 1.2 V while V_D is swept from 1.2 V to 0 V. The $G_{\rm EXT}$ model shows no change in I_S and remains up to 130% higher than the data.

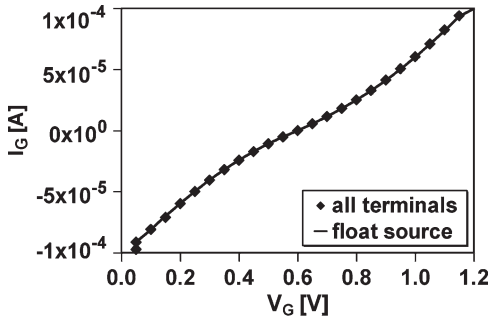

Fig. 6. The gate current after SBD ($R_{\rm EFF} = 12$ KΩ) with all terminals connected, and with the source floating. V_G is ramped from 0 V to 1.2 V while V_D is swept from 1.2 V to 0 V. After gate-to-drain SBD, the source has negligible effect on I_G.

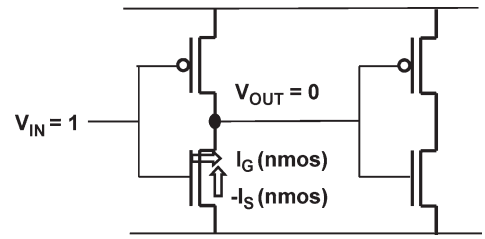

Fig. 7. The equilibrium condition $I_G = -I_S$ at the output node of an inverter where $V_{\rm IN} = 1$. $V_{\rm OUT}$ will rise to the voltage where equilibrium occurs.

gate current. Accordingly, the source current is not coupled to the gate current after SBD. The net effect of SBD on the source current is that the device is weaker and may fail in conditions where the $R_{\rm EXT}$ and $G_{\rm EXT}$ models will pass it. This is further elucidated in Fig. 7, where the charge at the output node of an inverter with $V_{\rm IN} = 1$ is controlled by the gate and source currents. $V_{\rm OUT}$ rises to the value corresponding to the equilibrium condition $I_G = -I_S$. This is illustrated for an SBD device in Fig. 8, where $V_{\rm OUT}$ rises up to 0.45 V, which exceeds the threshold voltage of the NFET in the next stage. Accordingly, this inverter is unstable, and the output flips from 0 to 1. The same analysis is performed for the $G_{\rm EXT}$ model, as shown in Fig. 9. $V_{\rm OUT}$ only rises up to 0.15 V; so according to this model, the inverter is stable, in contradiction to the SBD data. A comparison of Figs. 8 and 9 shows that this is primarily due to the underestimation of ΔI_S in the $G_{\rm EXT}$ model.

ΔI_D versus ΔI_S with $V_{GD} = 0$ is plotted in Fig. 10 for SBD and HBD. Despite there being no potential difference

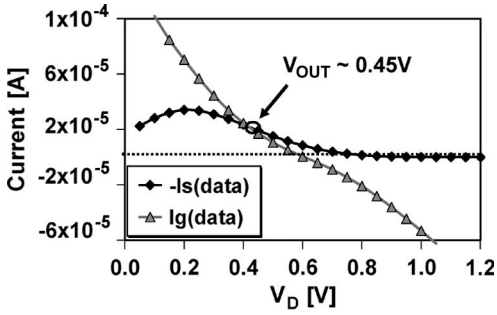

Fig. 8. I_G and I_S versus V_D ($V_{\rm OUT}$) for an SBD device ($R_{\rm EFF} = 10$ KΩ), where V_D is swept from 0 V to 1.2 V while V_G is swept from 1.2 V to 0 V. The output node in Fig. 7 rises up to 0.45 V, which exceeds the threshold voltage of the NFET in the next stage. Accordingly, the output will flip from 0 to 1.

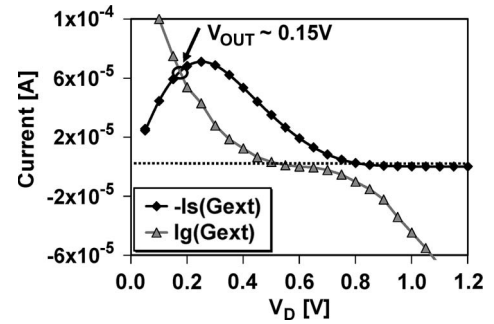

Fig. 9. I_G and I_S versus V_D ($V_{\rm OUT}$) for the $G_{\rm EXT}$ model, where V_D is swept from 0 V to 1.2 V while V_G is swept from 1.2 V to 0 V. Because this model does not detect changes in I_S, $V_{\rm OUT}$ only rises up to 0.15 V, which makes the inverter output appear stable, in contradiction to the SBD data in Fig. 8.

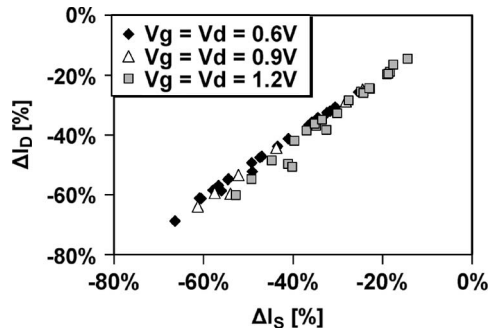

Fig. 10. ΔI_D versus ΔI_S for $V_{\rm GD} = 0$. Despite there being no potential difference between the gate and the drain, significant degradation in both I_S and I_D is observed, with $\Delta I_D = \Delta I_S$.

between the gate and the drain, significant degradation (up to 70%) in both I_S and I_D is observed, with $\Delta I_D = \Delta I_S$. This shows that for both SBD and HBD, the source and the drain are always strongly coupled when $V_G = V_D$. However, while the drain and source are always strongly coupled for SBD in inversion, the source *is* coupled to the gate for HBD, *except* when $V_G \sim V_D$ and at high V_D when $V_G > V_D$, as shown in Fig. 11. Accordingly, the coupling between the device terminals is complex and cannot be explained by the existing models.

I_G versus V_G for SBD and HBD is shown in Fig. 12. HBD is ohmic, as expected. For SBD, gate-to-drain breakdown follows a power law with an exponent from 1.7 to 2. This is significantly

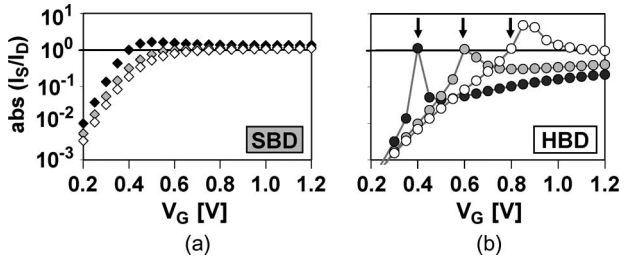

Fig. 11. I_S/I_D for (a) SBD (23 KΩ), and (b) HBD (2 KΩ). Fresh device: Horizontal line. Dark fill: $V_D = 0.4$ V. Gray fill: $V_D = 0.6$ V. Open fill: $V_D = 0.8$ V. For the fresh and SBD devices, the source is strongly coupled to the drain. For HBD, the source is coupled to the gate except when $V_G = V_D$ (vertical arrows) and at high V_D when $V_G > V_D$.

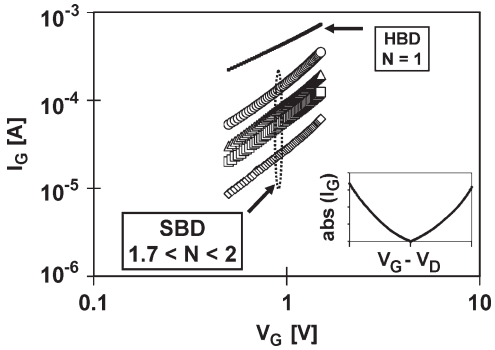

Fig. 12. I_G versus V_G at $V_D = 0$ V after SBD and HBD. Diamonds: 36 KΩ SBD. Squares: 16 KΩ SBD. Triangles: 11 KΩ SBD. Circles: 6 KΩ SBD. Dark line: 2 KΩ HBD. Inset (linear scale) shows that SBD (12 KΩ) I_G is polarity symmetric in $V_{\rm GD}$.

lower than for gate-to-body SBD [16]. The inset in Fig. 12 shows that SBD I_G is polarity symmetric in V_{GD}.

IV. Equivalent Circuit Model

The key features of gate-to-drain breakdown are as follows: 1) SBD I_G follows a power law in V_G with an exponent from 1.7 to 2.0 so that $1 < \mathrm{N} < 2$ encompasses gate-to-drain SBD and HBD. 2) I_G is polarity symmetric in V_{GD}. 3) All the terminal currents are degraded after breakdown across a wide range of voltage, including when $V_G = V_D$. 4) The source does not significantly contribute to I_G after SBD and is strongly coupled to the drain. 5) The source is coupled to the gate after HBD, except when $V_D \sim V_G$ and at high V_D when $V_G > V_D$.

The equivalent circuit for SBD only is shown in Fig. 13, and the equivalent circuit for SBD + HBD is shown in Fig. 14. Both configurations comprehend I_G, I_D, and I_S. There are two parallel depletion-mode NFETs (T1, T2) *operating in saturation* between the gate and the drain, each with a series resistor (R1, R2). This portion of the circuit provides a gate current that is polarity symmetric in V_{GD} and emulates a power law exponent from 1 to 2. The exponent of 2 is the long-channel saturation current limit, i.e., $I_{\rm DSAT} \sim k(V_G - V_T)^2$, and the exponent of 1 is the short-channel velocity saturated limit, i.e., $I_{\rm DSAT} \sim k(V_G - V_T)$ [17]. Thus, the gate-current power law exponent can be varied between 1 and 2 by tuning the channel lengths of T1 and T2 or by adjusting the saturation velocities of T1 and T2 to modulate the channel length dependence of

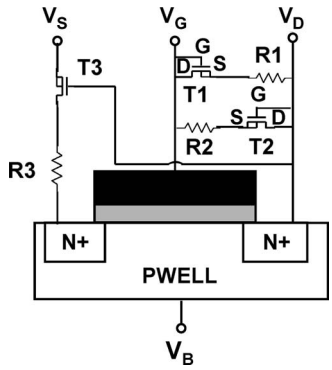

Fig. 13. Equivalent circuit (six elements) for gate-to-drain SBD. T1 and T2 are depletion-mode NFETs operated in saturation to emulate an I_G power law that is polarity symmetric in $V_{\rm GD}$. T3 is operated in the linear mode and couples the source to the drain. Note that there is no component from the gate to the source.

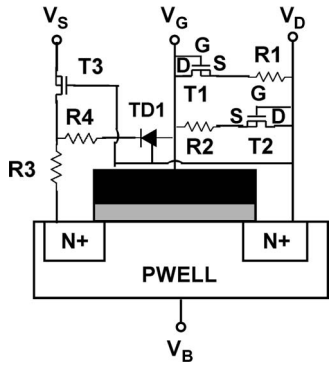

Fig. 14. Equivalent circuit (eight elements) for gate-to-drain breakdown, comprehending both SBD and HBD. Inclusion of TD1, which is a drain-controlled gate–channel-oxide tunneling diode, couples source and gate.

$I_{\rm DSAT}$ [19], [20]. Transistor T3 is operated in the linear mode to provide a voltage-controlled resistance that, together with its series resistor R3, models the drain-to-source coupling. Note that there is no component connecting the gate to the source. For the HBD model shown in Fig. 14, a drain-controlled gate–channel-oxide tunneling diode (TD1) and a series resistor (R4) are added to couple the source to the gate, as the source current after HBD is exponential. The results of SPICE simulations using these equivalent circuits are compared to the SBD and HBD data in Figs. 15 and 16, respectively. Except for the HBD I_S in the subthreshold regime when both V_D and V_G are low, which is a condition that does not typically occur in circuit operation, excellent fits for I_G, I_D, and I_S are obtained across a large voltage range. It should be noted that when properly optimized, the equivalent circuits do not introduce significant parasitic capacitances. The device parameters extracted from SPICE model fits are shown in Table I.

V. Discussion

In this paper, we have shown that gate-to-drain breakdown in state-of-the-art technologies results in severe degradation of all the terminal currents for both SBD and HBD. The equivalent circuit configurations in the literature do not adequately model our device behavior. The explanation for the

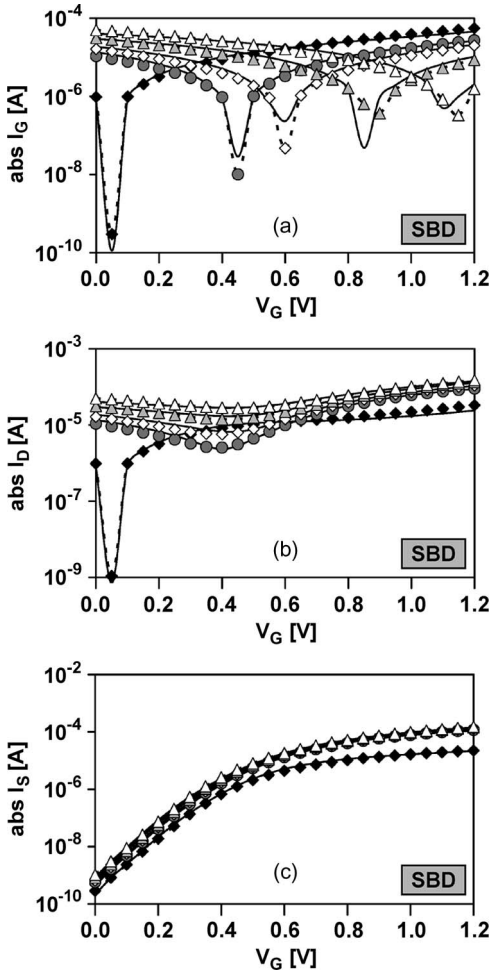

Fig. 15. Comparison of SBD data ($R_{\mathrm{EFF}} = 23$ KΩ) with SPICE simulations. (a) I_G; (b) I_D; (c) I_S. Solid lines: Model fits; symbols with dashed lines: Data. Dark Diamonds: $V_D = 0.05$ V; gray circles: $V_D = 0.45$ V; open diamonds: $V_D = 0.6$ V; gray triangles: $V_D = 0.9$ V; open triangles: $V_D = 1.2$ V.

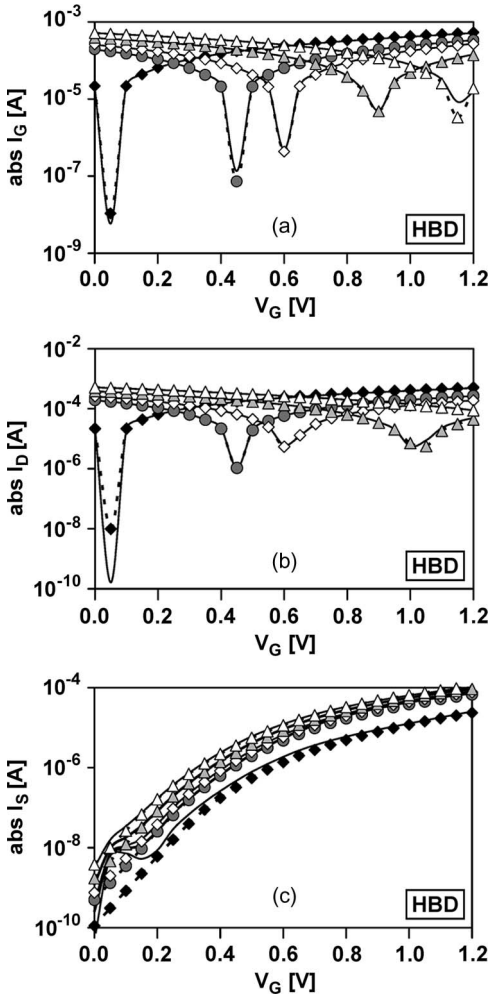

Fig. 16. Comparison of HBD data ($R_{\mathrm{EFF}} = 3$ KΩ) with SPICE simulations. (a) I_G; (b) I_D; (c) I_S. Solid lines: Model fits; symbols with dashed lines: Data. Dark Diamonds: $V_D = 0.05$ V; gray circles: $V_D = 0.45$ V; open diamonds: $V_D = 0.6$ V; gray triangles: $V_D = 0.9$ V; open triangles: $V_D = 1.2$ V.

discrepancies may lie in the differences in technologies used for the various investigations. It has been reported that the materials incorporated in the gate stack and the source/drain regions are introduced into the channel following gate-to-drain breakdown [18]. This could explain the strong source–drain coupling observed, particularly in short-channel devices. The resulting structural changes induced by breakdown might alter the channel potential and/or the channel mobility (a detailed analysis of the impact of breakdown on short-channel effects will be separately published). Another factor could be the range of the conductivity of the breakdowns. In this paper, all post breakdown R_{EFF} (1.0 V) are less than 80 KΩ.

While post breakdown degradation is severe at the waveform "edges," i.e., $|V_{GD}| \gg 0$, changes in terminal currents at intermediary voltages also play a significant role in post breakdown functionality. Not only are these conditions important during switching but even when the waveform is at an "edge," post breakdown degradation can result in node voltages rising into this intermediary regime, as shown in Fig. 8. Therefore, circuit reliability simulations must accurately model post breakdown degradation throughout the entire voltage waveform.

TABLE I
SPICE MODEL PARAMETERS FOR SBD ($R_{\mathrm{EFF}} = 23$ KΩ) AND HBD ($R_{\mathrm{EFF}} = 2$ KΩ) CORRESPONDING TO FIGS. 15 AND 16, RESPECTIVELY

R_{EFF}	R1	R2	R3	R4	T1	T2	T3	TD1
					V_{TH}	V_{TH}	V_{TH}	V_{TH}
[KΩ]	[KΩ]	[KΩ]	[KΩ]	[KΩ]	[V]	[V]	[V]	[V]
23	42	42	0.5	---	-0.1	-0.1	-14.2	---
2	4	4	0.2	2.5	-10.0	-10.0	-9.6	+0.5

VI. CONCLUSION

The degradation of NFET characteristics following a gate-to-drain breakdown is underestimated in equivalent circuits where components solely between the gate and the drain are employed. This arises because the coupling between device terminals after a breakdown is more complicated than is modeled by these configurations. Failure to account for the degradation in all terminal currents resulting from these interactions can result in erroneously optimistic reliability simulations. Properly optimized, the equivalent circuits presented in this paper provide excellent fits of SPICE simulations to post gate-to-drain breakdown data.

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