Effect of coupling capacitor in onchip interconnects of driver – receiver circuits

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Abstract *The demand from the consumers and the market are continuously increasing for portable and fast responding devices, then the pressure on VLSI designers community persistent continuously. Though the Moore's law predicts doubling of transistor density for every eighteen months the challenge every day on VLSI industry is continuous. Earlier the onchip interconnects were not considered for the vital metrics like power and delay, but it cannot be neglected further. Any interconnect does have the effect of Resistance (R), Inductance (L)and Capacitance (C). In most of the cases RC effect will be considered only in specific cases the effect of Inductance considered. In this work the effect of capacitance considered for both single interconnect and bus architecture and two designs say scheme A and scheme B are proposed. The scheme A based on only analog, and scheme B designed to respond both digital and analog that is for mixed signals. Scheme A is chosen since it is performing better in terms of power consumption and power delay product.*

Keywords: *Onchip interconnects, driver-receiver, coupling capacitor, delay, device performance.*

I. INTRODUCTION

Incorporation of transistors on a single chip with lot of constraints like millions of transistors in smaller space with lesser power consumption poses lot of difficulties. The two major performance metrics power consumption and delay are considered in this paper. In the case of power consumption and delay, the on-chip interconnects play a major part. The overall device performance mainly depends on chip interconnects also.
In this paper, after a detailed comprehensive study of different driver- receiver signaling schemes [1], optimized low swing signaling scheme based on MJ driver scheme [2] that is current mode logic circuit for driving long interconnects in on-chip global interconnects is considered. The MJ driver as a benchmark driver is better performance low swing CMOS driver circuit, driving of global interconnects with large capacitive load. The MJ driver performs 16% faster, reduces power consumption 3% and energy delay product by 19% compared to any other driver that is discussed with a comparative table in the next section. The MJ driver has 47% lower active area, since it requires only one set of signals for optimum performance at 1 and 0.8 V. The proposed driver remains unchanged during operation compared to 30% output swing in the case of other drivers.
Two schemes of A and B driver- receiver pair architectures have chosen in this work. A better architecture of driver receiver pair connected at the two ends of an interconnect line thoroughly discussed and simulated. This driver – receiver architecture designed has demonstrated that showing better in performance compared to other schemes inters of power consumption, delay and power delay product. The main intention of this research is the load. The effect of capacitance as load in onchip interconnect. In VLSI applications either it is an interconnect or bus architecture simulation results verify that with no capacitive load and with different capacitive loads.

The demand for handheld gadgets and portable devices, fast response, technically in digital electronics terms less delay globally increasing day by day. Also, in these devices the minimum power consumption is a concern. Under such conditions, the research on low power devices in integrated circuits is increasing to a greater extent. Therefore, technology scaling as well as the device design managing the static power dissipation is a concern. To drive the signals on the global bus onchip interconnects, we need an improvised low swing driver-receiver circuit, that is presented in this work. Focus mainly on capacitively driven interconnects that are used for the transmission of signals and in the case of buses a series coupling capacitor is introduced at an optimized location. A substantial improvement of 56% in the delay performance is obtained with the driver-receiver and capacitively driven interconnect topology combine for the data transmission bus.

II. LITERATURE REVIEW

There are many low swing schemes developed considering the

main metrics like less delay, low power, and good SNR. In this work mainly delay and low power given priority accordingly studied different works available and compared. Total nine different low swing driver – receiver circuit models discussed and compared with six parameters like Low Power Low Delay and Good SNR are required to be necessary and Area Penalty, Multiple V_{dd} and Leakage Current not desirable. First, A: Multiple Voltage Technique [3] the required parametres are attained but there is area penalty, leakage current, this design required multiple V_{dd} which is not desirable also this is receiver dependancy design. B: Static Source Driver [4], in this work though there is no area penalty and desirable metrics are achieved but Low threshold voltage V_{th} is required. This design is receiver dependent model. C: NMOS only Push Pull Driver [5], this work except the receiver dependancy and multiple V_{dd} else this is a better choice. D: Charge Sharing Bus [6], in this model area penalty and leakage current is main concern, hence not ideal choice. The Differential Voltage Mode Siganling architecture [7] though this design good in respect of power, delay and SNR but this takes extra V_{dd}. Similarly, the Single Current Mode Signaling [8] have the disadvantage of extra V_{dd} as well as leakge current. Differential Current Mode Signaling scheme and Driver Pre Emphasis Technique scheme [9] too having concerns like area penalty and high power respectively. The one design meets the requirement of low power, less delay and good SNR is MJ Driver architecture [2]. The comparative table is shown in the table. 1.

Table.1 Matrics Comparision

Metrics	A	B	C	D	E	F	G	H	I
Low Power	×	×	×	×	×	×	×		×
Low Delay	×	×	×	×	×	×	×	×	×
Area Penalty	×			×	×	×	×	×	
Multiple V_{dd}	×	×	×		×				
Good SNR	×	×	×		×	×	×	×	×
Leakage Current	×			×		×			

III. METHODOLOGY

The basic interconnect signaling scheme [10] for on chip architecture of the driver- receiver pair shown in the Fig.1 with capacitive load that can be altered accordingly, and the interconnect model is shown in the Fig.2 this gives interconnect length with parasitic capacitance from interconnect to ground. This is a resistance – capacitance model in π/3 in distributed one, with interconnect length in mm. This architecture simulated having a receiver out with a capacitance of 5 Pf. This architecture tested with the test conditions shown in the table.2[11].

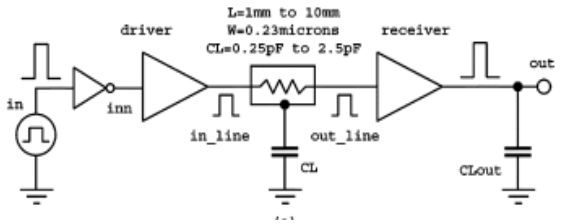

Fig. 1 On Chip interconnect signaling scheme with capacitive load.

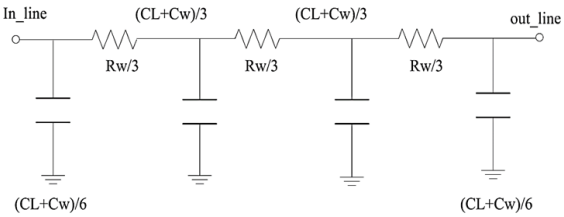

Fig. 2 Onchip Interconnect Model

Table .2 Test Conditions

Parameter	Value
Power Supply Vddh - Volts	1.0
Gate Source Voltage V_{gs} – Volts	0.54
Loading Condition C_L - pF/mm $C_{L\,Out}$ - pF	250 5

The designed architecture is shown in the Fig.3, this works on the basis of limiting the voltage swing along the total interconnect that improves the performance toa greater extent. The voltage swing is limited as per the equation 1.

$$\sim V_{tn} \leq V_s \leq \left(V_{dd} - |\sim V_{tp}|\right) \qquad (1)$$

The energy saving ratio is given by equation 2.

$$\frac{E_{low}}{E_{tot}} = \frac{V_s}{V_{dd}} \cong \frac{V_{dd} - |\sim V_{tp}| - V_{tn}}{V_{dd}} \qquad (2)$$

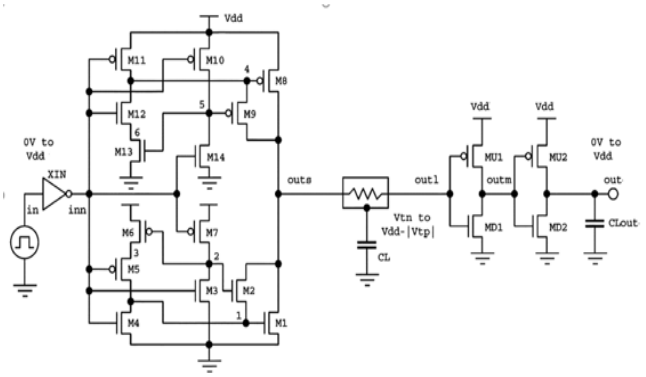

Fig. 3 Driver-Receiver Configuration Scheme – A.

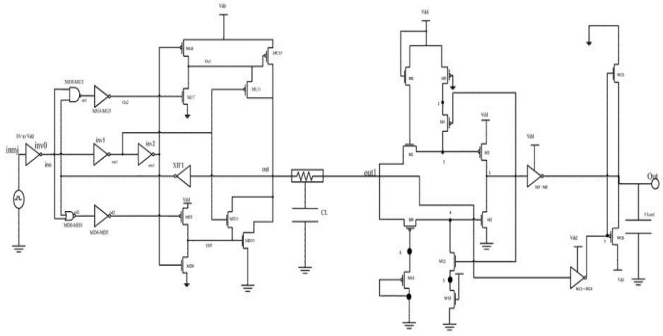

Fig. 4 Driver-Receiver Configuration Scheme – B.

In this work, two schematics A and B Fig. 4 [10] have taken, the performance of the both the schematics have compared- the two matrices power dissipation and power delay product shown in the table-3. The comparative table clearly says that the scheme – A is better choice and chosen for this work.

Table – 3 Comparison of Scheme A and B performance

Interconnect Length (mm)	Power Dissipation (µw)		Power Delay Product (pJ)	
	Scheme A	Scheme B	Scheme A	Scheme B
1	1	48.1	2.5	20
2	1.25	48.2	4	25
4	1.75	48.4	7.5	30
6	2	48.8	10	50
8	2.5	48.4	15	70
10	2.75	49	20	140

The driver- receiver architecture proposed as shown in the above Fig.3 [11] operates in active mode, diode connected and source follower mode. The full drive capacity is given by driver under active mode to make the interconnect line charge and discharge. This driver offers low impedance, and the low swing is controlled by diode connected mode. Noise immunity is provided by the third mode source follower mode. The transistor turn-off finally, as the interconnect is driven to other direction. Controlling the transistor sizing, the propagation delay can be improved with switching limits taken to overdrive capability. This scheme has one series only, that gives good drive strength with same area. Voltage level guard also be implemented when the line is not active in longer periods. When the working of circuit is concern, during the HIGH condition, M_3-M_4-M_6 transistors are ON, as well M_1- N driver – M_2-M_5-M_7 in OFF state. As the input goes from HIGH to LOW M_4-M_3-M_8 transistor, P- drive turned OFF. The gate of M_1 through transistor M_5-M_6 fully charged activating output transistor – Mode 1. When the interconnect line discharges through ground transistor M_7 active, males the M_6 OFF and switch ON M_2. As M_2 is active, M_1 gate is driven to the line as to match in mode2. Similar events occur in the upper half – M_8 side of the circuit.

The receiver side a simpler inverter, enable signal is added to it. In every transition as the driver line crosses $V_{dd}/2$, to maintain fast response, a simple balanced inverter to be selected. In this enable signal helps to turn off the receiver avoiding bus interconnect during the line is not used.

IV. RESULTS

Table. 4 reflects the effect of capacitance on the delay component. As there is no capacitance coupled to the output the delay simply increases. When there is a coupling capacitance of first trial 5pF though the interconnect length increases from 1 mm to 10 mm the variation is 12 ns to 17.8 ns. Even the coupling capacitance changed to 10pF it is observed that the change is not significant. When there is no coupling capacitance the delay ranges from 13 ns to 46 ns, that is more compared to 19 ns approximately double. Finally, no significant delay change. From table.5 it shows that keeping the length of the interconnect 1 mm same, as the coupling capacitance changes from 1 pF to 10pF the delay is same. Even in the table. 4 that shows that the delay increases with the increase in the length of interconnect and peaks at 7mm and later starts decreasing. The argument strengthens that the claim that a capacitively driven interconnect always more effective for higher interconnect lengths in the global interconnects.

Finally, from the above discussion it is clear that compared to without coupling capacitor, when there is capacitively driven interconnects provides a better performance in the case of delay than the normal interconnects. At the same version, the advantages of capacitively driven v/s normal interconnect are not effective in case of shorter interconnects, as the interconnect length increases, the performance improves many folds therefore the claim of improved performance for global wires with capacitively driven interconnects is established. Fig 5 and 6 shows the simulation output.

Table – 4 Comparison of transmission delay with 5pF, 10 pF and No capacitor values.

Interconnect Length (mm)	Delay (ns)		
	Coupling Capacitor (5 pF)	Coupling Capacitor (10 pF)	No Coupling Capacitor
1	12	12	13
2	15	15	17
4	18.5	19	25
6	20	20.5	31
7	20	21	35
8	19.5	20.5	38
10	17.8	19.2	46

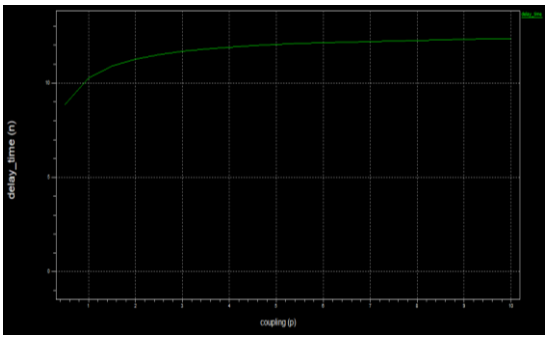

Fig. 5 Transmission Delay for varying coupling capacitor values with 1mm Interconnect length

Table.5 Transmission Delay for varying coupling capacitor values with 1mm Interconnect length

Coupling Capacitor (pF)	1	2	4	6	8	10
Delay (ns)	10.2	11.2	12	12	12	12

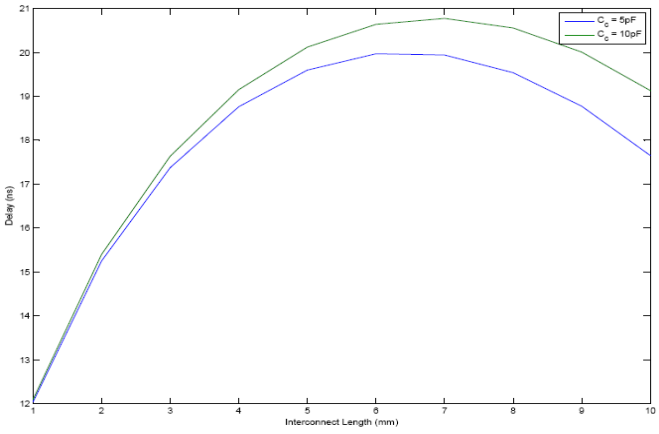

Fig. 6 Simulation output of coupling capacitor of 5pF and 10 pF with Interconnect length with 0 to 10 mm

V. CONCLUSION

From the above results and simulation, we can summarize that the capacitively driven interconnect has good compared to an interconnect without a capacitor. When the interconnect length is less than this is not having a prominent affect but for longer interconnects this shows better results. This work has attempted to better the interconnect performances like the delay and power consumption of driver receiver circuits.

VI. REFERENCES

[1]. T. Sridhar and Dr. A. S R Murty, "Comprehensive study on the signaling schemes in on chip Interconnects," 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, 2018, pp. 2042-2051.

[2]. J. C. Garcia, J. A. Montiel-Nelson and S. Nooshabadi, "Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects," 2007 IEEE International Symposium on Circuits and Systems (ISCAS), 2007, pp. 881-884, doi: 10.1109/ISCAS.2007.37804

[3]. F.S. Q. Zhu P. Chong, "A Placement Technique for Multiple Voltage Design," - 2006 for On-Chip Interconnects," 2007 IEEE International Symposium on Circuits and Systems (ISCAS), 2007,

[4]. Y. Nakagome, K. Itoh, M. Isoda, K. Takeuchi, and M. Aoki, "Sub-1-V swing internal bus architecture for Future low-power ULSIs," Solid-State Circuits, IEEE Journal of, vol. 28, 1993, pp. 414-419.

[5]. H. Zhang, V. George, and J.M. Rabaey, "Low-swing on-chip signalling techniques: effectiveness and Robustness," IEEE Trans. Very Large Scale Integrated System, vol.8,2000, pp. 264-272.

[6]. M. Hiraki, H. Kojima, H. Misawa, T. Akazawa, and Y.Hatano, "Data dependent logic swings internal bus architecture for ultra-low power LSI's," IEEE Journal of Solid-State Circuits, vol. 30, 1995, pp. 397-402.

[7]. A. Narasimhan, M. Kasotiya, and R. Sridhar, "A low-swing differential signalling scheme for on-chip global interconnects," 18th International Conference on VLSI Design, 2005, pp. 634-639.

[8]. A. Katoch, H. Veendrick, and E. Seevinck, "High speed current mode signal circuit for on-chip interconnects," IEEE International Symposium on Circuits and Systems, ISCAS 2005, vol. 4, 2005, pp. 4138-4141.

[9]. M.M. Tabizi, N. Masoumi, and M. Deilami, "High speed current mode signalling for interconnects considering transmission line and crosstalk effects," 50th Midwest Symposium on Circuits and Systems, MWSCAS'07, 2007, pp. 17-20.

[10]. T. Sridhar and Dr. A.S R Murty, "Power Efficient Clock Distribution for Switched Capacitor DC-DC Converters "Indonesian Journal of Electrical Engineering and Computer Science" Vol. 10, No. 1, April 2018, pp. 27~36 ISSN: 2502-4752, DOI: 10.11591/ijeecs.v10.i1.pp27-36.

[11]. T. Sridhar and Dr. A. S. R Murty, "Low power driver receiver topology with delay optimization for on-chip bus interconnects". International Journal of Engineering & Technology,[S.l.], v. 7, n. 3.29, p. 180-184, Aug. 2018. ISSN 2227-524X.

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