AN FPGA BASED PASSIVE K-DELTA-1-SIGMA MODULATOR

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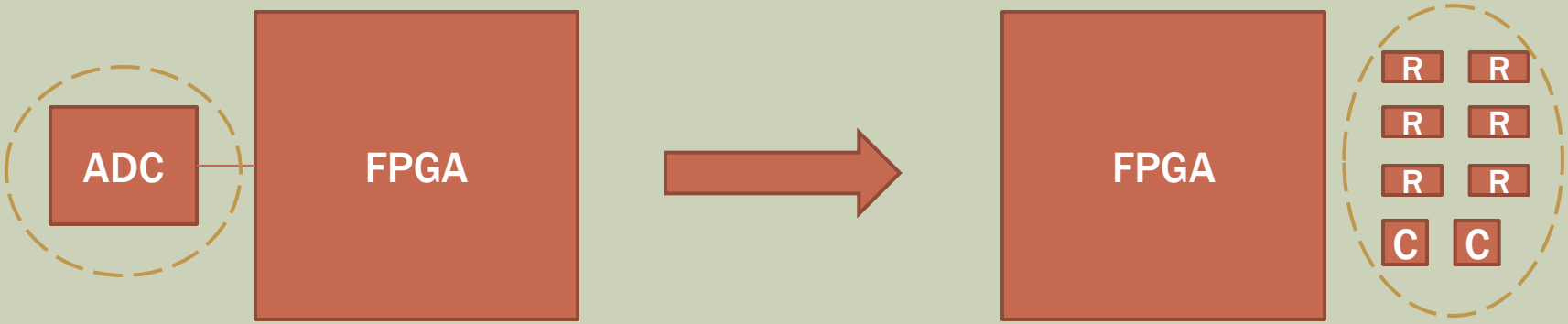
A BRIEF ROADMAP

- Need for FPGA Based ADCs
- Review of Basic ∑-Δ Principles/Adapting ∑-Δ ADCs for FPGAs
- Proposed KD1S ∑-Δ Modulator Topology
- Circuit Design
- Test Results

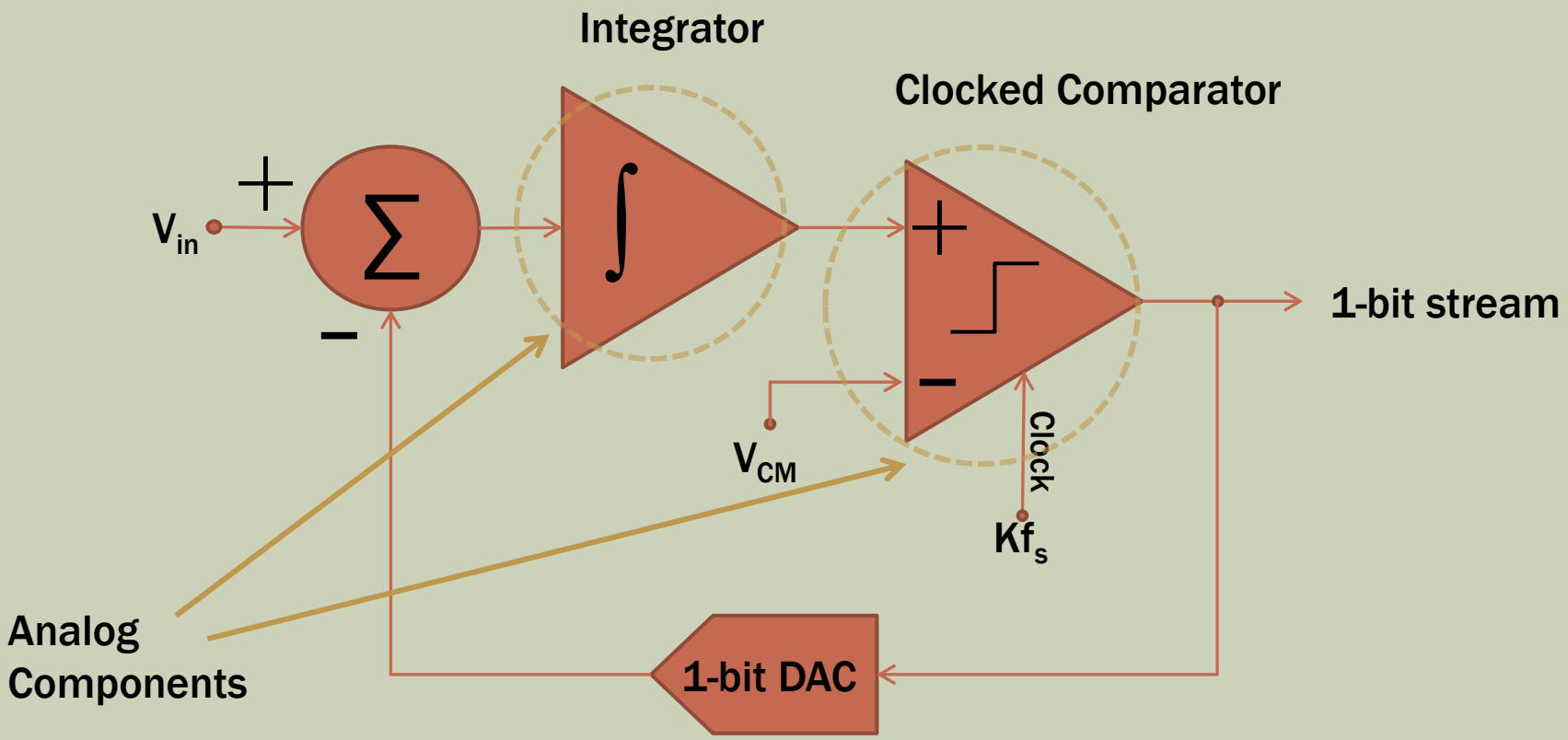
NEED FOR FPGA BASED ∑-Δ ADCS

FPGA based systems need to interface with the analog world.



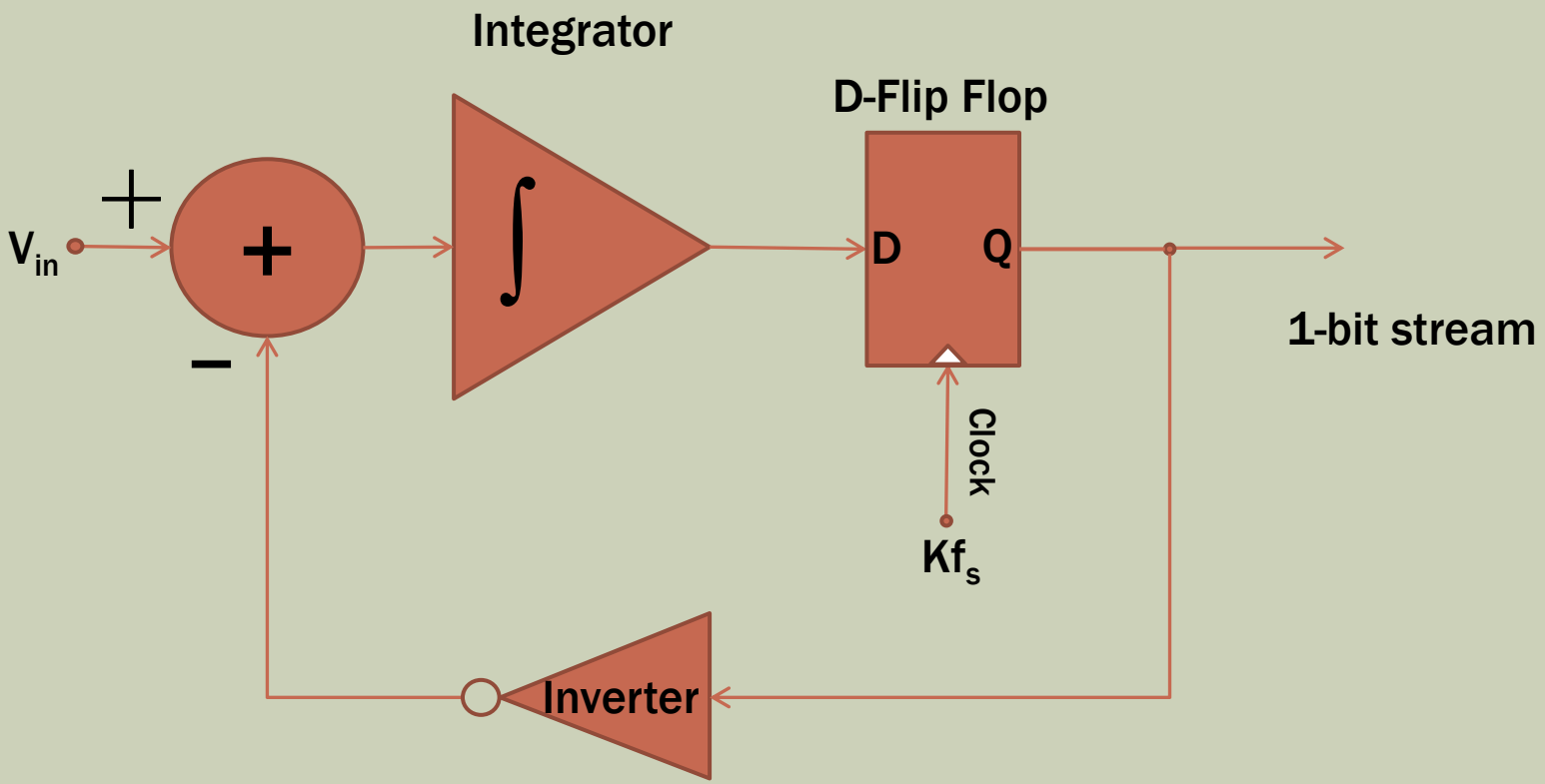
A costly ADC chip can be replaced with a handful of passive components.

REVIEW OF BASIC 1ST ORDER ∑-Δ MODULATORS



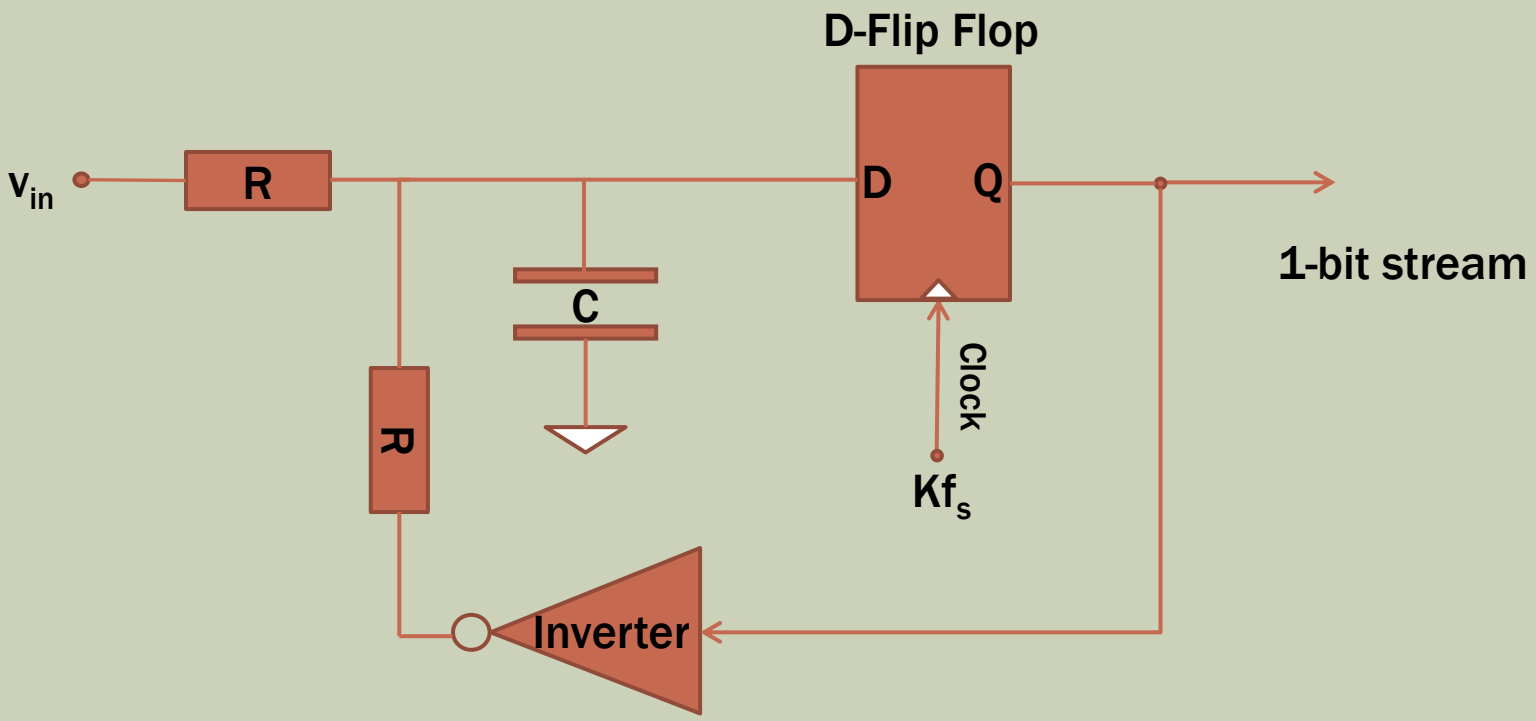
Generally, ∑-Δ modulators use clocked comparators as the quantizing element which are analog circuits.

ADAPTING ∑-Δ MODULATORS TO FPGAS



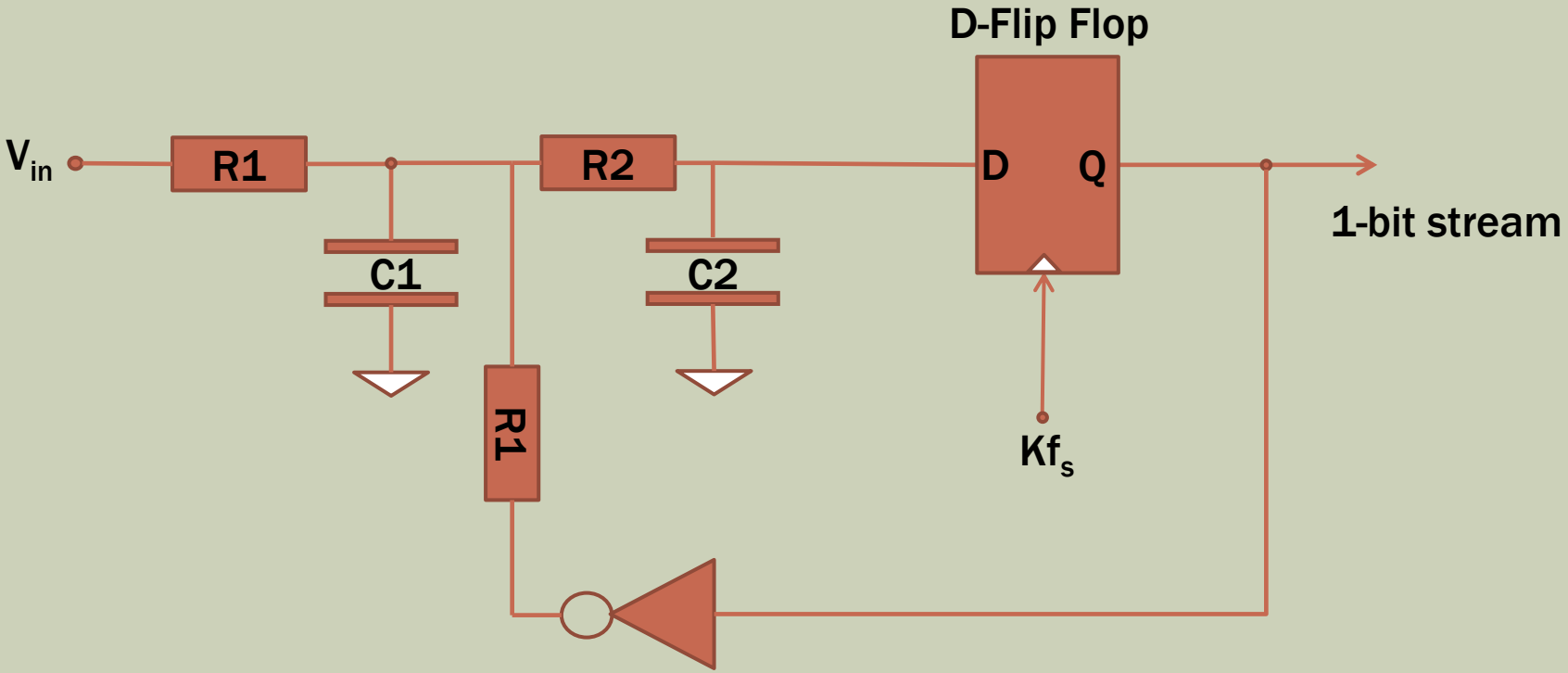
The clocked comparator can be replaced with a D-FF and the common mode voltage is replaced by the switching point of the D-FF.

ADDING PASSIVE COMPONENTS



The integrator and summing block are replaced by passive RC components.

IMPROVING THE DESIGN

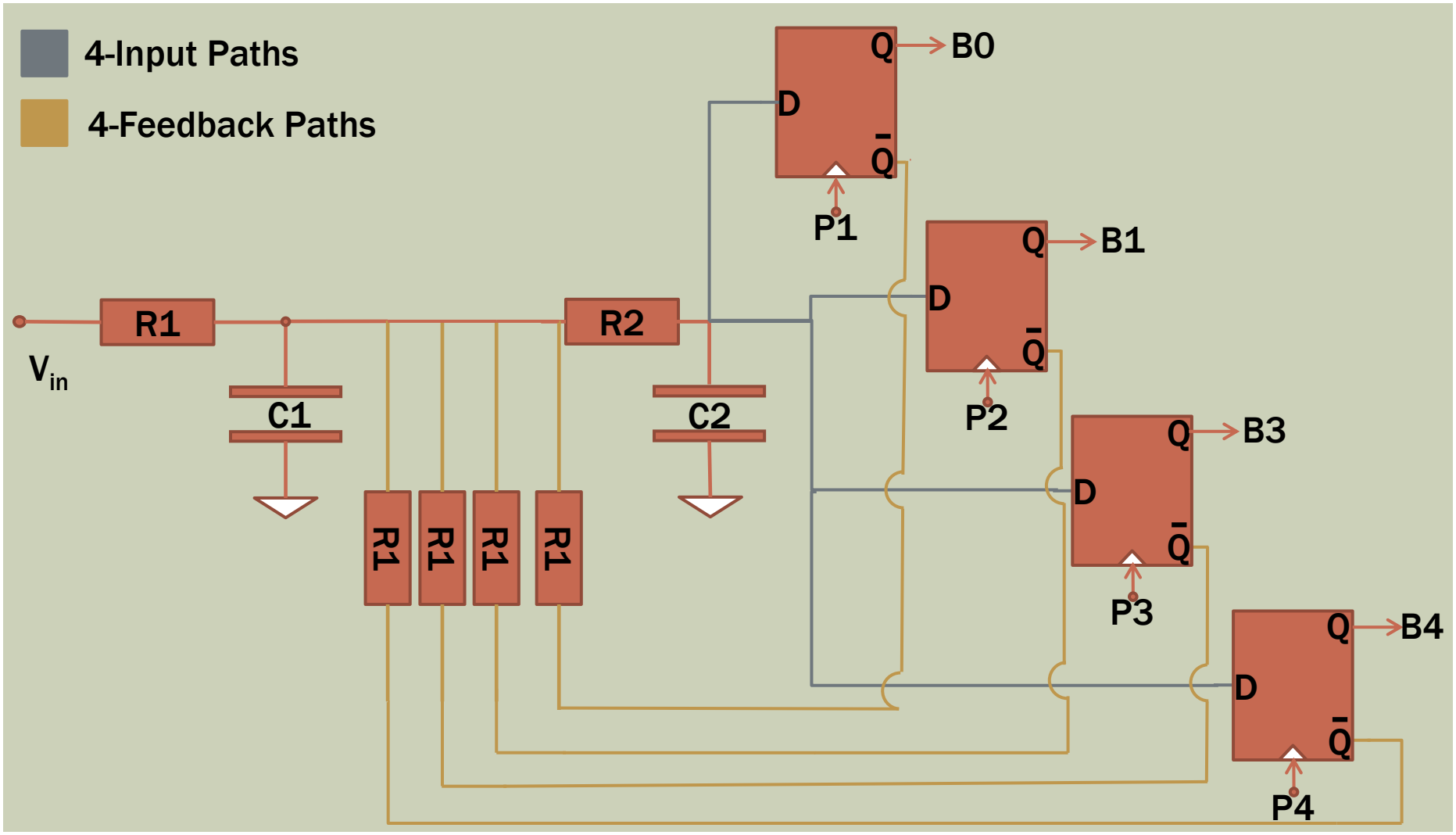


Previous work has shown that this particular passive 2nd order $\sum$-Δ topology has the best performance.

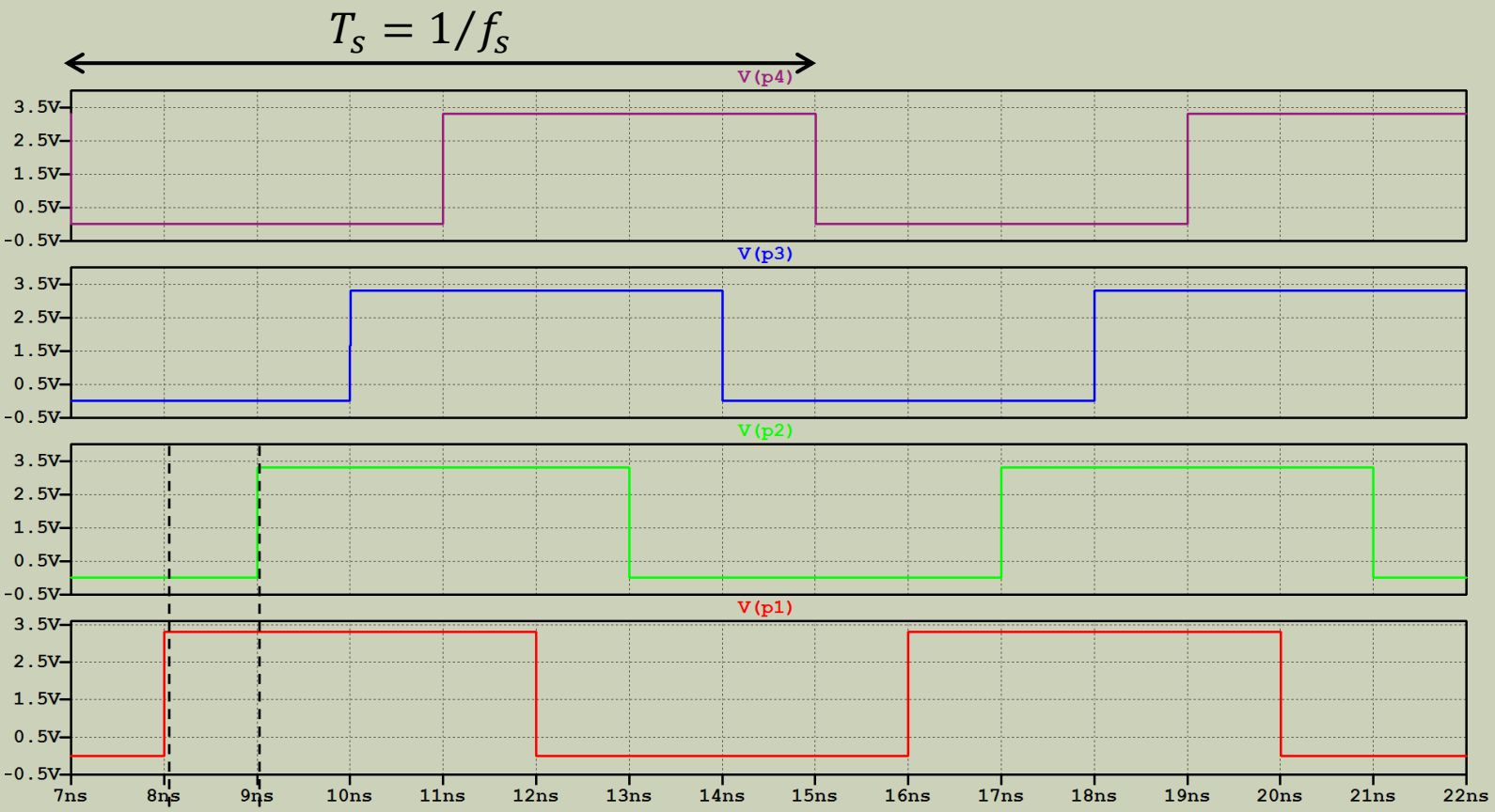
K-DELTA-1-SIGMA (KD1S)

- Requires K Quantizers
- There are K Feedback Paths
- Requires K Clock Signals
- Effective Sampling Rate is Increased K Times
- Only 1 Integrator (Sigma) Required

BASIC EXAMPLE



CLOCKS

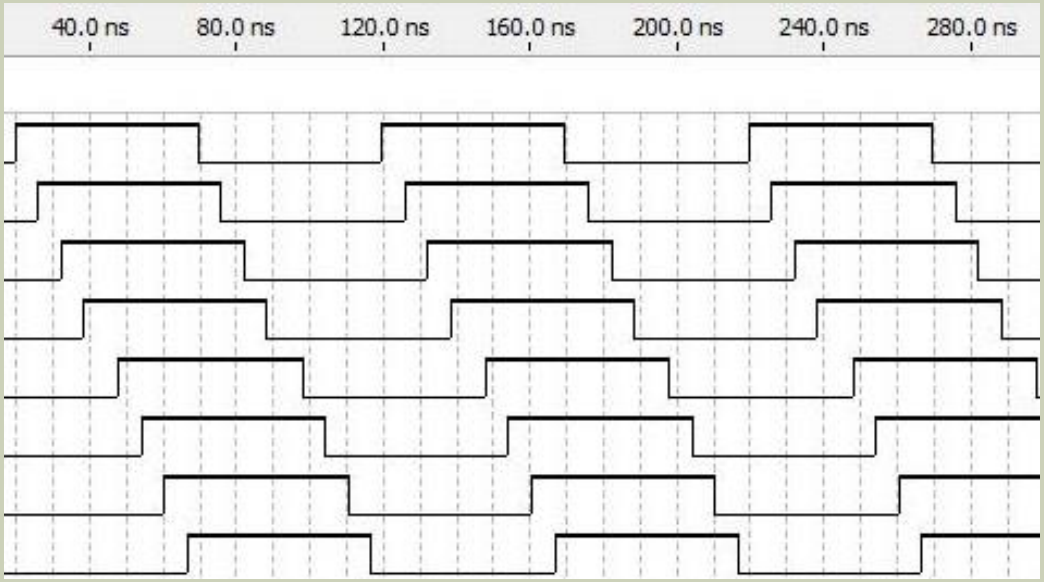


4 Equally Phase Shifted Clocks

$$\frac{T_s}{K_{path}} = \frac{T_s}{4}$$

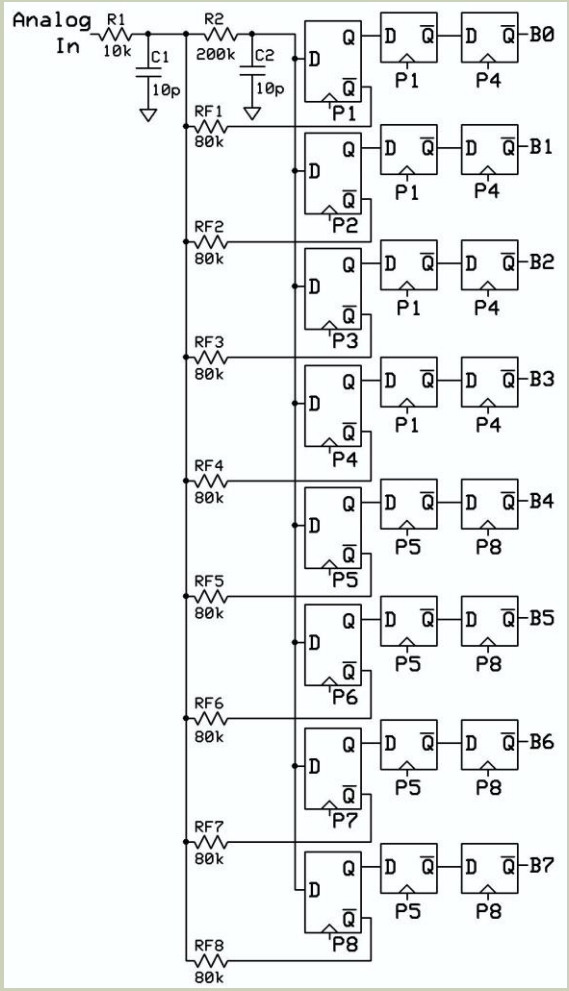
USING PLL RESOURCES ON AN FPGA

Two PLL blocks on an Altera Cyclone IV EP4CE115 FPGA was used to generate 8 phase shifted clocks for our 8 path KD1S Modulator



Simulation in Quartus

SCHEMATIC OF K1DS



Passive Components

- All passive RC components are located off-chip.

Quantizers

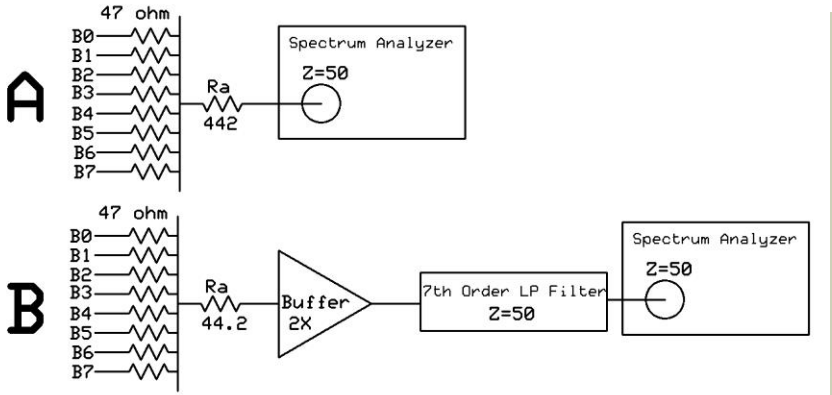
- First column of D-FFs are the 8 quantizing elements.
- P1-P8 are the phase shifted clocks.

Register

- Last two columns of D-FFs form a register to reclock the data.
- Output should be sent to digital filter block.

Only 8 logic elements and 2 PLL blocks used.

TESTING



Noise Shaping

- Test configuration “A” used to examine noise spectrum.

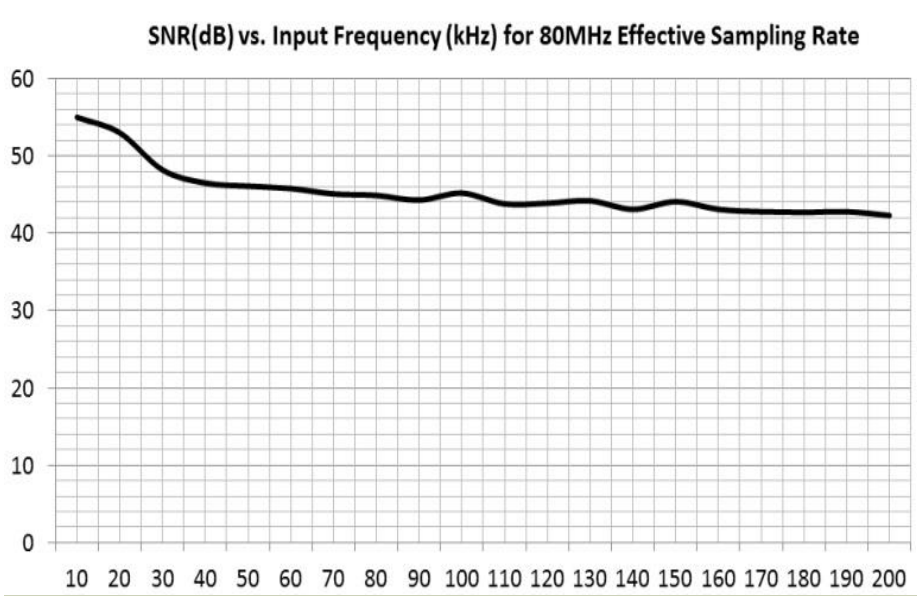
Signal to Noise Ratio

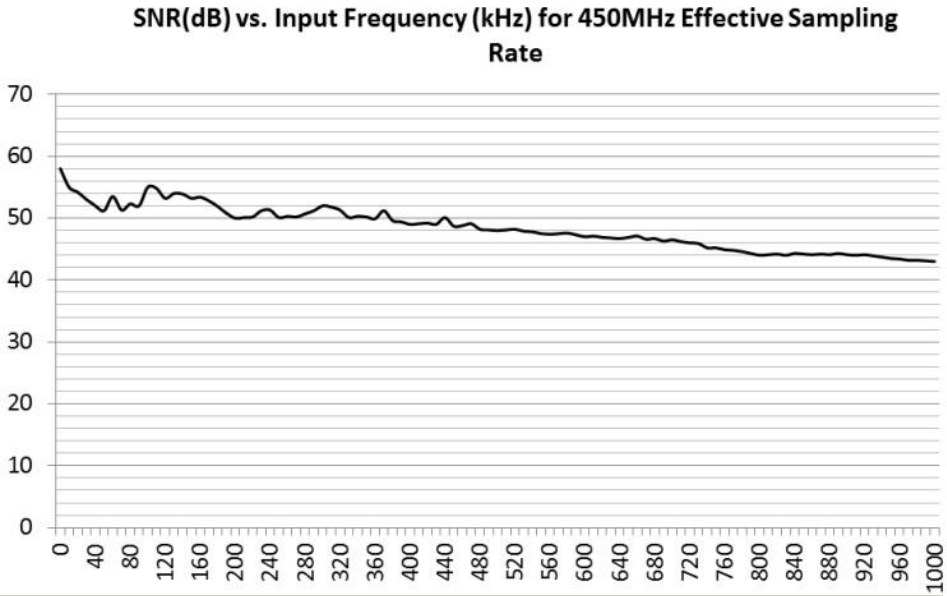
- Test Configuration “B” used to measure SNR.

Clocks

- Tests were done at clock frequencies of 10 MHz and 56.25 MHz.
- Effective sampling rates of 80 MHz and 450 MHz.

RESULTS





Peak SNR of 55 dB at 10 KHz corresponding to 8.8 effective number of bits (ENOB).

Peak SNR of 58 dB at 10 KHz corresponding to 9.3 effective number of bits (ENOB).

Oversampling ratio (OSR) nominally set to 512.

RESULTS SUMMARY

Parameter	Value
Base Clock Frequency	10 MHz / 56.25 MHz
Effective Sampling Rate	50 MHz / 450 MHz
Peak SNR	55 dB / 58 dB
ENOB	8.8 bits / 9.3 bits
Logic Element Use	8
PLL Use	2 (4 total on chip)
Percentage of Logic Elements Used	0.007% (8 out of 114,480)
I/O Pin Use	9

CONCLUSION

Expensive ADC chip can be replaced by a few passive components.

Sampling rates into the 10s of GHz should be possible with modern FPGAs.

Complex digital filtering can be performed on the FPGA.

Very low resource utilization.

Nominal 10-bit ADC can be implemented on FPGA.