**General Description**

The 100 Series GaN Controller is capable of operating and protecting all depletion-mode transistors. The non-inverting analog input accepts negative voltage to produce buffered negative gate bias. It allows 360° board placement with little or no line crossovers in the main board. A single power supply is enough for the 100 to provide dynamic control. Little or no filtering is needed in heavy RF environments. The 100 works seamlessly with 300 and 400 Series MOS switches that have compact footprints for locating near the transistor drain choke. It comes in evaluation boards that are ideal for fast prototyping.

**Features**

- Protects GaN devices from any power sequence of voltage supplies.
- Internal Negative voltage with 30mA OR external supply for 100mA boost.
- Bias Voltage has Fixed Gate OR Pulsed Gate configuration.
- Simultaneous Gate-Drain sequencing OR Independent Gate/Drain control.
- TTL OR Open Drain (<300mA) output drive for MOSFET switches.
- Temp compensation from local OR remote temp sensor feedback.
- >25dB EMI/RFI Rejection at all I/O ports except from auxiliary taps.
- <500 nsec total delay from V_Logic to V_Drain with applicable switch.
- RoHS* Compliant

**Specification Snapshot**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (+) Voltage</td>
<td>+20 V</td>
<td>+65 V</td>
</tr>
<tr>
<td>Supply (-) Voltage, Optional</td>
<td>-6 V</td>
<td>0 V</td>
</tr>
<tr>
<td>TTL Voltage Logic High</td>
<td>+3.6 V</td>
<td>+5.0 V</td>
</tr>
<tr>
<td>TTL Voltage Logic Low</td>
<td>0 V</td>
<td>+1.4 V</td>
</tr>
<tr>
<td>Internal (-) Supply V, Gate Pinchoff</td>
<td>-4.3 V</td>
<td>-0.5 V</td>
</tr>
<tr>
<td>Internal (-) Supply I</td>
<td>-30 mA</td>
<td></td>
</tr>
<tr>
<td>Gate Bias Voltage Range</td>
<td>-4.3V</td>
<td>-0.5 V</td>
</tr>
<tr>
<td>Out Switch Drive, Open Drain (V)</td>
<td>0 V</td>
<td>+60 V</td>
</tr>
<tr>
<td>Out Switch Drive, Open Drain (I)</td>
<td>300 mA</td>
<td></td>
</tr>
<tr>
<td>Output ON Prop Delay (T_Delay 1)</td>
<td>120 ns</td>
<td></td>
</tr>
<tr>
<td>Output ON Fail Time (T_Fail 1)</td>
<td>120 ns</td>
<td></td>
</tr>
<tr>
<td>Output OFF Prop Delay (T_Delay 5)</td>
<td>80 ns</td>
<td></td>
</tr>
<tr>
<td>Output OFF Rise Time (T_Rise 3)</td>
<td>80 ns</td>
<td></td>
</tr>
<tr>
<td>Gate ON Prop Delay (T_Delay 3)</td>
<td>160 ns</td>
<td></td>
</tr>
<tr>
<td>Gate ON Rise Time (T_Rise 2)</td>
<td>60 ns</td>
<td></td>
</tr>
<tr>
<td>Gate OFF Prop Delay (T_Delay 4)</td>
<td>160 ns</td>
<td></td>
</tr>
<tr>
<td>Gate OFF Fail Time (T_Fail 2)</td>
<td>60 ns</td>
<td></td>
</tr>
<tr>
<td>Soldering Temp (10 sec)</td>
<td>+260°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C</td>
<td>+85°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C</td>
<td>+150°C</td>
</tr>
</tbody>
</table>

**Typical Connection Diagram**

**Ordering Information**

Model  
100X_02R6  
100X_02R8  
100X_01R4  
100X_00R8  
120X_02R6  
120X_02R8  
120X_01R4  
120X_00R8  
124X_02R6  
124X_02R8  
124X_01R4  
124X_00R8

**UNIVERSAL GaN CONTROLLER:**  
NEGATIVE ANALOG INPUT, SINGLE DC SUPPLY, VGS SHUTDOWN AT -2.6V THRU -0.8V**, INDEPENDENT OR SEQUENTIAL SWITCHING OF DRAIN AND GATE

**DRAIN CONTROLLER:**  
100X WITH NO GATE SWITCHING CAPABILITY

**BASIC SEQUENCER:**  
100X WITH NO GATE SWITCHING, NO INTERNAL NEGATIVE AND LOGIC (+5V) SUPPLIES

* Select type X, L, or T
** All models have provisions for adjusting Vgs shutdown threshold to desired level.

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM
**Outline & Land Pattern**

**Controller I/O Pin Descriptions**

**WARNING**
- Do not connect Outputs together unless specified to do so.
- Do not ground unused Outputs. Leave open.
- Familiarize with the maximum rated voltages and currents.

**NTP** has ~4.3V output from a voltage inverter. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 100 Series only. Otherwise, leave open.

**V6N** input is connected to an optional negative supply of >–6V if gate current boost of 100mA is needed for saturated GaN. Internally, there’s 30mA. Leave open otherwise.

**POT** input receives negative voltage for 100 Series or positive voltage for 200 Series. This unity gain buffer provides negative bias to the transistor gate. Temperature-compensation voltage is added here as well.

**PGA** output produces a square-wave triggered by TTL to pin GTL. It provides gate bias to GaN at a level set from POT pin and down to V_pinchoff established from either the voltage inverter (~4.3V) or from pin V6N.

**FGA** output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

**PTP** has ~5.0V output from a voltage regulator. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 200 Series only. Otherwise, leave open.

**GTL** input takes active-low, TTL signal (~4.7V) to control gate switching of the device. It is tied to DTIL pin to sequence the gate and drain voltage. This is not used for sub-models. Disconnect from DTIL for independent control.

**DTIL** input controls the drain switching end of the transistor. When tied with GTL, the active-low TTL enables switches drain voltage ON and would remain there until gate voltage undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during ramping Vdd up & down.

**VP4** input is connected to an optional supply of ±5V. Leave open unless required by sub-models.

**DTIL** output is an active-low TTL drive signal reserved for 300 Series Power CMOS switches. Leave pin open otherwise.

**DFB** input monitors the presence of drain voltage when the MOS switch is ON. Use if gate switching is desired; otherwise, leave open for sub-models.

**DRV** output connects to the gate input of MOSFET switch module. Connect to multiple switches with up to 300mA total loads.

**VDS** input receives up to ±80V from the same supply that powers the GaN.

**REG** is an auxiliary port of +5.7V from a voltage regulator.

**SHD** is an auxiliary port for adjusting the gate voltage shutdown threshold. From this node, connect 100KΩ-1MΩ resistor to REG (or PTP) ports for increasing the threshold level, or to GND for decreasing said level.

**Typical Timing Diagrams**

Refer to Application Note XAN-2 for further details.