International Journal of Modern Science and Technology, 2021;6(5-6):95-100.
ISSN: 2456-0235.
www.ijmst.co

Research Article

A low power full adder design with digital to analog converter circuit by generic 250nm devices

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Abstract

In recent trends most of the digital circuits are combinations of full adders and multiplexer. In past many reported that adders, multiplexer are suffered from the problems of voltage swing and high noise when operated at low voltage. Authors have discussed 8-bit multiplexer design employing CMOS full adder using Double Pass Transistor and multi output carry look ahead logic. DPL adder avoids the noise edge problem and speed deprivation at low value of supply voltages associated with complementary pass transistor logic circuits. Consequently new design methodologies are being implemented in which CMOS logic full adder is one of the proposed circuit having low power consumption and high speed. For this we adopted AND and OR gates. The investigation is carried out with simulation runs on GENERIC250nm. These gates are regulated for obtaining sum output with DPL. In this paper we implemented multiplexer by using CMOS logic full adder.

Keywords: Full adder; Generic 250 nm; AND gate; OR gate.

Introduction

Multiplexer plays an important role in today's digital signal processing and various other applications. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplexer design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so, the need of high speed and low power multiplier has increased. Literature delineates outline and execution of fast multiplier [1,2]. The fastest types of multipliers are parallel multipliers. Among these, the Array multiplier is the basic one. However, they suffer from more propagation delay. This paper presents the methods required to implement a high speed and high performance parallel complex number multiplier. The designs are structured using Radix-4 Modified Booth Algorithm and Wallace tree [3,4].

Real time applications such as controlling environmental conditions demand quick response of the processor for processing the acquired signals. Multiplier is an important feature of signal processing. Atypical processor central processing unit devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology [5,6].

In the present work, authors proposed a novel 4x4 bit reversible multiplier circuit. Gates was used to construct the reversible multiplier circuit. The proposed reversible multiplier circuit can multiply two 4-bitsbinary numbers. Multiplier modules are common to many DSP applications. The fastest types of multipliers are parallel multipliers [7,8]. Among these, the Array multiplier is the basic one. However, they suffer from more propagation delay. This paper presents the methods required to implement a high speed and high performance parallel complex number multiplier. The designs are structured using Radix-4 Modified Booth Algorithm and Wallace tree [9-12].

Real time applications such as controlling environmental conditions demand quick response of the processor for processing

Received: 08.05.2021; Received after Revision: 18.05.2021; Accepted: 21.05.2021; Published: 28.06.2021.

the acquired signals. Multiplier is an important feature of signal processing. Atypical processor central processing unit devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction [13-22]. Reversible logic circuits are of interests to power minimization having application Effective multiplexer power-delay space design using generic 250 nm device low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In this paper we propose a novel 4x4 bit reversible multiplier circuit. The gates were used to construct the reversible multiplier circuit. The proposed reversible multiplier circuit can multiply two 4-bits binary numbers. It can be generalized for NxN bit multiplication.

Existing system

Multiplexers are a combinational logic component that has several inputs and only one output. MUX directs one of the inputs to its output line by using a control bit word (selection line) to its select lines shown Fig 1. Multiplexer contains the followings: o data inputs o selection inputs ‘o’ a single output ‘o’ Selection input determines the input that should be connected to the output. The multiplexer sometime is called data selector. The multiplexer acts like an electronic switch that selects one from different. A multiplexer may have an enable input to control the operation of the unit.

Multi output carry look ahead adder

In order to achieve high-speed in arithmetic operation, carry propagation time is the deciding factor as itlimits the speed of the whole logic circuit which increases with the size of the adder? For n-bit Parallel adder,Total propagation delay = S + (n −1) C Where S is propagation delay of sum and C is propagation delay in carry. In parallel adders (ripple carry adder), carry propagates in series or ripple which increases with size of adder.

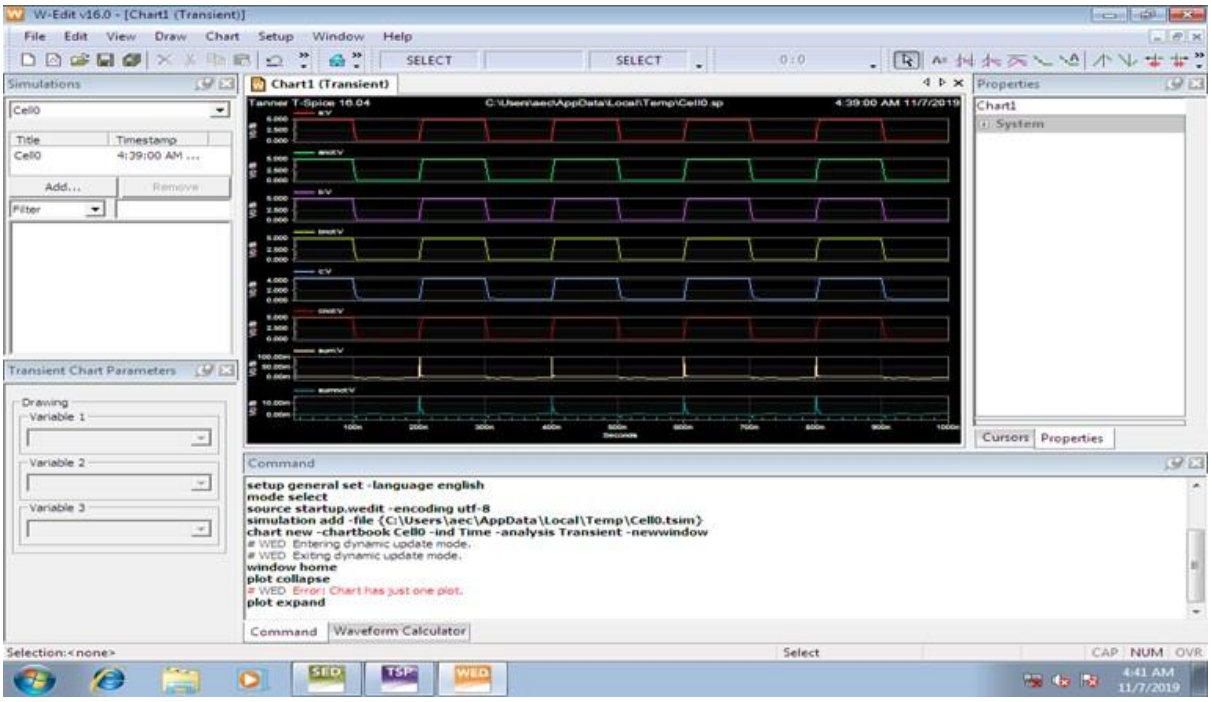

Fig. 1. One bit full adder output waveform

Carry propagation time can be reduced by two ways as demonstrated. One solution is to develop faster gate with reduced delays. Another solution is to reduce the carry propagation delay at the cost of increasing the complexity of design. For reducing the carry propagation time in a parallel adder, several techniques are used out of which Carry look ahead adder logic is most widely used shown Fig. 2. Recently shown that the 8-bit CLA adder was used Manchester Carry Chain (MCC) in multi output domino CMOS logic. Carries have

developed the multi output domino gates. CMOS full adder design is implemented using stack of PMOS and NMOS transistors. The basic architecture of full adder design consists of 28 transistors and three input variables (a, b and c) and two output variables (sum and carry) of 1-bit each.

Proposed system

CMOS full adder

To create new full adder with desired performance, different logic styles are used, in which CMOS logic style is one achieves greater efficiency. As an example DPL full adder CMOS logic style is used. In module one, circuit is designed using AND-OR gates to produce internal signals.

It is based on complementary pass transistors and DPL. The first half his circuit is inherently fast due to use of high mobility NMOS transistors and fast differential cross-coupled PMOS uses only NMOS pass transistors for generating the output. Transistor has a direct impact on its area. Moreover the series transistors in the output create a weak driver shown Fig. 1. Additional inverter at the last stage is required to provide the necessary driving power, which results in higher power consumption.

DPL full adder

A new design is introduced to structure of the full adder which is a combination of both pass transistors logic and static CMOS logic. The power dissipation is evaluated by estimating the power flowing into the circuit. For each value of supply voltage, we first performed the functional verification for each topology considering all possible input transitions shown Fig 2. Comparison analysis of an 8-bit adder design and 8-bit multiplier design. It is apparent that multi output Carry look ahead adder architecture has smaller delays, even though its speed advantage is greatly reduced for lower VDD. At high supply voltages DPL and CLA adders are always faster than the earlier version. At VDD =0.6V, propagation delay of multi output CLA is 29.21% less than ripple carry adder and 6.09% less than DPL adder but it consumes more power in comparison with the other two adder designs shown Fig. 3. It is clear that the power dissipation for multi output Carry look ahead adder architecture is always the highest. Hence, these new topologies should not be used when the primary target is low power consumption. Thus, multi output CLA adder is more suitable for time critical operations. At VDD = 0.5 V the 8-bit multiplexer designed using DPL adder has 22.39% less delay than the multiplier with CMOS full adder shown in the fig. 4 and those 15% improvement in delay as compared to multiplier designed using DPL adder.

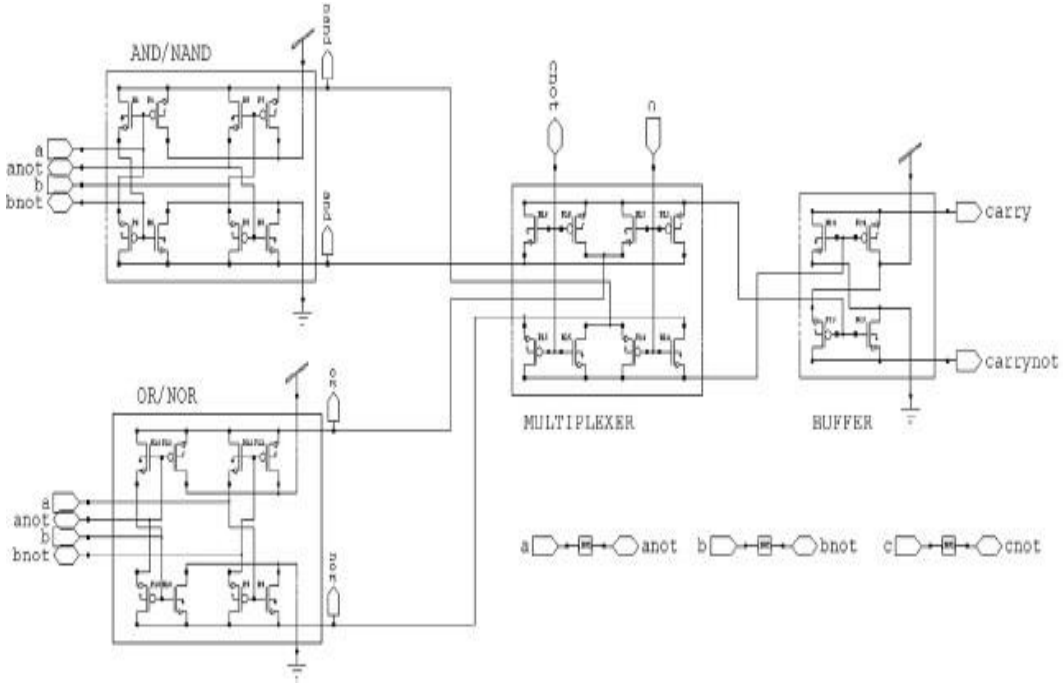

Fig. 2. AND and OR gates using one bit full adder

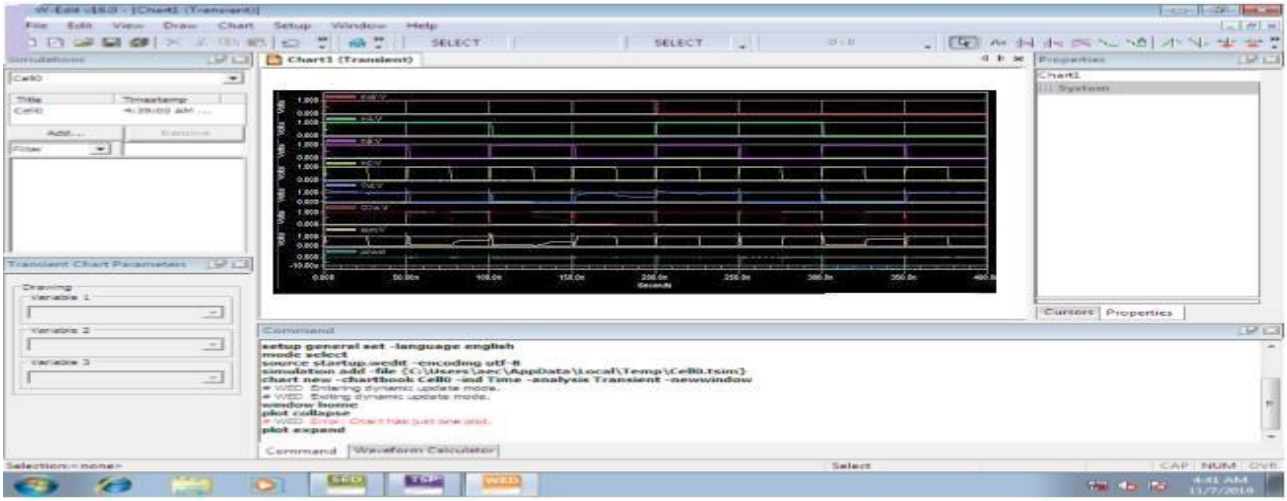

Fig. 3. AND and OR gate using one bit full adder output waveform

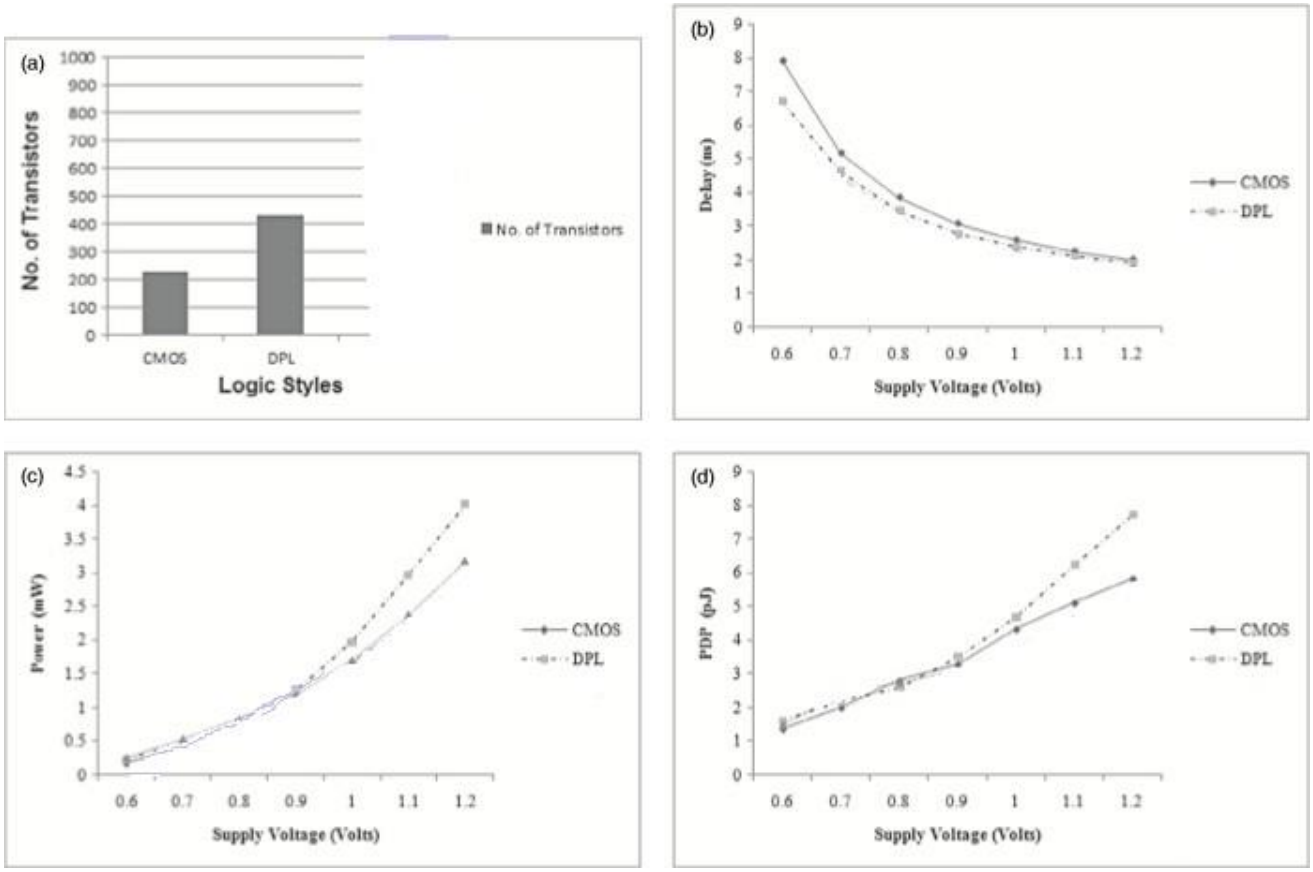

Fig. 4. Comparison analysis of multiplexer (a) Transistor count (b) Delay versus VDD (c) Power versus VDD

Conclusion

The present work has proposed basically compare the results of delay and power dissipation of CMOS FULL ADDER range and also how these are related with different design parameters. The present work has proposed speed efficient multiplexer architecture designed using double pass transistor logic adder. Further, authors carried out a comparison among the multipliers employing latest adder architectures. The comparison results are obtained in power-delay space. Thus, the design guidelines are derived to make the selection of appropriate multiplier design at the beginning of the design process. This work will help to proper characterize and analyze of the CMOS DPL full adder.

Conflict of interest

Authors declare no conflict of interest.

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