Implementation of Carrier Phase and Time Recovery Loop for Future Generation Communication Systems

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Abstract*—Signal propagation delay in digital modulation systems results into a frequency shift at receivers' end. This shift causes an ideal constellation to rotate and leads to the introduction of a phase error. To minimize such an error, each receiver consists of a carrier recovery block. Coherent detection, a prime feature of a quadrature amplitude modulation (QAM) receiver, offers increased spectral efficiency and superior sensitivity. This study aims to propose an algorithm for a carrier phase loop with a fixed-point precision. The algorithm tests a received signal phase with the QAM receiver to modify the output phase to a consistent fixed constellation. In addition, simultaneous timing recovery is performed, which can be used for a variety of applications. Moreover, the model is programmed in C/C++ and packaged as a system generated block and automatically assembled, replicated, and implemented with a coherent receiver system. The complete simulation of the proposed algorithm is designed and developed using Simulink software. The results of the model can be implemented in next-generation communication systems.

Keywords*—Carrier; Coherent; Constellation; Error; Receiver; Recovery

I. INTRODUCTION

Quadrature amplitude modulation (QAM) has witnessed an exponential growth in a variety of communication applications, namely satellite and optical systems. In QAM, symbol rate reduction can be attained by supplementing additional points in constellation—which lessens bandwidth requirements of a system and enhances spectral proficiency.

In digital communication systems, it is very important to match the phase of a signal that is sent from a transmitter to a receiver. If both phases do not match, then a clock cycle will not recover properly.

To attain such advantages, precise estimation of frequency and phase must be conducted in coherent (synchronous) receivers. However, in reality, an offset in phase of a signal caused by channel delay and offset in frequency caused by a transmitter and receiver carrier frequency cause rotation in constellation. Such a rotation causes error rate degradation leading to incorrect predictions [1, 2].

A robust performance carrier recovery is a fundamental part of a coherent QAM receiver that comprises extremely low steady-state phase latency and should be impulsively achieved in systems [3].

This study presents a carrier phase and time recovery system for QAM systems, which is modeled in MATLAB Simulink. The system is designed for a 16-QAM system, which can be translated up to a 256-QAM system.

The remainder of this paper is organized as follows. Section II focuses on the literature review that is used for implementing carrier phase and time recovery loop. Section III illustrates the proposed system. Section IV emphasizes on results and discussion. Lastly, Section VI, concludes the study.

II. LITERATURE REVIEW

Zhiwen *et al.* [1] introduced square counterchange method for coherent demodulation. They proposed a square phase locked loop for coherent detection of two differential phase-shift keying carrier signals.

Moreover, their proposed phase-locked loop possessed advantages such as improved noise resisting capabilities and resolving 180° phase shift issues during detection. By means of Simulink, an emulational circuit was simulated with perfect carrier extraction.

Siqiang [4] developed a system for a digital carrier recovery loop aimed at higher-order QAM signals using a coordinate rotation digital computer (CORDIC) algorithm and a phase frequency detector (PFD).

The initial carrier recovery loop used polarity decision (PD) algorithm under two modes (i.e., fast and slow) to capture frequency offset and subsequently switched to decision-directed (DD) algorithm to reduce phase jitters. In addition, the author proposed a new carrier recovery loop using the CORDIC algorithm for a digital direct frequency synthesizer (DDFS) encompassing high accuracy and flexibility to be implemented on a very large-scale integration platform over a circuit designed using standard lookup tables.

Marwa *et al.* [5] proposed modifications in DD carrier recovery for 16-QAM optical transmission systems. Compared to standard DD systems, the modified system proved beneficial for *S*-curve, and experiments were conducted at 11 Gbaud. The proposed system was resistant to phase noise that was

introduced during coherent systems with a signal-to-noise ratio gain of 0.8 dB in comparison to the standard approach.

Bornoosh *et al.* [6] proposed a new architecture for minimizing the phase noise of digital carrier recovery algorithms (software based) without being dependent on loop filter performance.

For RF oscillators and IF digital down converters to function properly, phase noise characteristics must be as good as possible. Simulation results demonstrated a 20 dB improvement in phase noise compared to the standard CR algorithm resulting in a simple phase estimation circuitry.

Using quadrature phase shift keying with sliding window averaging and differential decoding, Irshaad *et al.* [7] presented a new carrier recovery algorithm for 16-QAM.

The output parameters were obtained within a theoretical limit, i.e., linewidth symbol-duration product was greater than 10^{-4} and the penalty of block averaging was >0.5 dB for sliding window averaging with the target bit error rate of 10^{-3} for a measured phase noise.

Moreover, the proposed algorithm with the sliding window technique outperformed the block averaging technique for the same measured noise.

Takashi *et al.* [8], for M-QAM, proposed a new digital signal processing-based technique for a carrier phase recovery having high tolerance to large carrier frequency offset and phase noise occurring in laser systems.

Experiments were conducted on 16 and 64 QAM signals, and successful results were obtained up to a carrier frequency offset (CFO) of 1.3 GHz, i.e., as high as 10% of the symbol rate. Furthermore, there has been degradation in quality factor as large CFO led to an estimation error that was converted into a large phase noise.

Li *et al.* [9] proposed a streamlined feedforward carrier recovery algorithm for QAM. A two-stage estimation structure and a sliding block approach with low computation were proposed.

An analytical model was proposed considering optical signal-to-noise, product of laser linewidth, and symbol rate for deciding a sliding window size. Monte Carlo simulation was performed to analyze the performance of the algorithm on 16, 64, and 256 QAM signals.

It was observed that low computational efforts can be achieved for every symbol with 11% reduction in laser linewidth tolerance.

Qijia *et al.* [10] proposed a low, complex, and innovative structure for a carrier recovery loop using joint frequency for digital QAM receivers, especially for low signal-to-noise regions.

The structure was able to recover frequency as well as phase of the QAM signal. By using frequency recovery loop, the initial phase offset could be easily recovered. Significant reduction in steady-state variance was observed when a stop-and-go controller and a non-zero-mean input were introduced.

Kim and Choi [3] proposed a PD-based carrier recovery algorithm for high-order QAM signals. A carrier recovery loop was designed with PD and automatic transfer-mode controller (ATC) to detect appropriate time for mode transition in order to track a phase during a steady state.

The proposed ATC algorithm could attain a frequency offset up to ±200 kHz when compared with a conventional DD algorithm, which was < ±10 kHz.

Benani *et al.* [2] compared two DD phase detectors, namely an original phase detector and a phase frequency detector that were used in a decision feedback carrier recovery loop for the coherent demodulation of 16 QAM.

Real-time and extensive simulation results were performed for both the detectors during the procurement of phase in the actuality of phase noise. Test results exhibited that a phase frequency detector had a 15-fold increase of loop procurement range compared to a phase detector.

III. Proposed System

Figure 1 shows receiver block diagram. Digital down conversion (DDC), baseband processing, and forward error correction (FEC) decoder are the three major blocks at a receiver's side for any digital communication system. DDC converts a band limited signal from ADC to IF baseband frequency at a low sampling rate.

ADC mostly converts huge data having a small portion of a signal that consumes a narrow bandwidth in an entire spectrum of a signal on which processing needs to be performed. Extraction of a signal of interest and removal of redundant data can be carried out using DDC. The sub-components of DDC are direct digital synthesizer (DDS), a low pass filter, and a down sampler.

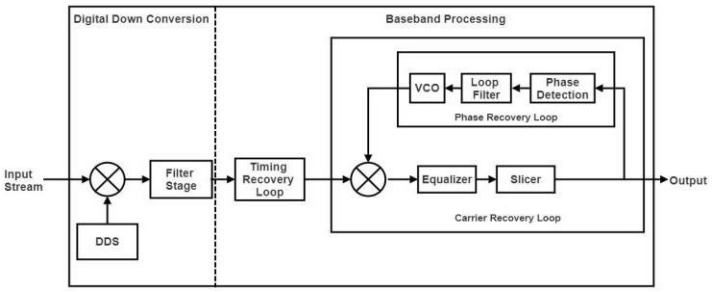

Fig. 1. Receiver block diagram

Baseband processing block consists of a timing recovery loop, a carrier recovery loop, and an adaptive equalizer. The timing recovery block extracts an optimal symbol rate or diverse symbol rates from a modulated signal to recover timing information (i.e., strobe signal), which is disseminated to the blocks.

The carrier recovery block determines phase offset caused by the difference in frequency of a received baseband signal and a receiver's local oscillator and compensates for frequency and phase difference caused by this offset. Moreover, to

reduce inter symbol interference (ISI), an adaptive filter is used.

The forward error correction (FEC) block is responsible for error correction to detect and correct a restricted number of errors in transmitted data without the requirement of retransmission. For error correction, any FEC can be used, but mostly, convolution codes are used with a Viterbi decoder for which a soft or hard input decoder can be used. In order to minimize the number of distorted bits and FEC requirements, gray code can be used. All possible transmitted symbols are compared with received complex values of QAM symbols, and the bit value of the nearest among them was sent to a decoder of FEC.

In this process, a transmitter sends—along with a data frame—a redundant error correcting code. The algorithm for a carrier recovery loop is built on the *Costas loop*.

Costa loop circuits are phase locked loop (PLL)-based circuits that are used during coherent detection to recover a carrier frequency from a suppressed carrier modulation signal and a phase modulation signal.

PLL consists of a digital voltage-controlled oscillator (VCO), phase detector, and loop filter. The process of locking to a certain frequency is as follows.

The input to the VCO is the output of the phase detector, and the output of the VCO is one of the inputs to the phase detector. The phase detector compares the VCO output with an incoming frequency and produces a DC offset voltage that is in direct proportion to the phase difference of both the frequencies.

The DC voltage is then processed through an LPF that removes high frequency noise pulses from a DC offset signal. Such a signal is then given as an input to the VCO. The output frequency generated is proportional to the DC offset value.

The output and incoming frequency are compared again and adjusted via a feedback loop until the DC offset value is zero, i.e., VCO's output frequency is locked to the input frequency.

This process is performed in the carrier recovery block, which is responsible for compensating the phase offset, thereby providing a fixed and stable constellation.

- *Advantages of the proposed system:* The proposed system operates in a purely digital domain. It is highly accurate, numerically controlled, and obtains a fixed-point constellation compared to existing models. In addition, this system will be used in upcoming technologies such as LTE, 4G, 5G, etc.

- *Limitations of the proposed system:* The efficiency of the proposed system can be increased by increasing a greater number of sample data. Moreover, conversion time can be further reduced.

IV. Results and Discussion

Table I indicates the major parameters set in the Simulink model.

TABLE I. Major Parameters Set in the Simulink Model

Sr. No.	Simulation Parameters	Values
1.	Modulation type	16-QAM
2.	Data rate (D)	8bits/sec
3.	Sampling rate	1/800
4.	Frequency symbol (F_{symbol})	1 MHz/$1e^6$
5.	Square root raise cosine filter	$\alpha = 0.5$
6.	Delay length	1
7.	Derivative gain	10
8.	Proportional gain	5
9.	Integrator	IIR Filter
10.	F_{delay}	10

Figure 2 shows carrier and timing recovery model implemented on MATLAB Simulink.

Both carrier recovery and timing are implemented as separate blocks.

The inputs to these blocks are samples with error-induced signals having carrier frequency error and symbol timing error.

In the carrier recovery block/timing recovery block, the loop filter removes noise from the error signal generated by the phase detector to provide an improved signal to the VCO.

The second-order loop filter integrated with PLL is a minimum requirement for both total tracking phase error and frequency offset.

The gain of a loop filter is fixed keeping in mind that it controls the bandwidth of PLL. Depending on the application, the PLL's bandwidth is set as there is a trade-off between the range of frequency processed and noise filtering capability.

The phase detector uses the Decision Directed algorithm, wherein the current symbol is processed and decision is made by quantizing the received sample to the nearest point in the constellation.

Quantization of received symbol is necessary to estimate the actual transmitted signal. The Decision Directed algorithm is able to function even in the presence of few errors, but when numerous errors occur in the diminutive period, the algorithm deviates; hence, the carrier recovery loop diverges.

Once the carrier recovery loop converges to correct incoming frequency, the scattering of constellation is removed.

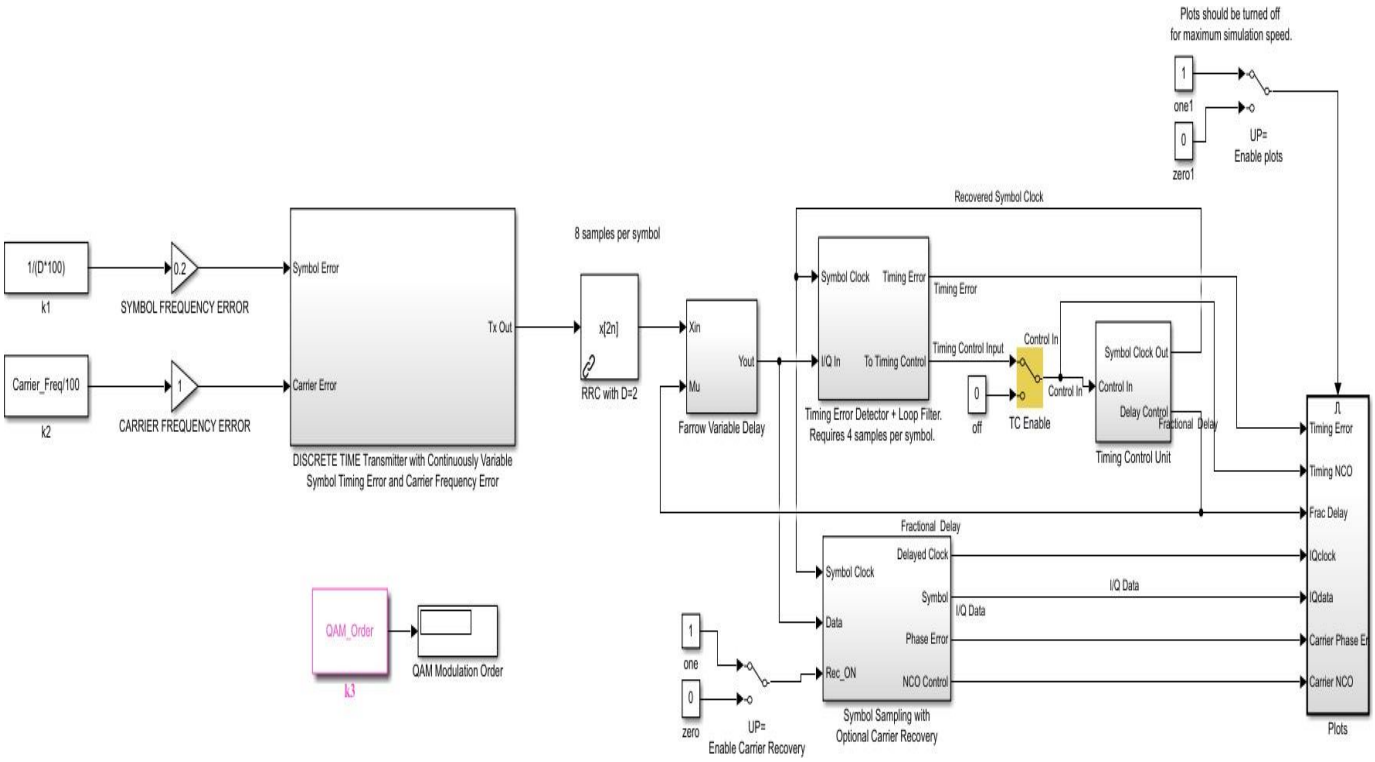

Fig. 2. Simulink model of carrier phase and time recovery loop

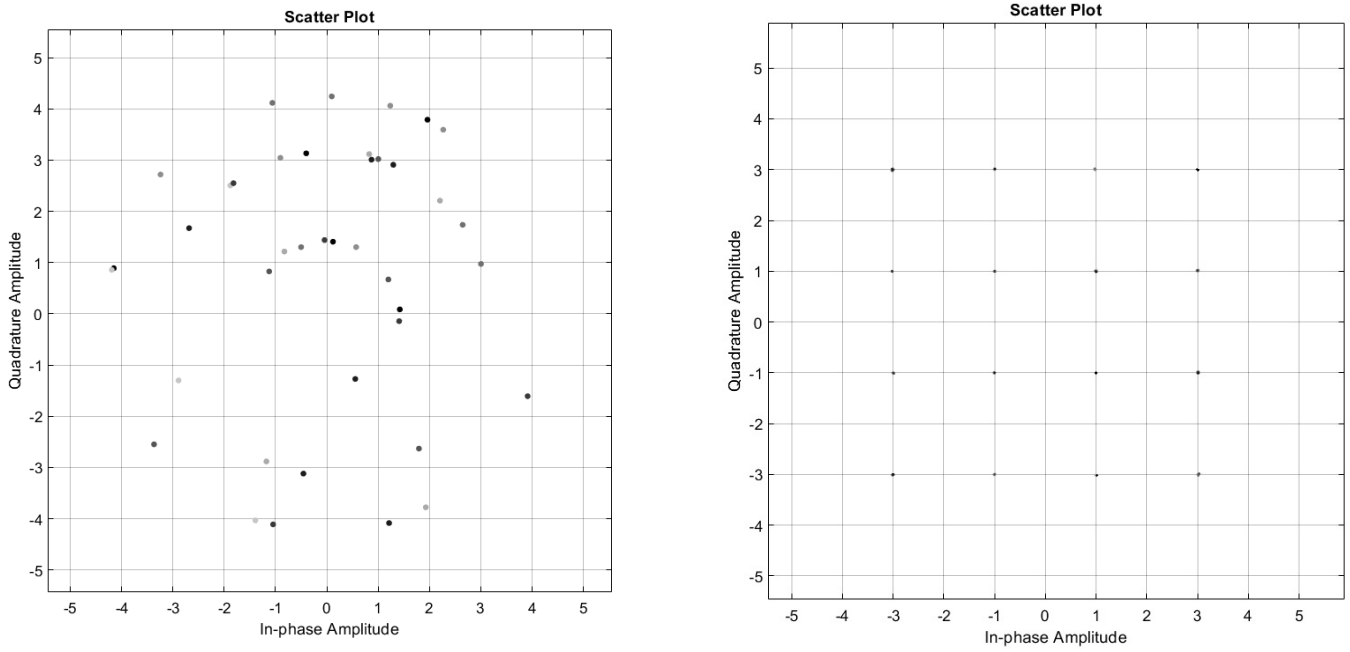

Fig. 3 QAM constellation before (left) and after (right) carrier recovery

Figure 4 shows carrier recovery block performance. From the figure 4, it is evident that the system takes <1 ms to converge to carrier frequency as observed by the output of numerical controlled oscillator, and the phase error obtained is

<0.1 radians. The initial oscillation observed in carrier phase error graph is due to the fact that the VCO undergoes many iterations until it is locked to a desired frequency. Similarly, in carrier numerically controlled oscillator (NCO), control oscillation represents the convergence of constellation (16-QAM) to its standard position.

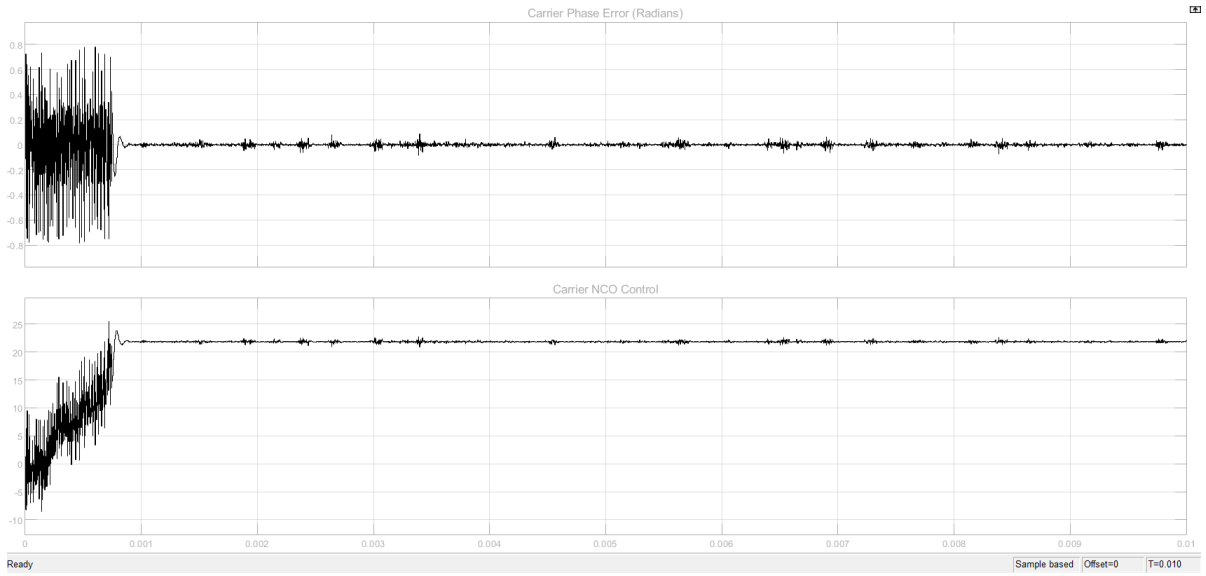

Fig. 4. Frequency recovery output

Furthermore, the functionality of the timing recovery block is similar to that of the frequency recovery block, wherein instead of frequency, PLL calculates the difference in phase between the sampling clock and the received preamble signal. The process of time loop filter is of similar functionality as mentioned above for the carrier recovery block. Since the system is under damped, the output of PLL will oscillate around the desired output as it converges. The parameters of the loop filter need to be set in such a manner in order to achieve faster acquisition and accurate tracking for optimum response. Figure 5 shows the output of timing recovery block.

From the figure, it is evident that the error is close to 0 with a constant output frequency generated by the NCO with a constant fractional delay. In the process of timing recovery, the input signal is XOR'ed with a delay version of the input signal. This process continues for many iterations until the error is close to zero, and this can be performed by varying fractional delay until it reaches a convergence point, as observed in error and fractional delay graph. High value of NCO indicates high error signals, and as observed, as error reduces, NCO value also decreases.

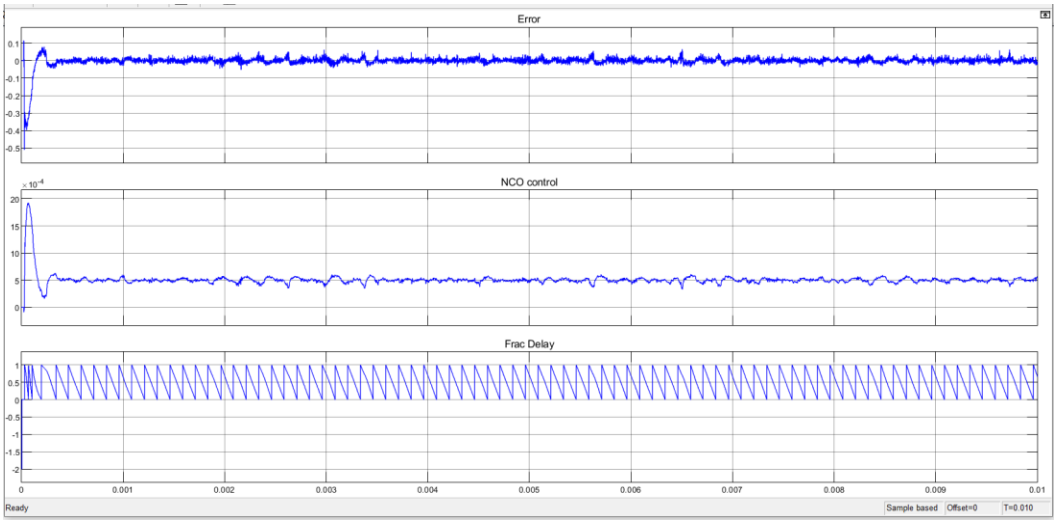

Fig. 5. Timing recovery block

V. Conclusion, Future Work, Applications

This paper presented a design for carrier phase and time recovery loop for a 16-QAM signal, which is based on the Decision Directed (DD) algorithm. For the proper functioning of the system, a second-order loop filter was used to achieve faster acquisition and tracking with appropriate filter parameters. Simulation shows good performance of the design and offers stable constellation. The system converged in < 1 ms with a phase error < 0.1 radians and timing error close to zero.

In the near future, the design process of taking the carrier phase recovery loop algorithm can be written in C/C++, and it can be synthesized, optimized, simulated, and verified in a system generator and implemented into an FPGA chip and can be directly used for a coherent system.

In addition, once programmed, these chips can be directly integrated with a communication transceiver. This system can be upgraded for next-generation telecommunication applications, satellite systems, or optical communication by keeping the model same but upgrading from 16-QAM to high-order QAM, which can be carried out by changing Simulink parameters.

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