4-Mbit (512K x 8) Static RAM

Part Number: DPA71049D02A

The DPA71049D02A is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers.

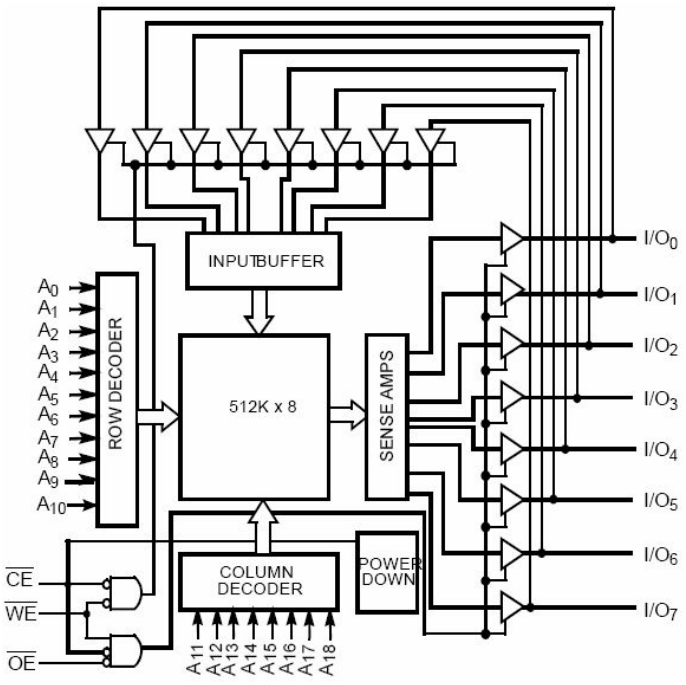
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

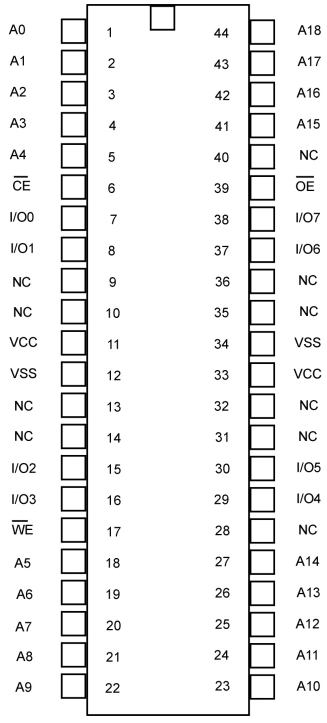
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

- **-55˚ to +125˚C operating temperature**
- **High speed**
  - **t_{AA} = 12 ns**
- **Low active power**
  - **I_{CC} = 90 mA @ 10 ns**
- **Low CMOS Standby power**
  - **I_{SB2} = 12 mA**
- **Supply voltage**
  - **5.0 V dc**
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **44-pin SO ceramic flatpack, same footprint as 44-pin TSOP II**
- **Custom packaging is available**
- **This product uses Cypress CY1049D die and is tested to meet military and space operational environment requirements.**

Logic Block Diagram



Pin Configuration



DPA Components International…. 2251 Ward Avenue…. Simi Valley, CA 93065…. (805) 581- 9200