4-Mbit (256K x 16) Static RAM

Part Number: DPA71041D02A

The DPA71041D02A is a high-performance CMOS static RAM organized as 256K words by 16 bits.

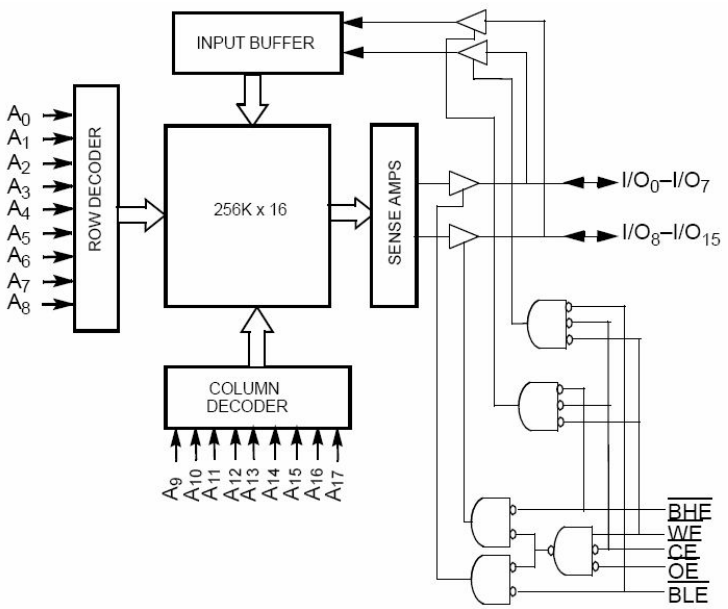
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}.

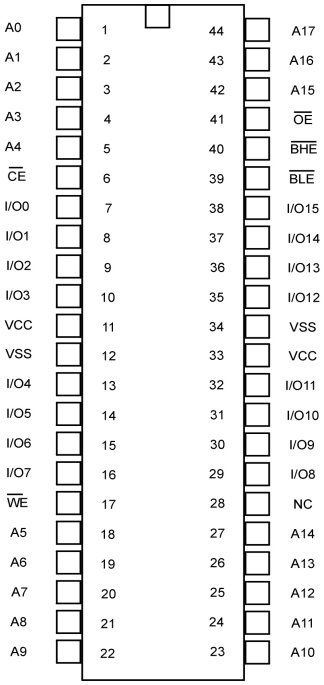
The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled ($\overline{OE}$

- **-55˚ to +125˚C operating temperature**
- **High speed**
  - **t_{AA} = 12 ns**
- **Low active power**
  - **I_{CC} = 95 mA @ 12 ns**
- **Low CMOS standby power**
  - **I_{SB2} = 15 mA**
- **Supply voltage**
  - **5.0 V dc**
- **2.0 V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **44-pin SO ceramic flatpack, same footprint as 44-pin TSOP II**
- **Drop-in replacement for Cypress CYC71041D**
- **Custom packaging is available**
- **This product uses Cypress CYC71041D die and is tested to meet military and space operational environment requirements.**

Logic Block Diagram



Pin Configuration



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