A 8.33 GHz D Flip Flop Using True-Single-Phase-Clock (TSPC)

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***Abstract*—**In this paper speed and power tradeoff are compared between TSPC and its modified version. Comparing with the conventional TSPC model which works at 5GHz with the proposed design it is seen that operating speed of the proposed design has been increased upto 8.33GHz and power consumption is reduced and this is compared on same technology at 2V. Increase in speed is achieved by eliminating one transistor from the conventional design. Divide by 2 operation is performed on the 180 nm CMOS Technology on Cadence spectre tool.

Keywords*—TSPC;DFF;ETSPC;*

I. INTRODUCTION

High speed DFFs are the basic elements in a high-speed operation of circuits. This Flip-Flop is the basic element in the frequency dividers used in PLL. Using DFF Dual modulus prescalers which are required for different division ratio of the high frequency can be made. The main parameters which are needed to be considered in the design of DFF are speed and power optimization.

There are several methods which are used to design DFF with different number of transistors used, it includes CML, TSPC, ETSPC in [4] etc. CML is the one which consumes high power and have the highest operating frequency among all. As CML consumes more power so it is not used at low frequencies, we only use it at high frequencies where other circuits cannot work. Among all known circuits TSPC circuit has the lowest power consumption(μW). After reducing one transister in each branch of TSPC circuit ETSPC in [4] is made, but it consumes more power due to short circuit currents which are increased in this circuit.

From few decades It is seen that scaling of the CMOS Technology has been very prominent and the tradeoff between delay and power has become more significant from the application point of view[2]. Therefore, designing a circuit under given specification has become difficult and these two parameters frequency divider are mainly dependent on the D flip flop circuit design.

Considering the above-mentioned requirements, in this paper design technique of D flip flop using TSPC technology has been investigated. Circuits which operates at high frequency, in the order of gigahertz, fast frequency divider which consumes less power are desired. Analyzing the known topologies for making D flip flop, it is observed that TSPC is good in performance if we consider the delay and power trade off of the circuit.

in this paper TSPC D flip flop is being compared with a design which modifies TSPC circuit which makes this circuit to operate at high frequencies then the conventional TSPC design. These two D flip flops are designed on Cadence Spectre tool 180 nm CMOS Technology.

Arrangement of rest of the paper is in this manner. Section II discusses TSPC design and proposed design. Section III ends up with the conclusion.

II. TSPC D FLIP FLOPS

A. TSPC D flipflop

TSPC DFF's setup time can be written as Tsetup = $t_{D\text{-}X}$, where $t_{D\text{-}X}$ shows the propagation time from node D to node X. The total propagation delay of the circuit by [3] can be found by

$$t_{X\text{-}Q} = t_{X\text{-}Y} + t_{Y\text{-}QBAR} + t_{QBAR\text{-}Q} \quad (1)$$

where $t_{D\text{-}QBAR}$ and $t_{D\text{-}Q}$ are the propagation delay from CLOCK to Q_{BAR} and Q, respectively. $t_{X\text{-}Y}$, $t_{Y\text{-}QBAR}$, $t_{QBAR\text{-}Q}$ shows the propagation delay from node X to Y, Y to QBAR, and QBAR to Q, respectively. One of the advantage of TSPC is that OR and AND gate logic are working in the first stage of TSPC D flip flop itself, which makes the first stage of TSPC as clocked NAND/NOR Gate. Due to which the logic that is reduced to the amount of two inverter delay. Actually, there are lot of structures by which we can realize TSPC DFF but the optimize design is to use only one AND/OR logic Gate before TSPC DFF. As TSPC utilizes AND/OR logic gates in first stage, which further the reduction in logic depth, area, power. After making the design of circuit, design rules are considered and changed by [1].

Maximum frequency at which a TSPC flip flop can be operated is obtained by the formula In [5] equation (2)

$$f_{max}=\frac{1}{2\times\max(t_{pLH},t_{pHL})} \quad (2)$$

Power of the circuit is directly dependent on the operating frequency. TSPC DFF proposed in [8] shown in figure 1 in which transistors are placed near the power supply to enhance the switching speed.

Working of three stages of TSPC DFF as shown in Fig. 1 can be seen as follows. In Fig.2 we can see that First stage takes input data in negative cycle of clock and holds it during

positive half of the cycle. Now the second stage precharges node Y in the negative cycle of the clock and then it evaluates the data in the positive cycle, finally the third stage passes the evaluated data in the positive cycle and holds it in the negative cycle and This is the output.

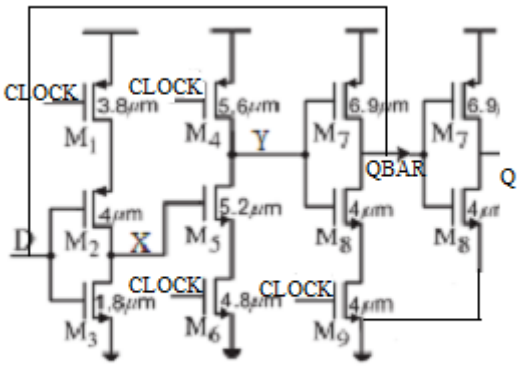

Fig. 1 Conventional design for TSPC D flip flop

That is why the result of the evaluation in the 2nd stage determines output of DFF.At the time when input is high, node Y charge is hold and QBAR goes low after clock goes high. However, when input is low, node Y need to be discharged before QBAR goes high, this limits the speed of TSPC operation. As the 2nd Stage works like the Domino logic, increasing one transistor at node Y makes NOR logic due to which output can be changed without passing from first stage.

B. Proposed DFF

In our proposed design in Fig. 3 we are exploiting the fact that in second branch TSPC one transistor can be reduced and instead of using complementary clock we can use PMOS only for clock signal and one NMOS transistor is eliminated which results in increase in maximum operating frequency upto which divide by 2 operation can be performed. By eliminating 1 transistor from the 2nd stage we are using the concept of ratioed logic [5]. According to this logic the circuit is made fast at the evaluation phase because as soon as the value of X node goes high in the

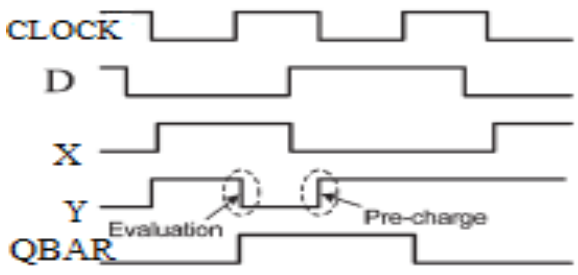

Fig. 2 Waveforms for the Flip Flop at different stages.

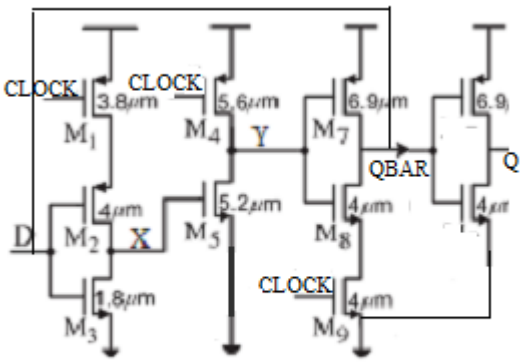

Fig. 3 Proposed design for D flip flop.

negative cycle of the clock Y node charges as per the concept of ratioed logic and it does not charge to the fullest so that at the time of discharge it does not discharges from the highest value which makes the charging discharging of the circuit fast and also the load capacitance of the second stage is reduced, which makes the overall speed of the circuit faster than the conventional TSPC design. In this circuit power consumption is slightly increased because of 2nd stage short circuit current. Therefore, this design can work at highest speed as compared to conventional TSPC design at the cost of very small increasing power consumption.

III. Simulations and Results

Proposed design of D flip flop is compared with the conventional TSPC D flip flop in Table I. This D flip flop is designed in a 180 NM CMOS Technology on Cadence spectre simulator. Since the design of conventional TSPC D flip flop proposed in [5] is at 130 nm CMOS technology therefore which resimulated the same design in 180 NM CMOS Technology as shown is Fig.4.Now the propose design can be fairly compared with the conventional design. Applied clock signal is a square waveform with peak swing of 2V. The simulation is done with 2V power supply and waveform is shown in Fig. 5. Maximum operating frequency calculated as output showing of 1.8V.for the reference TSPC divide if taken into consideration because maximum operating frequency and power are compared with the proposed design. At maximum operating frequency power consumption of both the circuits are compared in the results. From figure 3 it is clear that operating frequency of the proposed design has increased.

In addition, there is always a tradeoff between the maximum operating frequency and the lowest operating frequency, so if we increase the highest operating frequency used to creating frequency tends to increase as well. Maximum operating frequency of the proposed design is normalized to TSPC D flip flop, then speed of proposed design comes out to be 66% more then the conventional design.

TABLE I. Comparison Table

Design Parameters	Work in [1]	Work in [1] Resimulated/measured	Presented work (Sim/measured)
Process(µm CMOS)	0.13	0.18	0.18
Supply Voltage(V)	1.2	2	2
Max. frequency(GHz)	5	5	8.33
Power(mW) at maximum operating frequency	-	1.278	2.201

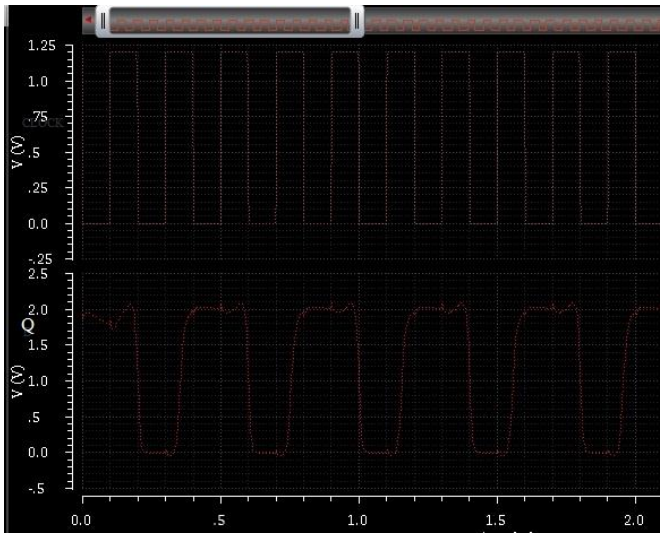

Fig. 4 Waveforms for the Resimulated conventional Flip Flop output.

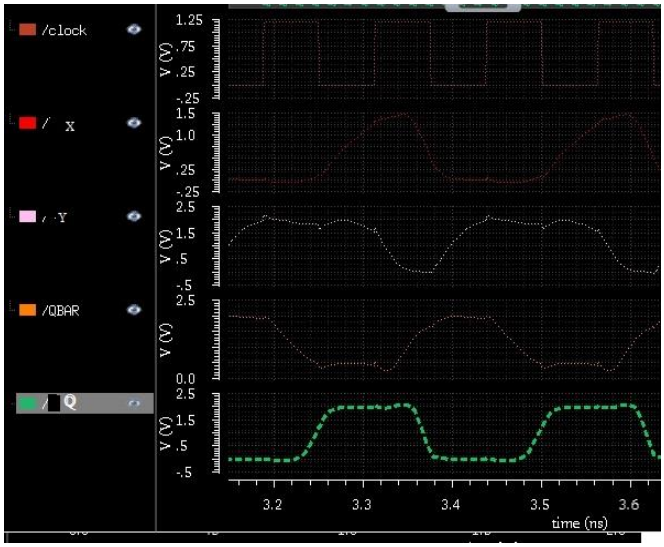

Fig. 5 Waveforms for the Proposed Flip Flop at different stages.

IV. CONCLUSION

D Flip flop is the most important block in designing of frequency dividers which are used in PLL. In this paper TSPC design for D flip flop has been modified to increase the operating frequency on the cost of slight increasing power consumption. Due to this change in the design of TSPC maximum operating frequency is increased to 8.3 gigahertz. Area, delay and load capacitance of the circuit is reduced. We can see the circuit as an intermediate design between TSPC and ETSPC circuits and the main advantage of this circuit is that it is working at higher frequency than the conventional design and the power consumption is just slightly increased.

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