A Review Paper on Effective Methodology for IC Compiler Power Optimization

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Abstract—In this mobile era, low power design is very important. In the DSM technology, efforts have been made to improve the power in every aspect of the design. From architecture to RTL coding, from RTL to GDS implementation. Electronic design automation (EDA) vendors are implementing various algorithms and techniques in their implementation tool to reduce/optimize power. Power optimization using the automatic place & route tools, helping in optimizing (reducing) the power consumption of a digital design. To meet this challenge, researchers have developed many different design techniques to reduce power. The complexity of today's ICs, with over 100 million transistors, clocked at over 1 GHz, means manual power optimization would be hopelessly slow and all too likely to contain errors. Computer-aided design (CAD) tools and methodologies are mandatory.

Index Terms **—** VLSI, Low Power Design, Power Dissipation, Dynamic Power, DSM, ICC II,

I. INTRODUCTION

One of the key features that led to the success of complementary metal-oxide semiconductor, or CMOS, technology was its intrinsic low-power consumption. This meant that circuit designers and electronic design automation (EDA) tools could afford to concentrate on maximizing circuit performance and minimizing circuit area. Another interesting feature of CMOS technology is its nice scaling properties, which has permitted a steady decrease in the feature size (see Moore's law), allowing for more and more complex systems on a single chip, working at higher clock frequencies.

The rate of dissipating the energy from the source to the system over a time is basically referred to as power dissipation. It is basically classified into two categories:

1 Peak Power 2. Average Power

Maximum instantaneous power over a time is known as Peak power which makes the device less reliable by introducing the glitches due to which the system may not work properly. Cooling and packing of the system are affected by average power. In current scenario, battery lifetime is a decisive factor for the commercial success of the product. A high absolute level of power is not only undesirable for economic and environmental reasons, but it also creates the problem of heat dissipation. In order to keep the device working at acceptable temperature levels, excessive heat may require expensive heat removal systems. In fact, power consumption is regarded as the limiting factor in the continuing scaling of CMOS technology[11].

In this review paper section II consists of Literature Review, section III Power analysis of CMOS circuits, section IV IC Compiler- An overview, Section V METHODOLOGY, section VI consists of Conclusion.

2 LITERATURE REVIEW

Sung-mo kang et al , [1] have described the need of low power design and also proposed the different methodology to achieve low power consumption. This chapter has primarily concentrate on the circuit –or transistor-level design.

Gary Yeap , [2] have described different technique to reduce the leakage and static current, switching voltage, capacitance, switching frequency and find out several popular figures of merits for low power design.

Mr.Suhas D.kakde et al.[3] have proposed the different low power design strategies. And also provided the different factors to reduce the switching activity. And also realized that low power interconnect using advance technology reduced swing or reduced activity approaches.

Kamal K Mehta, [4] have covered literature review of dynamic power dissipation aspect and related technical issue. And also elaborated various factor to reduce power dissipation. This paper discuss about residue effect on system design after dynamic power problem is incorporated.

Wasim Maroofi et al [5] have described the design methodologies for low power VLSI architecture. In this paper all the methodologies are accomplished in 90nm CMOS technology. And it also describe the importance of extended battery life.

Ambily Babu, [6] have described the various source of power dissipation in digital CMOS and the power optimization technique at circuit and device level. And also described the various expression related to power dissipation.

IC Compiler II (ICC2) is a complete place and route system delivering industry-best quality-of-results (QoR) for designs across all process nodes, while enabling unprecedented productivity. IC Compiler II is specifically designed to address today's hypersensitive time to market pressures with innovative solutions for flat and hierarchical design planning,

early design exploration and prototyping, placement and optimization, clock tree synthesis, routing, manufacturing compliance, and low-power challenges[7].

3 POWER ANALYSIS OF CMOS CIRCUITS

3.1 Power consumption:

The power consumption of digital CMOS circuits is generally considered in terms of three components.[5]

- The switching power component, related to the charging and discharging of the load capacitance at the gate output.
- The short-circuit power component. During the transition of the output line (of a CMOS gate) from one voltage level to the other, there is a period of time when both the PMOS and the NMOS transistors are on, thus creating a path from VDD to ground.
- The static power component, due to leakage, that is present even when the circuit is not switching. This, in turn, is composed of two components - gate to source leakage, which is leakage directly through the gate insulator, mostly by tunneling, and source-drain leakage attributed to both tunneling and sub-threshold conduction[5]. The contribution of the static power component to the total power number is growing very rapidly in the current era of Deep Sub-Micrometer (DSM) Design. In DSM technology leakage power dissipation in a cell becomes significant.

3.2 Power Estimate at different levels:

Power can be estimated at a number of levels. The higher levels of abstraction are faster and handle larger circuits, but are less accurate. The main levels include [8]:

- Circuit Level Power Estimation, using a circuit simulator such as SPICE.
- Static Power Estimation does not use the input vectors, but may use the input statistics. Analogous to static timing analysis.
- Logic-Level Power Estimation often linked to logic simulation.
- Analysis at the Register-Transfer Level. Fast and high capacity, but not as accurate.

3.2 *Power* Dissipation:

Power dissipation is of basically of two types-

A) Static power B) Dynamic power

Static power is constituted due to leakage currents and it is produced by the reverse bias current whereas dynamic power is constituted by short circuit power and capacitive switching power.

Total power dissipated by a digital circuit is given by:

$$\mathbf{P_{(Total)} = P_{(Static)} + P_{(Dynamic)} + P_{(Short\ Circuit)}}$$

Where $P_{(Dynamic)}$ is the dynamic power dissipation due to switching of transistors, $P_{(Short\text{-}circuit)}$ power is the short-circuit current power dissipation when there is a direct current path from power supply down to ground.

3.3 *Source of Power Dissipation*

Power dissipation in digital CMOS circuits is caused by four sources as follows.

1) The leakage current, which is primarily determined by the fabrication technology, consists of two components:
   - Reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor.
   - The sub-threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage,
2) The standby current which is the DC current drawn continuously from V_{dd} to ground,
3) The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions,
4) The capacitance current which flows to charge and discharge capacitive loads during logic changes.

3.4 *Power Minimization Techniques*

The challenge to reduce power, the semiconductor industry adopted a multi-faceted approach, attacking the problem from many fronts[12]:

1) Reduction in chip and packaging capacitance: Achieved through process development, SOI with partially or fully depleted wells, CMOS scaling to submicron device design size, and advanced interconnected substrates such as Multi-Chip Modules (MCM).
2) Scaled supply voltage: Very effective in reducing the power dissipation, but requires new IC fabrication process system. Supply voltage scaling also requires support circuitry for low-voltage operation.
3) Improving design techniques: Can be very successful as the cost to reduce power by design is relatively small in comparison to the other approaches and considered high in potential.
4) Power management strategies: various static and dynamic power managing techniques are application dependent, but, also prove to be significant.

4 IC COMPILER- AN OVERVIEW

IC Compiler is an integral part of the Synopsys Galaxy Design Platform that delivers a complete design solution, including synthesis, physical implementation, low-power design, and design for manufacturability (DFM). IC Compiler is a single, convergent, chip-level physical implementation tool that includes flat and hierarchical design planning, placement and optimization, clock tree synthesis, routing, DFM, and low-power capabilities that enable designers to implement today's high-performance, complex designs. Widely adopted and recognized as the industry standard for physical implementation, IC Compiler provides best-in-class quality of results (QoR), strong signoff correlation, and powerful DFM capabilities.

5 METHODOLOGY

In this paper, focus is to optimize leakage power. Author studied the leakage power optimization technique offered by Synopsys ICC tool. After detailed study of power optimization and tool capabilities, author decided to use a methodology in ICC to optimize leakage power. For leakage power optimization, the following methodology setup was used.

5.1 Design multi-Vt setup

For implementation, Multi-Vt flow will be used. All the cell variant (Ultra low leakage/ low leakage/ nominal leakage) will be used during partition execution and timing ECO [9].

5.2 MCMM setup for power optimization

Power specific corner and scenario will be used in design for ICC2 power optimization. By default, power scenario will be active throughout the flow [10].

6 CONCLUSION

In this paper, evaluated ICC2 power optimization capabilities on design and various power reduction techniques are reviewed. Used the all Leakage power optimization capabilities of ICC2 and performed power analysis. Design for low power CMOS circuits implies the skill to reduce the power consumption. Various technologies have various trade offs and their selection is made as per the requirement. It can help the designers to understand the basics of low power. Future challenge in this field is to make a perfect balance between various factors that contribute to dynamic power dissipation.

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