Study of Field-Effect Transistors and Construction and Characteristics of JFET's

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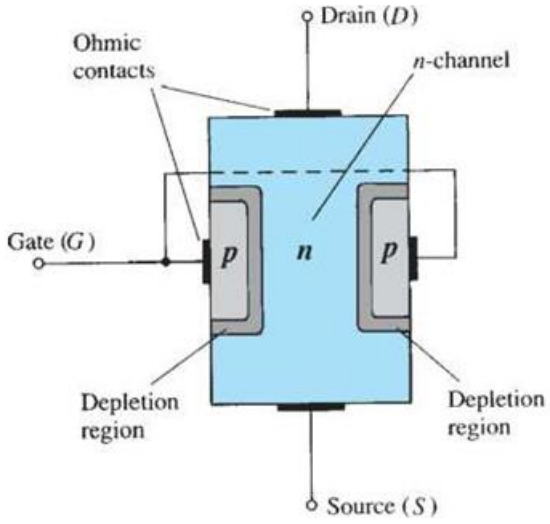
Abstract- The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. JFET transistor is a voltage-controlled device. For the FET the current ID will be a function of the voltage VGS applied to the input circuit. The FET is a unipolar device depending solely on either electron (n- channel) or hole (p -channel) conduction.
The term field effect in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

Key Words- FET, JFET, MOSFET, MESFET

Type of FET:

Three types of FETs:
the junction field-effect transistor (JFET), the metal-oxide- semiconductor field-effect transistor (MOSFET), and the metal-semiconductor field-effect transistor (MESFET). The MOSFET category is further broken down into depletion and enhancement types. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

CONSTRUCTION AND CHARACTERISTICS OF JFETs
JFET is a three-terminal device with one terminal capable of controlling the current between the other two. The major part of the structure is the n-type material, which forms the channel between the embedded layers of p-type material. In the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. that resembles the same region of a diode under no-bias conditions.



VG = 0 V, VDs Some Positive Value

A positive voltage VDS is applied across the channel and the gate is connected directly to the source to establish the condition VGS =0 V .Under the conditions the flow of charge is relatively uninhibited and is limited solely by the resistance of the n-channel between drain and source. The depletion region is wider near the top of both type materials. The current ID will establish

the voltage levels through the channel as indicated on the figure. The result is that the upper region of the p-type material will be reverse-biased by about.

As the voltage VDS is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of ID versus VDS.AS VDS increases and approaches a level referred to as VP, the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If VDS is increased to a level where it appears that the two depletion regions would touch", a condition referred to as pinch-off will result.

FIG 3 JFET at VGS = 0 V and VDS 7 0 V

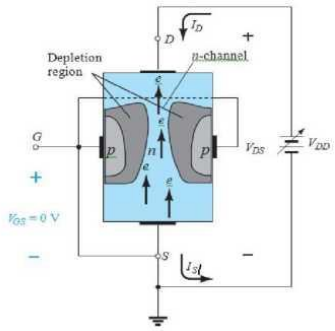
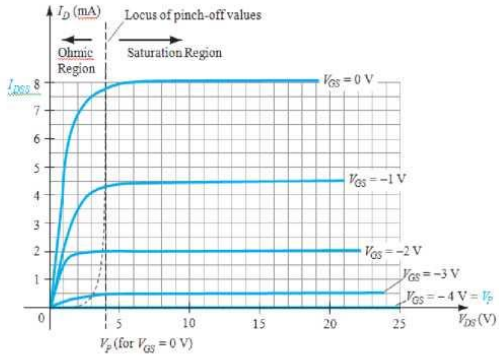


FIG 4 ID versus VDS for VGS = 0 V.



As ^{V}DS is increased beyond ^{V}P, the region of close encounter between the two depletion regions increases in length long the channel, but the level of ^{I}D remains essentially the same. In essence, therefore, once ^{V}DS 7 VP the JFET has the characteristics of a current source. As shown in Fig.5, the current is fixed at ^{I}D = ^{I}DSS, but the voltage ^{V}DS (for levels 7 VP) is determined by the applied load.

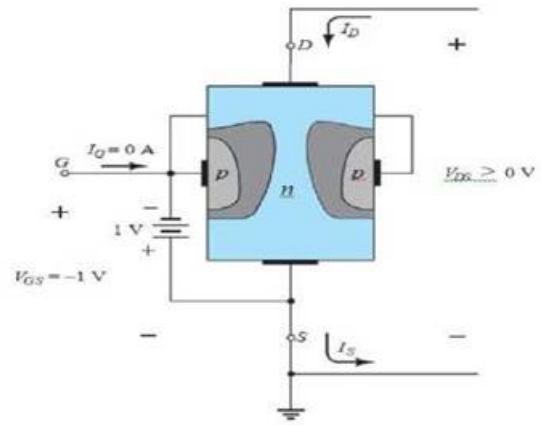
The choice of notation ^{I}DSS is derived from the fact that it is the drain-to-source current with a short circuit connection from gate to source. ^{I}DSS is the maximum drain current for a JFET and is defined by the conditions ^{V}GS =0 V and

^{V}DS>| VP |

VGS < 0 V

The voltage from gate to source, denoted ^{V}GS, is the controlling voltage of the JFET. Curves of ^{I}D versus $^{V}_{DS}$ for various levels of ^{V}GS can be developed for the JFET. For the n-channel device the controlling voltage ^{V}GS is made more and more negative from its ^{V}GS = 0 V level. The effect of the applied negative-bias ^{V}GS is to establish depletion regions similar to those obtained with ^{V}GS 0 V, but at lower levels of $^{V}_{DS}$ Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of $^{V}_{DS}$, as shown in Fig. 6 for ^{V}GS = - 1 V. The resulting saturation level for ^{I}D has been reduced and in fact will continue to decrease as ^{V}GS is made more and more negative. Eventually, ^{V}GS when ^{V}GS = - ^{V}P will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of ^{V}GS that results in ^{I}D = 0 mA is defined by ^{V}GS =^{V}P, with ^{V}P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs



Comparison of some of the general characteristics of BJT with FET:

One of the most important characteristics of the FET is its high input impedance. The variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage.

FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips. The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

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