Design and Analysis of Multiplexer and Demultiplexer using different Low Power and High Speed Adiabatic Logic Techniques

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Abstract **-** The main objective of this paper is to minimize leakage power dissipation and achieve high performance in digital circuits. Now-a-days, with more devices becoming portable and battery operated, the power dissipation in a device is becoming a major concern. Moreover with the technology change, the number of transistors in a chip is also increasing at a rapid rate. By the increase in more number of transistors in a chip, it occupies more area and subsequently the power dissipation in the form of heat also grows. Adiabatic circuits are the low power circuits where the power dissipation is very less compared to standard CMOS. Adiabatic logic circuits use energy recovery to minimize power dissipation. Following this trend, this paper presents an ADIABATIC LOGIC based design approach for low power and high speed adiabatic 8*1 Multiplexer and 1*8 Demultiplexer. Including that some standard adiabatic logic styles like ECRL, 2N2N2P, PFAL are implemented. These adiabatic logic styles have been improved by designing proposed logic. All the simulations are carried out in TANNER EDA TOOL V15.0 at 250nm technology for implementing the design techniques.

Keywords*---Adiabatic logic, Multiplexer, Demultiplexer, CMOS, ECRL, 2N2N2P, PFAL, Proposed Logic, Delays, Power disisipation, Power saving.*

I. INTRODUCTION

Due to the shrinking size of systems in today's period of technology, researchers in the field of low power microelectronics have become responsible for handling low power concerns along with reduced size, which in turn increases the power dissipation in the form of heat. The most popular logic for implementing different designs is CMOS logic. Though CMOS technology provides circuits with low static power dissipation during switching operation, but the major concern with CMOS is it has very large switching power consumption, which directly depends on the switching frequency. There are three main sources of power dissipation in digital circuits: dynamic, short circuit, leakage power [1].

$$P_{total} = P_{static} + P_{dynamic}$$

$$P_{static} = P_{sc} + P_{leak}$$

$$= I_{sc} V_{dd} + I_{leak} V_{dd}$$

$$P_{dynamic} = C_L V_{dd}^2 f_{clk}$$

P_{static} is the static power dissipation of CMOS which includes both short circuit power and leakage power, which is very less compared to other logic circuits. $P_{dynamic}$ is the dynamic power dissipation which directly depends upon the switching frequency f_{clk}, combined load capacitance C_L and is directly proportional to square of supply voltage V_{dd}. In order to reduce power dissipation in CMOS, the first step to do is to constrict V_{dd}, but it lowers the performance of the circuit. Another technology parameter is C_L and it depends on device intrinsic capacitances. In CMOS, the total energy taken from the supply is $C_L V_{dd}^2$, in that half of the energy gets dissipated in transistors and the other half is stored in capacitors. The lower bound of energy dissipation in CMOS is (1/2) $C_L V_{dd}^2$.

II. LITERATURE REVIEW

Adiabatic logic is the latest approach for power saving in digital circuits. It is different from static CMOS because instead of using oscillating power supply, it uses the so called power clock. It is also called as "Reversible Logic" because the energy taken from the supply for logic implementation is again given back to the supply. The adiabatic term is taken from thermodynamics, which means "no exchange of heat/energy". Though CMOS technology provides low static power dissipation, during switching operation, currents are generated due to the discharge of load capacitances; it causes the power dissipation that increases with an increase in clock frequency. Such losses were prevented by the adiabatic logic technique, because the charge doesn't flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage, the power clock, and the power can be reused [2]. This is the main reason that adiabatic circuits are used as low power VLSI circuits.

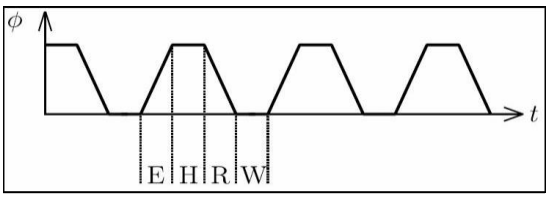

Figure 1.Trapezoidal four-phase power clock

Each of the power clock cycle consists of four intervals as shown in Figure.1, where at the first stage, in the Evaluate (E) interval; the outputs are evaluated from the stable input

signals. During the next stage of Hold (H) interval, the outputs are kept stable and then passed to the next subsequent stable input signal. In the Recover (R) stage, the energy is recovered again back from the supply. In the final stage of Wait (W) interval, as for symmetry reasons it is introduced, so similarly for the symmetrical signals also, it becomes easier and more efficient to be executed.

III. ADIABATIC LOGIC TECHNIQUES

Adiabatic logic circuits are classified into two types as:
(a)Partial/Quasi adiabatic logic circuits
(b)Full adiabatic logic circuits

(a) Partial/Quasi adiabatic logic circuits: In these circuits, the adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power clock [3]. These circuits have simple architecture and power clock system. Some of the popular partial adiabatic logic circuits are ECRL, 2N2N2P, PFAL, NERL, CAL etc.

(b) Full adiabatic logic circuits: These circuits have no adiabatic loss, because the complete charge on the load capacitance is recovered back by the power supply. The transistor requirement for these circuits is more, so the architecture design is more complex. Some of the full adiabatic logic circuits are PAL, SCRL.

In this paper, the standard partial adiabatic logic techniques like ECRL [2] [4] [7], 2N2N2P [2] [5] [7], PFAL [2] [6] [7] are discussed as follows:

A. Efficient Charge Recovery Logic (ECRL):

ECRL is suggested by Y.MOON and D.K.JEONG [4]. It is shown in Figure.2; this logic uses two cross-coupled P-MOS transistors M1 and M2 to store the output logic value and also uses two N-MOS transistors blocks for the logic implementation of the ECRL adiabatic logic [8]. The structure of this logic looks like Cascode Voltage Switch Logic (CVSL) with differential signalling. This logic produces full output swing because of the cross-coupled P-MOS transistors in both precharge and recovery phases and as well as this circuit suffers from non-adiabatic loss because of the threshold voltage V_{tp} *i.e.*, required to turn ON the PMOS transistors. The amount of loss in ECRL logic is given as:

$$E_{ECRL} = C_L |V_{tp}^2| /2$$

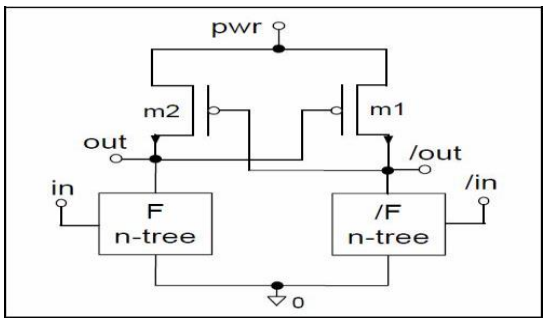

Figure 2.ECRL General Schematic

B. 2N2N2P:

This is one of the logic belongs to quasi adiabatic logic family, which is derived from ECRL in order to reduce coupling effect. This logic consists of two back to back CMOS inverters which are considered as a latch as shown in Figure.3, but the major advantage [9] over ECRL is that it consists of two cross-coupling NMOS switches which leads to non-floating outputs for the major part of the recovery phase. The main difference between ECRL over 2N2N2P is, it has a pair of cross-coupled NMOS transistors instead of cross-coupled PMOS transistors [6]. This logic family is very much similar to standard SRAM cell as it has cross coupled inverters.

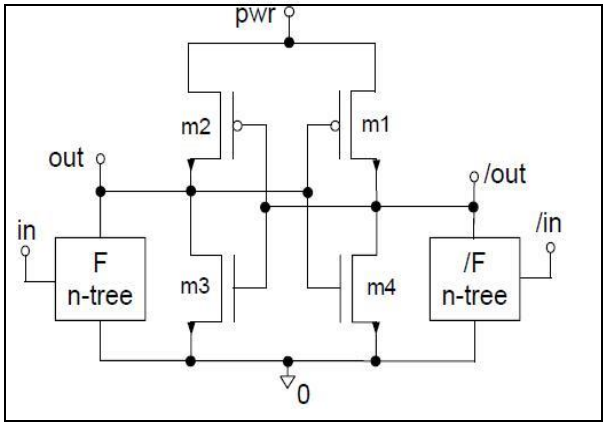

Figure 3.2N2N2P General Schematic

C. Positive Feedback Adiabatic Logic (PFAL):

This logic is also named as dual rail circuit, because, this logic provides with partial energy recovery [10], [11]. As compared to other similar logic families, PFAL has the lowest energy consumption and a good robustness against technological parameter variations [12]. This circuit is similar to 2N2N2P, but the basic difference to PFAL [5] over 2N2N2P is, two NMOS trees are connected in parallel with two PMOS. The logic implementation of PFAL is done under the two NMOS blocks. The PFAL gates is an adiabatic amplifier, a latch made by two PMOS M1-M2 and two NMOS M3-M4 as shown in Figure.4, because of this it avoids a logic level degradation on the output nodes out and $\overline{out}$.

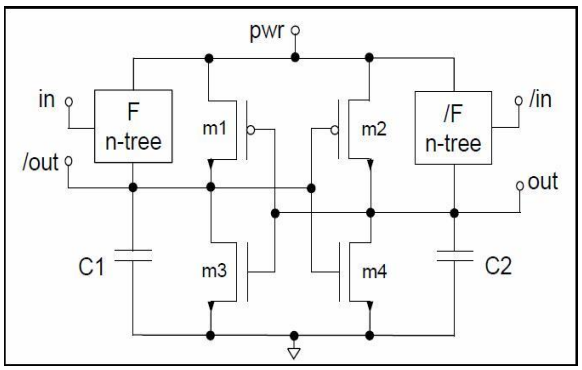

Figure 4.PFAL General Schematic

While the previous paper works are done on Multiplexer based Adiabatic Logic, which involves the usage of NMOS pull down configuration [13], cross coupled inverters [14], Two Phase Drive Adiabatic Dynamic CMOS Logic (2PADCL) [15], now this paper analyses the total power dissipation of the multiplexer and the demultiplexer using different standard logic styles and proposed a new logic style with lesser power dissipation [16], [17], [18].

The paper is précised as follows: the block diagram, truth table and the output expressions of multiplexer and demultiplexer is given in section IV. In section V, proposed logic circuit is described and in section VI, all the schematic designs and their simulated output waveforms are prescribed at 250nm technology. Finally, the comparative analysis based on area per chip based on transistor count, power dissipation and delay is done on section VII.

IV. EXPRESSIONS FOR MULTIPLEXER AND DEMULTIPLEXER

Multiplexer is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexer is also called as "Data Selector". It consists of 'I' given data inputs and 'S' selection inputs which is directly routed to a single output line 'Y' based on selection of inputs [19].

The block diagram of 8*1 Multiplexer is shown in Figure.5.

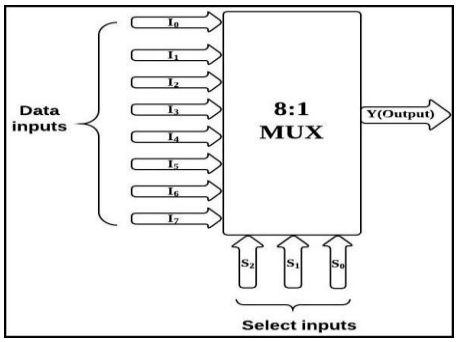

Figure 5.Block Diagram of 8*1 Multiplexer

TABLE I. Truth table of 8*1 Multiplexer

Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

From the table I, 8*1 Multiplexer output is deduced in the following way:

$$Y= \bar{S}_2\bar{S}_1\bar{S}_0I_0 + \bar{S}_2\bar{S}_1S_0I_1 + \bar{S}_2S_1\bar{S}_0I_2 + \bar{S}_2S_1S_0I_3 + S_2\bar{S}_1\bar{S}_0I_4 + S_2\bar{S}_1S_0I_5 + S_2S_1\bar{S}_0I_6 + S_2S_1S_0I_7$$

The reverse operation of the digital Demultiplexer is the digital Multiplexer. Demultiplexer is a device that takes a single input line and routes it to one of several digital output lines [16]. It consists of 2^n outputs with 'n' selection lines, which are used to select which output line to send from the input. Demultiplexer is also called as "Data Distributor".

The block diagram of 1*8 Demultiplexer is shown in Figure.6.

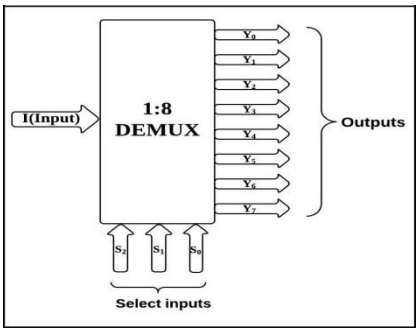

Figure 6.Block diagram of 1*8 Demultiplexer

TABLE II. Truth table of 1*8 Demultiplexer

Selection Inputs			Outputs							
S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	I	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

From the table II, 1*8 Demultiplexer output is deduced in the following way:

$$Y_0 = \bar{S}_2\bar{S}_1\bar{S}_0I$$
$$Y_1 = \bar{S}_2\bar{S}_1S_0I$$
$$Y_2 = \bar{S}_2S_1\bar{S}_0I$$
$$Y_3 = \bar{S}_2S_1S_0I$$
$$Y_4 = S_2\bar{S}_1\bar{S}_0I$$
$$Y_5 = S_2\bar{S}_1S_0I$$
$$Y_6 = S_2S_1\bar{S}_0I$$
$$Y_7 = S_2S_1S_0I$$

V. PROPOSED LOGIC CIRCUIT

The proposed logic circuit follows the conventional CMOS logic inverter, which is also driven by a single power supply, $P_{CLK.}$ The major difference of proposed circuit over CMOS inverter is, it has addition of two extra MOS transistors, one above the PMOS transistor and one below the NMOS transistor as shown in Figure.7, here the pull up end has the extra PMOS transistor and the pull down end has the extra transistor, where these two extra transistors are biased in saturation region as their drain and gate are shorted [16]. Addition of these two transistors results in power reduction of the circuit.

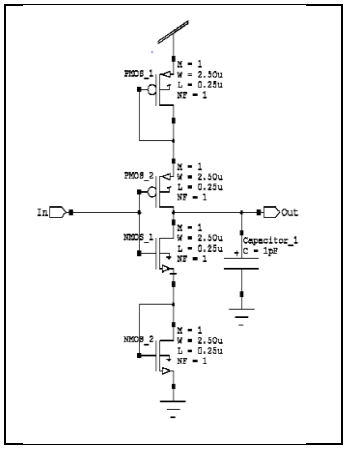

Figure 7.Basic Proposed Logic Inverter Schematic

In the evaluation and precharge phase of the power supply P_{CLK}, it swings up and down and the voltage that is stored inside the load capacitor C_L is transferred back to the supply. In this way, the energy is gained back from the output.

VI. SIMULATIONS AND WAVEFORMS

A. *Standard CMOS (8*1 Multiplexer):*

The schematic design of Standard Complementary MOS circuit for 8*1 Multiplexer is given in Figure.8.

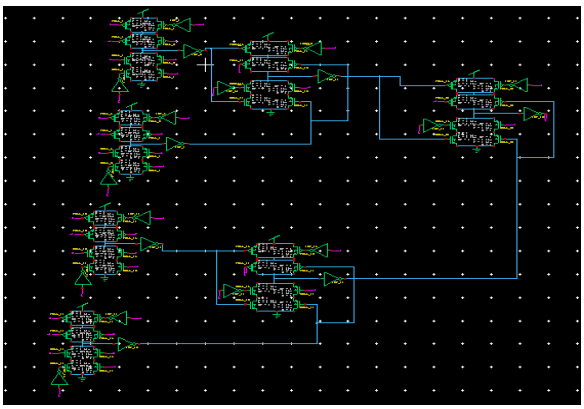

Figure 8.CMOS 8*1 Multiplexer Schematic Design

Upon simulation, the output waveform obtained for the CMOS circuit is given in Figure.9.

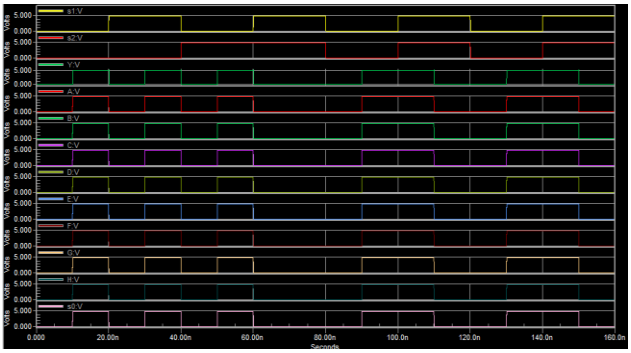

Figure 9.CMOS 8*1 Multiplexer Output Waveform

B. *ECRL (8*1 Multiplexer):*

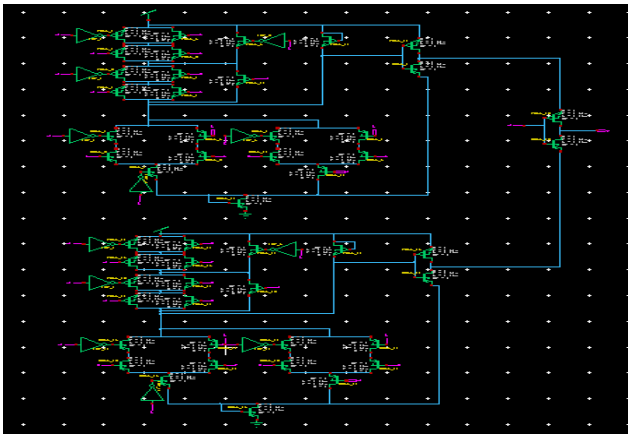

Figure 10.ECRL 8*1 Multiplexer Schematic Design

The NMOS Pull-down is used for implementing the necessary N-tree logic block (F) and similarly the inversion of ($\bar{F}$) logic block is designed by using PMOS. The required inputs and its complements for F and $\bar{F}$ is given according to the selection inputs as shown in Figure.2 &10.

Upon simulation for the above ECRL 8*1 Multiplexer, the output waveform is given in Figure.11.

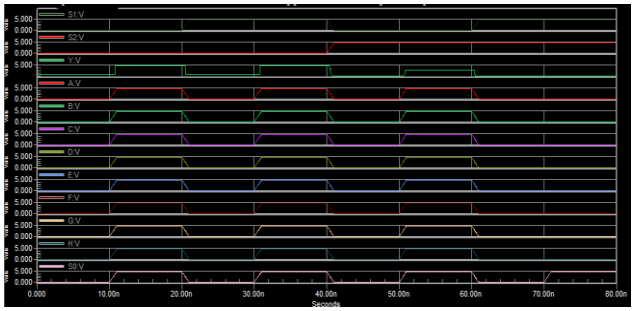

Figure 11.ECRL 8*1 Multiplexer Output Waveform

Depending on the selection bits, a particular input is selected from one of the 8 inputs and the outputs for ECRL 8*1 Mux is based according to the required selection inputs. The outputs are complementary.

*C. 2N2N2P (8*1 Multiplexer):*

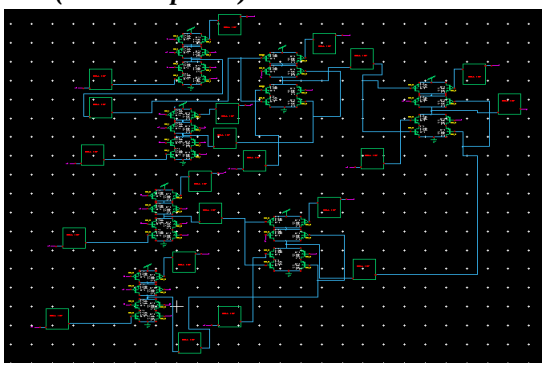

Figure 12.2N2N2P 8*1 Multiplexer Schematic Design

In the 2N2N2P Schematic as shown in Figure.12; here the NMOS logic block is used instead of n-tree and is placed parallel to the Pull-down NMOS transistors as shown in Figure.3. The outputs are complementary.

Upon simulation, the output waveform for the 2N2N2P Schematic is given in Figure.13.

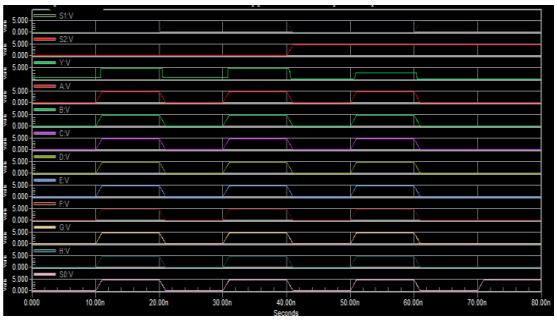

Figure 13.2N2N2P 8*1 Multiplexer Output Waveform

Depending on the selection input bit combination of 2N2N2P 8*1 MUX, the output is evaluated.

*D. PFAL (8*1 Multiplexer):*

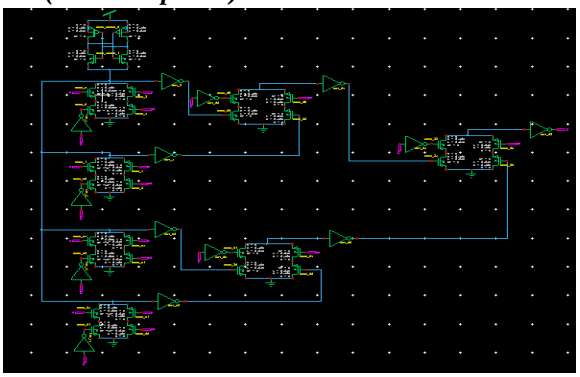

Figure 14.PFAL 8*1 Multiplexer Schematic Design

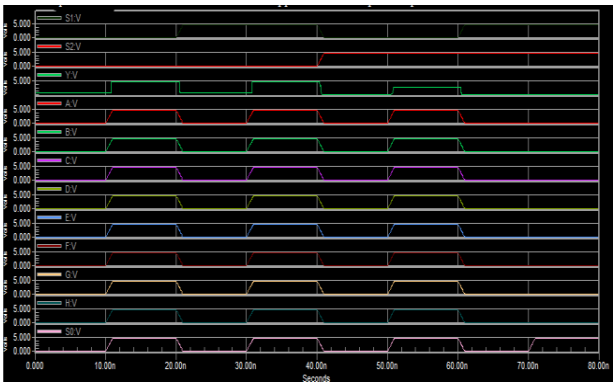

Figure 15.PFAL 8*1 Multiplexer Output Waveform

Upon simulation, the output waveform for PFAL is obtained according to selection bit inputs.

*E. PROPOSED LOGIC CIRCUIT (8*1 Multiplexer):*

The proposed logic is very much similar to CMOS circuit except the proposed logic uses two extra transistors, one PMOS above the pull-up and one NMOS below the pull-down where both the gate and drain are shorted in both pull-up and pull-down devices as shown in Figure.7. Hence, both the devices operate in saturation region. The outputs are not complementary [16]. The Schematic of proposed logic circuit is given in Figure.16.

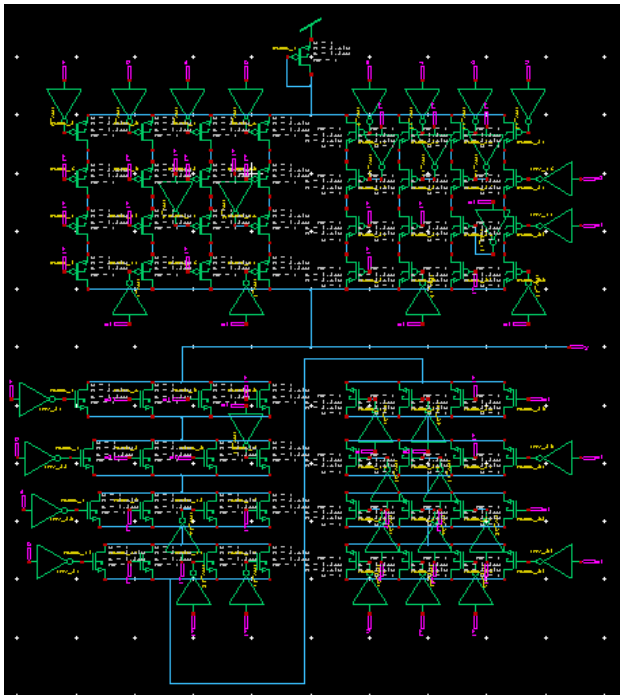

Figure 16.Proposed Logic 8*1 Multiplexer Schematic Design

Based on the simulation, the output waveform for the Proposed Logic Schematic circuit design is shown in Figure.17.

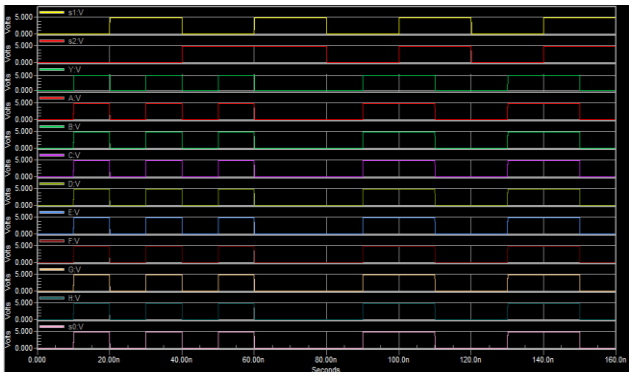

Figure 17.Proposed Logic 8*1 Multiplexer Output Waveform

The outputs for the Proposed Logic are obtained regarding the selection bit inputs.

*F. Standard CMOS (1*8 Demultiplexer):*

The schematic design of Standard Complementary MOS circuit for 1*8 Demultiplexer is given in Figure.18.

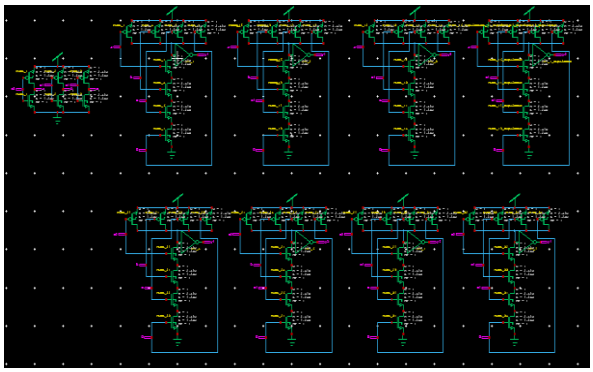

Figure 18.CMOS 1*8 Demultiplexer Schematic Design

Upon simulation, the output waveform obtained for the CMOS Demux circuit is given in Figure.19.

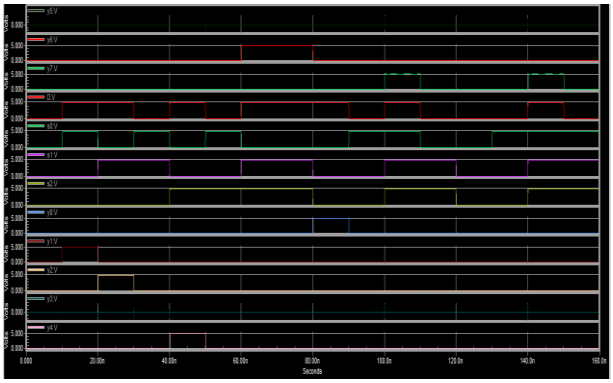

Figure 19.CMOS 1*8 Demultiplexer Output Waveform

*G. ECRL (1*8 DeMultiplexer):*

The schematic design of ECRL circuit for 1*8 Demultiplexer is given in Figure.20.

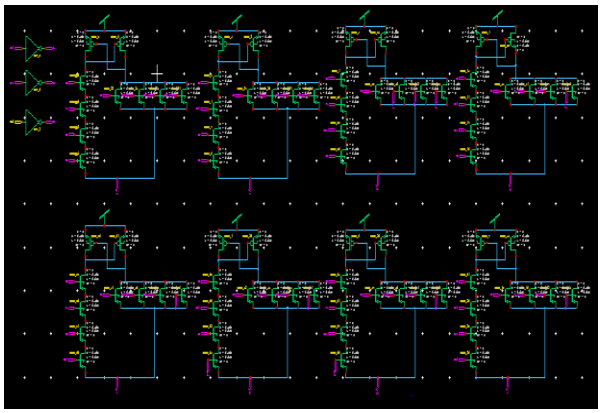

Figure 20.ECRL 1*8 Demultiplexer Schematic Design

Upon simulation, the output waveform obtained for ECRL Demux circuit is given in Figure.21.

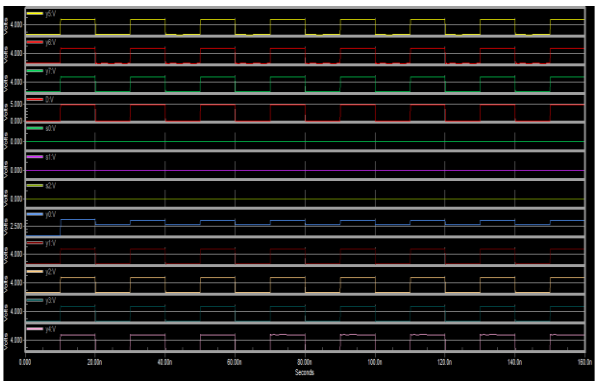

Figure 21.ECRL 1*8 Demultiplexer Output Waveform

After the simulation, the outputs for ECRL are obtained according to the selection bit inputs.

*H. 2N2N2P (1*8 DeMultiplexer):*

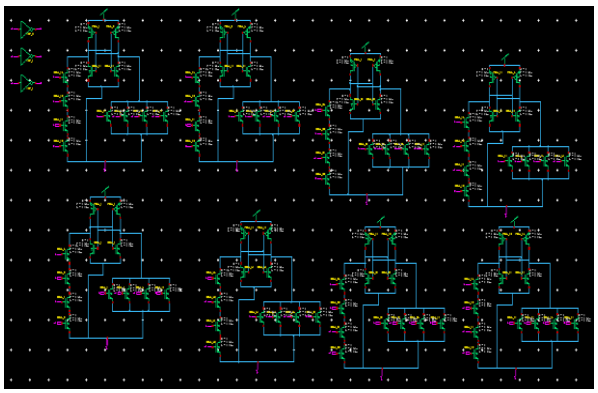

Figure 22.2N2N2P 1*8 Demultiplexer Schematic Design

In the 2N2N2P Schematic as shown in Figure.22, here the NMOS logic block is used instead of both n-tree (F and $\overline{F}$) and is placed parallel to the Pull-down NMOS transistors as shown in Figure.3. The outputs are complementary.

Upon simulation, the output waveform obtained for 2N2N2P Demux circuit is given in Figure.23.

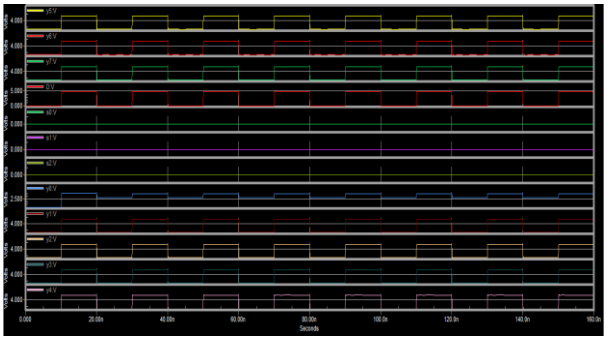

Figure 23.2N2N2P 1*8 Demultiplexer Output Waveform

*I. PFAL (1*8 DeMultiplexer):*

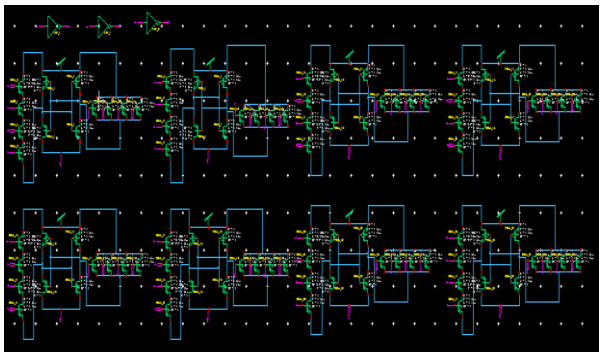

Figure 24.PFAL 1*8 Demultiplexer Schematic Design

In the PFAL schematic as shown in Figure.24; the two cross-coupled CMOS inverters are connected back to back and the NMOS logic block is used instead of n-tree for both (F and $\bar{F}$) and is kept parallel to the PMOS logic blocks. The outputs are complementary.

Upon simulation, the output waveform obtained for PFAL Demux circuit is given in Figure.25.

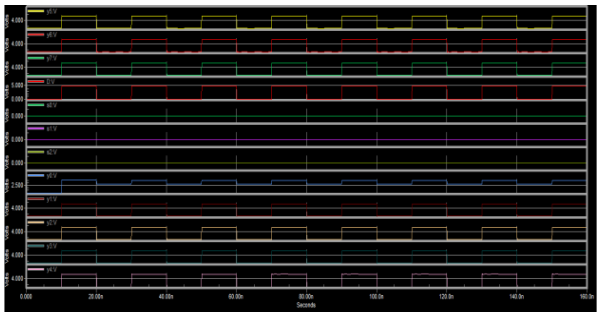

Figure 25.PFAL 1*8 Demultiplexer Output Waveform

*J. PROPOSED LOGIC CIRCUIT (1*8 DeMultiplexer):*

The schematic design of Proposed Logic circuit for 1*8 Demultiplexer is given in Figure.26.

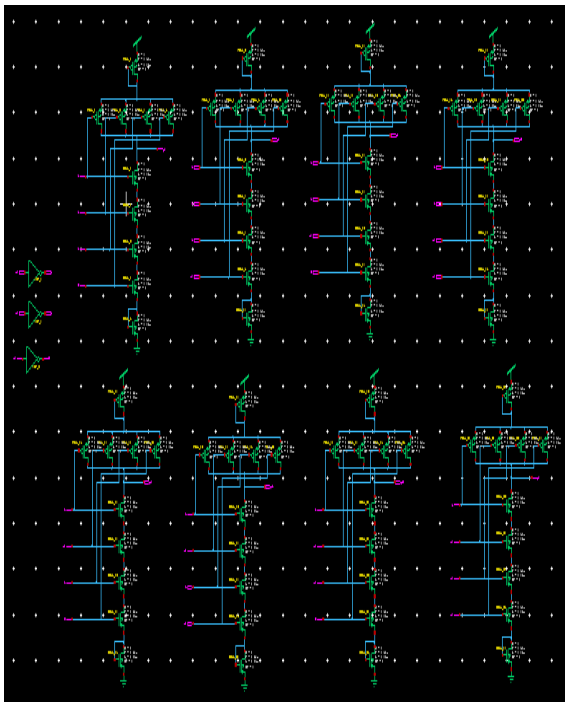

Figure 26.Proposed Logic Circuit 1*8 Demultiplexer Schematic Design

Upon simulation, the output waveform obtained for PFAL Demux circuit is given in Figure.27.

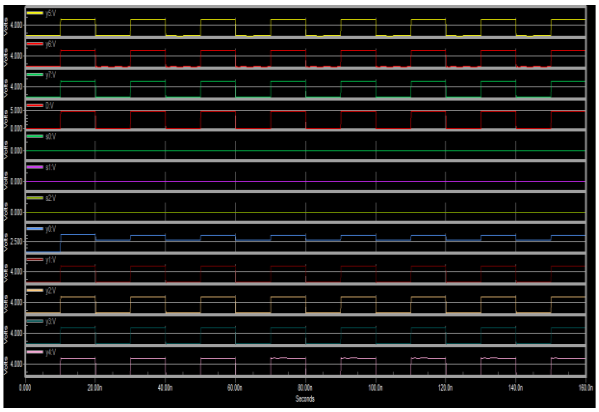

Figure 27.Proposed Logic Circuit 1*8 Demultiplexer Output Waveform

VII. POWER CONSUMPTION ANALYSIS AND COMPARISON

All the schematic designs of proposed logic design and standard adiabatic logic styles like ECRL, 2N2N2P, PFAL and CMOS logic style for both the Multiplexer and Demultiplexer are done using TANNER EDA TOOL V15.0 and the simulations are done using T-SPICE. Their power consumption outputs are carried out at 250nm technology with W =2.5u and L =250n, and the DC supply voltage, V_{DD} = 5v.

*A. 8*1 Multiplexer:*

Table III & IV shows the performance of the Multiplexer for the Proposed Logic over the Standard adiabatic logic styles in terms of Transistor count, Area per chip, Delay and most significantly the Power Dissipations as well as it presents the percentage of Power Saving of the Proposed Logic with respect to the standard adiabatic logic styles.

TABLE III. PERFORMANCE ANALYSIS OF VARIOUS LOGIC STYLES FOR 8*1 MULTIPLEXER AT 250nm TECHNOLOGY

Parameter	Logic Styles				
	CMOS	ECRL	2N2N2P	PFAL	PROPOSED
Transistor Count	77	64	56	46	75
Area Per Chip(μm^2)	19.25	16	14	11.5	18.75
Delay (ns)	79.11	52.72	64.54	69.42	49
Total Power Dissipation (μW)	0.412	0.140	0.171	0.121	0.012

TABLE IV. PERCENTAGE POWER SAVING OF PROPOSED LOGIC WITH RESPECT TO STANDARD LOGIC STYLES FOR 8*1 MULTIPLEXER

LOGIC STYLES	CMOS	ECRL	2N2N2P	PFAL
% OF POWER SAVING	97.04%	91.34%	92.8%	89.9%

From the Tables III & IV, it can be inferred that the proposed logic for the multiplexer shows the least power dissipation and delay when compared to adiabatic logic styles and standard CMOS style. The percentage power savings of 89.9% over PFAL, 91.34% over ECRL, 92.8% over 2N2N2P and 97.04% over CMOS shows significant improvement over the standard logic styles. For a system comprising of many such multiplexers, the power saving will be large and the efficiency of the circuit will be high because of the reduction in delay.

*B. 1*8 Demultiplexer:*

Similarly, for the Demultiplexer, the Tables V & VI shows the performance analysis and percentage power savings of the Proposed Logic with respect to the standard adiabatic logic styles.

TABLE V. PERFORMANCE ANALYSIS OF VARIOUS LOGIC STYLES FOR 1*8 DEMULTIPLEXER AT 250nm TECHNOLOGY

Parameter	Logic Styles				
	CMOS	ECRL	2N2N2P	PFAL	PROPOSED
Transistor Count	78	83	99	99	83
Area Per Chip(μm^2)	19.5	20.75	24.75	24.75	20.75
Delay (ns)	65.37	40.29	58.96	55.25	35.45
Total Power Dissipation (μW)	0.346	0.370	0.3895	0.3397	0.077

TABLE VI. PERCENTAGE POWER SAVING OF PROPOSED LOGIC WITH RESPECT TO STANDARD LOGIC STYLES FOR 1*8 DEMULTIPLEXER

LOGIC STYLES	CMOS	ECRL	2N2N2P	PFAL
% OF POWER SAVING	77.74%	79.18%	80.2%	77.33%

From the Tables V & VI, it can be clearly observed that the proposed logic for the Demultiplexer shows the least power dissipation and delay when compared to adiabatic logic styles and standard CMOS style. The percentage power savings of 77.33% over PFAL, 77.74% over CMOS, 79.18% over ECRL and 80.2% over 2N2N2P indicates its superiority over the standard logic styles. For a system comprising of many such demultiplexers, the power saving will be enormous and gives high efficiency over speed.

VIII. CONCLUSION

Adiabatic logic is an efficient technique for designing low power circuits compared to standard CMOS logic. Simulation indicates it is a power saving logic. From the analysis we can conclude that the logics for the Multiplexer and the Demultiplexer over the proposed logic show the least power dissipation and highest efficiency in speed with reduction in delay parameter when compared to adiabatic logic styles and standard CMOS style. The future scope of this work is that multiplexers and demultiplexers with highest number of input and output lines can be constructed by cascading the proposed ones.

ACKNOWLEDGEMENT

I would like to express my gratitude to **Prof. P.V.SRIDEVI**M.E.,Ph.D., Professor, Department of Electronics and Communication Engineering, for her invaluable guidance, advice and supporting me in successfully doing this project.

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