Low Power and Low Leakage based Ternary Half Adder using FinFET Technology

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Abstract - In this paper, we study and simulate low power low leakage based ternary half adder using FinFET technology. The great challenge in the nanometer regime is due to Short Channel Effects that cause an exponential increase in the leakage current. With the advancement in technology, Conventional CMOS has Short Channel Effects. In order to reduce the Short Channel Effects, FinFET is used. FinFETs are the new emerging transistors that can work in the nanometer range to overcome these Short Channel Effects. Due to the recent technology trends all the electronic markets are based on reliable and speed performance devices. By developing semiconductor industry, all the passive and active components are assembled on a single chip named as an Integrated chip (IC). Developing this type of technology made all the electronic devices becomes smarter and reliable in performance. It shows improvement in Average Power, Leakage and PDP.

Keywords **-** FinFET, Ternary Half Adder, Ternary Logic, HSPICE, 32nm

I. INTRODUCTION

As indicated by Moore's law the elements of individual devices in a coordinated circuit have been diminished by a factor of around two at regular intervals. This downsizing of devices has been the main impetus in innovative advances since the late twentieth century. In any case, as substantiated by ITRS 2009 release, further downsizing has confronted genuine limits identified with manufacture innovation and device exhibitions as the basic measurement contracted down to sub-22 nm range. [7] The points of confinement include electron burrowing through short channels and slight protector films, the related leakage currents, aloof power dissipation, short channel effects, and varieties in device structure and doping. These breaking points can be defeated to some degree and encourage further downsizing of device measurements by altering the channel material in the conventional mass MOSFET structure with a solitary carbon nanotube or a variety of carbon nanotubes. [6][5] Electronic device, innovation and circuit specialists are investigating conceivable options for the fate of semiconductor industry to improve execution of electronic framework. [4] Research is being completed in growing high-portability transistor channel materials, for example, III-V compound semiconductors, stressing the channel material to improve bearer versatility just as in utilizing non-planar transistor structures in particular CNTFETs and multigate structures. [1][2]All the while, novel one-dimensional structures e.g., nanowires and carbon nanotubes (CNTs) are additionally being effectively inquired about. CNTs, with their predominant transporter portability, have developed as a potential possibility to help the Si innovation guide in a post 2015-time allotment, albeit various difficulties remain. Subsequently, carbon nanotube field-effect transistors (CNTFETs) give chance to look into at both device and circuit levels. [3]

In 1989, a twofold gate SOI structure was manufactured which they called a completely double gate FET. This was the primary revealed creation of a FinFET-like structure. FinFETs have pulled in expanding consideration over the previous decade in light of the debasing short-channel conduct of planar MOSFETs. Figure 1 shows the better short-channel execution of FinFETs over planar MOSFETs with a similar channel length. Figure 2 demonstrates a regular planar a FinFET. While the planar MOSFET channel is level, the FinFET channel (otherwise called the fin) is vertical. Thus, the stature of the channel (*H*FIN) decides the width (*W*) of the FinFET. This prompts an exceptional property of FinFETs known as width quantization. This property says that the FinFET width must be a various of *H*FIN, that is, widths can be expanded by utilizing different fins. Accordingly, self-assertive FinFET widths are impractical. Albeit littler fin statures offer greater adaptability, they lead to different fins, which thus prompts more silicon zone. Then again, taller fins lead to less silicon impression, yet may likewise result in basic insecurity. [8]

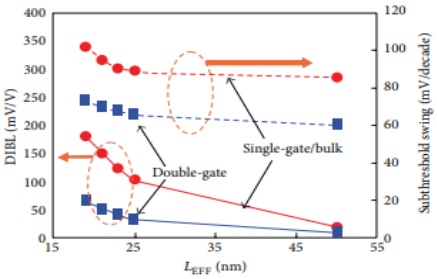

Figure 1: DIBL in DG and Bulk Transistors

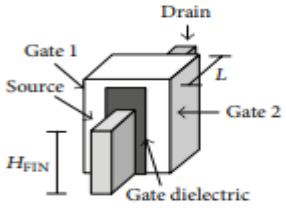

Figure 2: FinFET

SG FinFETs can be additionally classified dependent on asymmetries in their gadget parameters. Ordinarily, the work capacities (Φ) of both the front and back gates of a FinFET are the equivalent. Be that as it may, the work capacities can likewise be made extraordinary. This prompts a lopsided gate work SG FinFET or ASG FinFET (Figure 6) [86, 87]. ASG FinFETs can be created with particular doping of the two gate-stacks. They have promising short-channel qualities and have two requests of extent lower *I*off contrasted with that of a SG FinFET, with *I*on just to some degree lower than that of a SG FinFET [49]. Figures 7 and 8 show correlations of the drain current *I*DS versus front-gate voltage *V*GFS bends for SG, IG, and ASG nFinFETs and pFinFETs, separately, exhibiting the benefits of ASG FinFETs. In this work we have used SG type FinFET. [9][10]

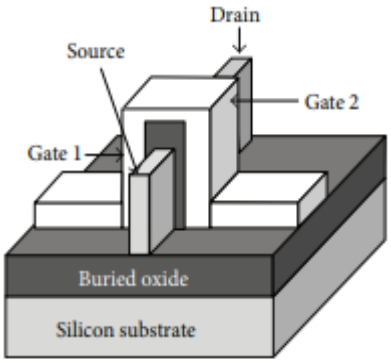

Figure 3: SOI FinFETs

II. IMPLEMENTATIONS

In this section, implementation is mentioned, Software used is HSPICE and technology node is 32nm.

Ternary adder using FinFET:

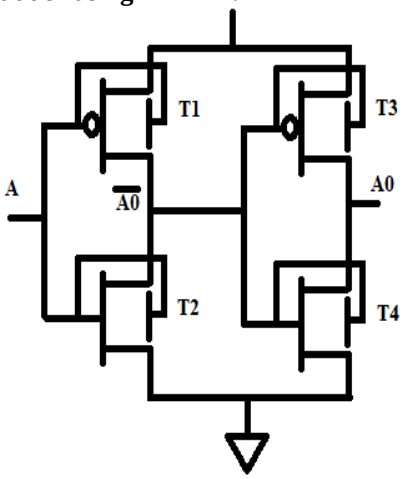

Figure 4: Decoder circuit using FinFET

The above figure shows the decoder circuit using FinFET, Here A is the input of the decoder and A0 is the output of the decoder circuit these circuit is used to generating A0 and A0 bar.

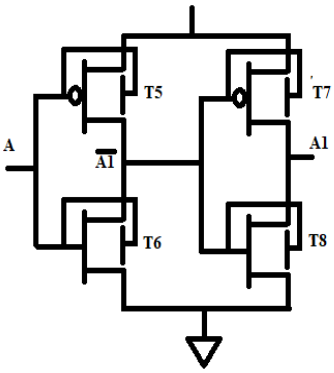

Figure 5: Decoder circuit using FinFET

The figure 5 shows the same decoder circuit we are seen in figure 4, here we are using this circuit for generating A1 and A1bar.

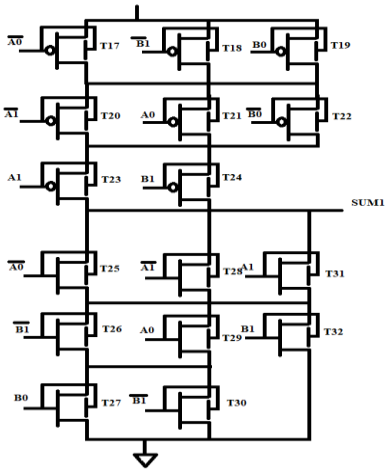

Figure 6: Circuits for Sum Generator Sum1

The above figure shows the circuit for sum generator, here we are implementing sum1, the output of the circuit is binary form.

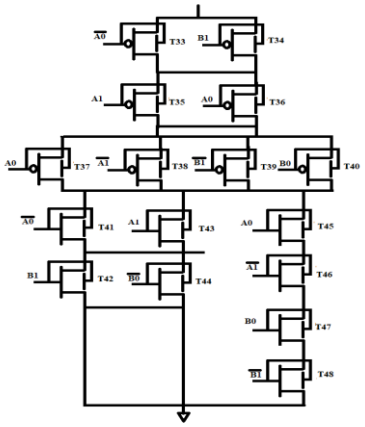

Figure 7: Circuits for Sum Generator Sum2

The figure 7 shows the sum generator, here we are implementing sum2, here we are getting a binary output

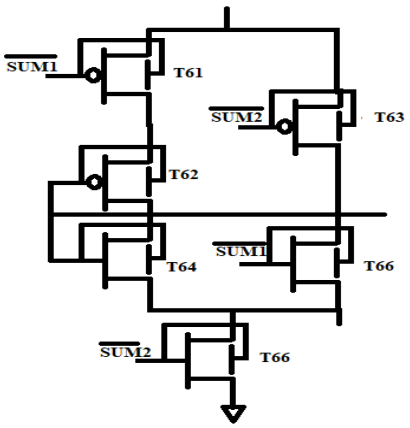

Figure 8: Circuits for Sum Generator encoder

The figure 8 shows the circuit for sum generator encoder, the encoder output is total sum of sum1 and sum2, here finally getting the ternary output

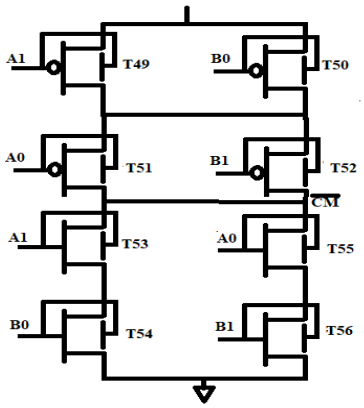

Figure 9: Circuits for carry generator Cm

The figure 9 shows the circuit for carry generator Cm, here we are using the p channel FinFET and n channel FinFET

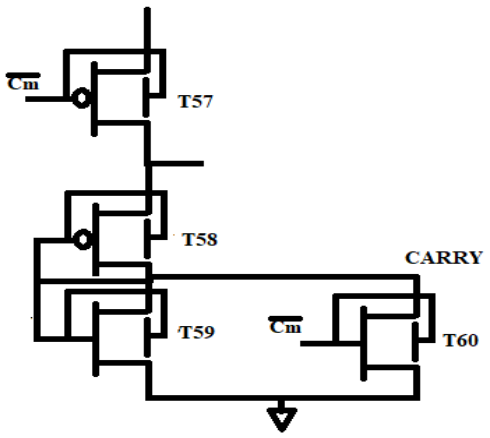

Figure 10: Circuits for carry generator carry

The above figure shows the carry generator circuit, the carry is obtained from Cm using the carry encoder circuit given in Figure 10

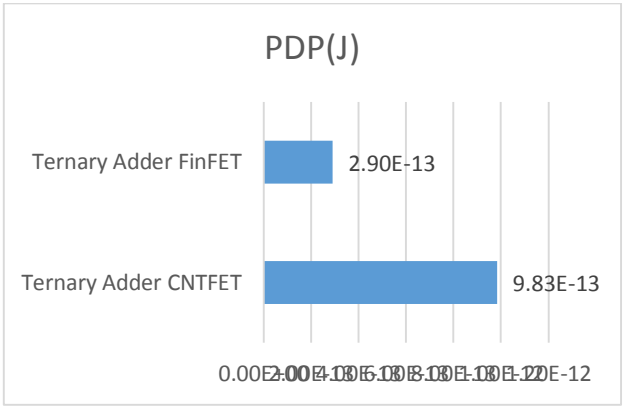

Figure 11: PDP of proposed system

The figure 11 shows the PDP of proposed system. here comparing the ternary adder CNTFET and ternary adder FinFET, here the PDP is the high in ternary adder CNTFET compare to ternary adder FinFET

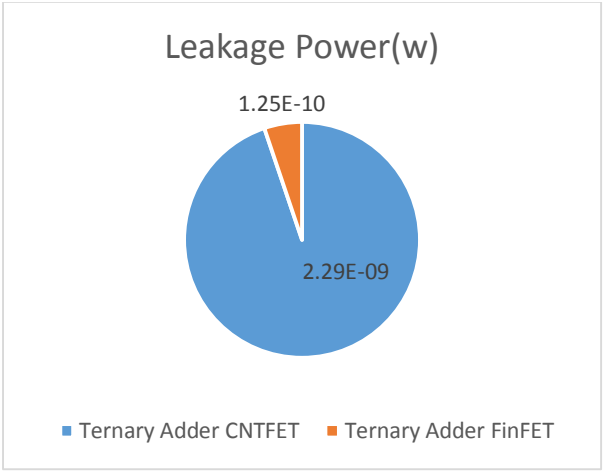

Figure 12: leakage power of proposed system

The figure 12 shows the leakage power of proposed system, here the leakage delay is high in ternary adder CNTFET

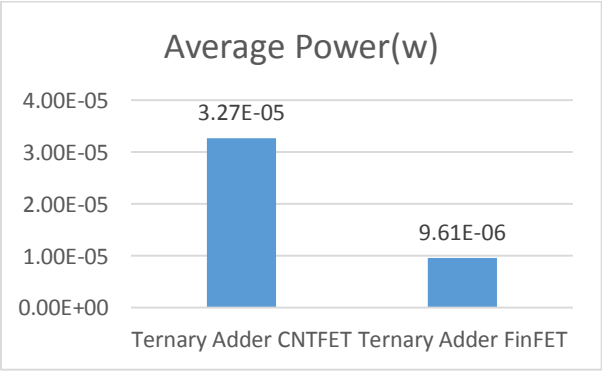

Figure 13: average power of proposed system

The average power of proposed system, the average delay is high in ternary adder CNTFET more than ternary adder FinFET

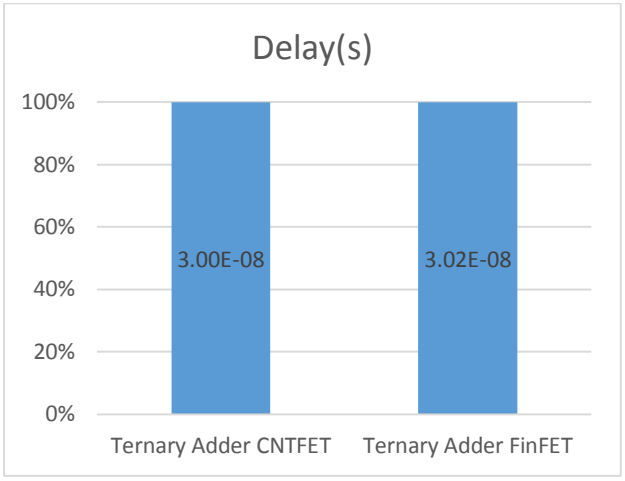

Figure 14: Delay of proposed system

The above figure shows the delay of proposed system

Table 1: simulation result

	Ternary Adder CNTFET	Ternary Adder FinFET
Average Power(w)	3.27E-05	9.61E-06
Delay(s)	3.00E-08	3.02E-08
PDP(J)	9.83E-13	2.90E-13
Leakage Power(w)	2.29E-09	1.25E-10

The above table shows the different parameter comparison in ternary adder CNTFET and ternary adder FinFET

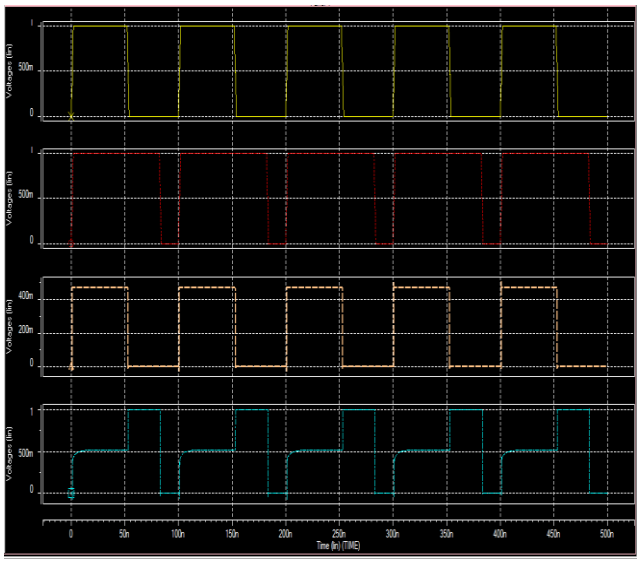

Figure 15: Waveform of FinFET based Ternary Adder

The above figure shows the waveform of FinFET ternary Adder

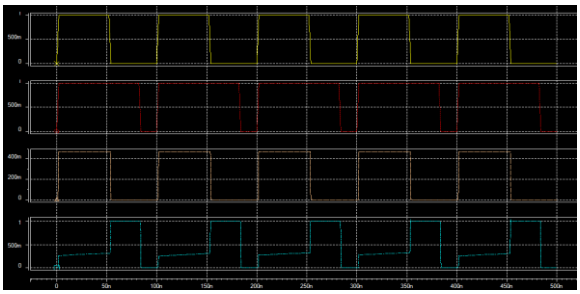

Figure 16: Waveform of FinFET based Ternary Adder

The figure 16 shows the waveform of FinFET ternary Adder

III. CONCLUSION

Hence we are studied low power low leakage based ternary half adder using FinFET technology, here we are using different technology mainly FinFET technology, in this technology used to improving the average power, delay, PDP, leakage power of ternary adder FinFET. In results section we can see we are comparing the ternary adder CNTFET and ternary adder FinFET and we are using different circuits.

IV. REFERENCES

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