A Review on Low Power Double Tail Comparator in VLSI Technology

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Abstract **-** In this review paper we study Low Power Double Tail Comparator. the need for low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. High speed dynamic regenerative comparators are used in low power and area efficient analog to digital converters to improve speed and power efficiency. Speed and power consumption are the two factors that define the comparators accuracy. This provides faster, more efficient modification of the comparator design. This further reduces the power consumption and provides higher speed by reducing the delay time of the circuit.

Keywords **-** A nalog to digital. Speed and efficiency, tail comparator, digital converters, accuracy, power consumption

I. INTRODUCTION

In modern life, electronic equipment is frequently used in all fields such as communication, transportation, entertainment, medical, household etc. The requirement of analog to digital converters is increasing day by day as they play a major role in converting the analog signals to digital ones. ADCs act as interface between the natural analog world and the real time digital world [1]. Comparator is the fundamental block which acts as heart of the ADC. In general, a comparator is defined as an electronic device which compares the given analog input signal with reference voltage and produces a digital output i.e, either logic '0' or logic '1'. If the input to the non-inverting input is greater than that to the inverting input, the output is a logical 1. If the input to the non-inverting input is less than that to the inverting input, the output is a logical 0[2].

One of the most important basic building blocks in analog and mixed-mode circuits is the comparator. The function of a CMOS comparator is to compare an input signal with a reference signal and produce a binary signal output. Comparator uses back to back cross coupled inverters to convert the voltage into digital output in a short period of time. The performance of the comparator plays an important role in realization of high integration, low power, low cost and good design [3].

II. LITERATURE REVIEW

A low-offset, low-power consumption, small area comparator is a very important circuit block for many applications, such as memory sensing circuits, analog to digital converters. (ADC), and so on. Therefore, offset voltage cancellation or calibration techniques are vital for realizing a low offset voltage comparator. In conventional designs, preamplifiers were used for offset voltage cancellation [1]. However, it increases power consumption because wide bandwidth amplifiers are required to reduce the offset voltage in the high frequency. A dynamic latched comparator shows higher load drivability than the conventional dynamic latched comparator. The addition of two inverters between the input and output stage of the conventional double-tail dynamic comparator, the regenerative latch stage was improved. Clocked regenerative comparators are fundamental circuit blocks, which are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback [2]. The need for ultra-low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In the base paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the trade-offs in dynamic comparator design [3]. Comparator is one of the fundamental building blocks in most of the analog-to-digital converters (ADCs). Many of the highspeed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep sub-micrometres (UDSM) CMOS technologies suffer from very low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [4].

III. COMPARATOR

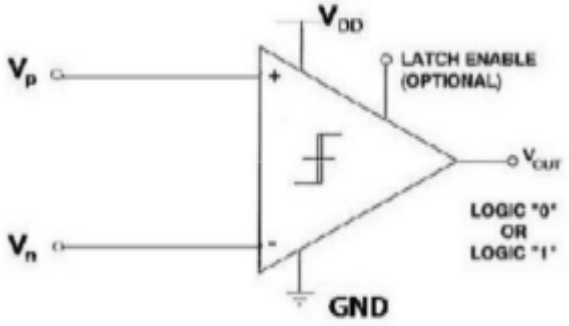

Figure 1: Schematic of Comparator

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison. Vp is the input voltage (pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator [4]. Designing high-speed comparators is more challenging when the supply voltage becomes smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate for the reduced supply voltage. It also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as Flash ADCs [5]. The performance of high speed analog to digital converters (ADCs) basically depends on the comparator. The conversion from analog to digital form mostly involves comparator action where the value of analog voltage at some point in time is compared with some standard value. The input to the ADC is a voltage. In ADC the input signal is converted into the digital signal in the form of binary [6]. Comparator compares two currents or voltages and based on the comparison produces the digital output. The basic function of a CMOS comparator compares a input signal with the reference signal and generates the output accordingly. A comparator consists of a high gain differential amplifier. Comparator is one of the building blocks in most of the analog-to-digital converters without which the process of data conversion cannot take place. In general comparators are very fast. Many high-speed ADCs, such as flash ADCs, require high-speed, low-power comparator [7]. There are three main stages in a comparator; the first stage is the pre-amplifier stage. In this stage the input signal which is fed to the comparator is being amplified. The second stage is a positive feedback stage. This is mainly used to identify the input signal which is high or low. The final stage is the decision-making stage and an output buffer stage. Here the main purpose of buffer is to amplify the information which is obtained and produce a digital signal as its output. Designing a comparator is done by considering input common mode range, power dissipation, propagation delay and area of the entire chip [8]. comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many highspeed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep submicrometric (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [9]

A. Conventional dynamic comparator -

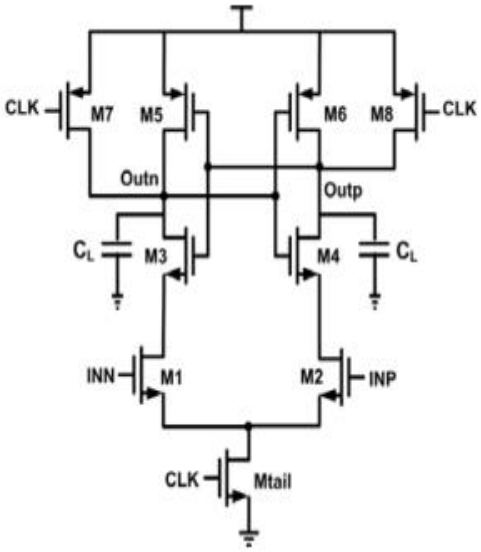

Figure 2: Schematic diagram of the conventional dynamic comparator.

A comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator [9]. The need for ultra-low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the trade-offs in dynamic comparator design. Based on the presented analysis, where the circuit of a conventional doubletail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time [10]. High input impedance is the main advantage of Single tail structure, no static power consumption, rail to rail output swing and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of the input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is that due to several stacked transistors, the delay time of the latch consumes

very high supply voltage. Beside this another disadvantage of this structure is that there is only one path for current through tail transistor Mtail, which defines the current for both the latch (the cross-coupled inverters) and the differential amplifier. Due to this there is some delay in the passage current from one node to ground or from one latch to another latch [8].

B. Conventional Double- Tail Dynamic Comparator - The schematic of conventional double tail comparator is shown in the figure 3. This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

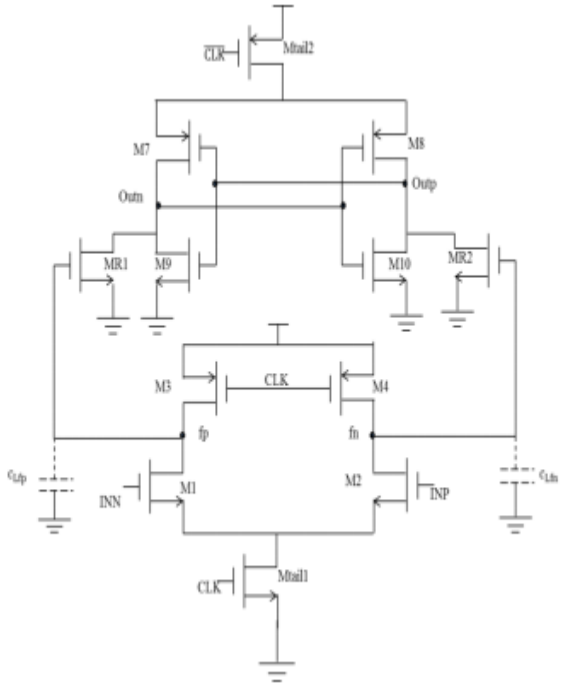

Figure 3: Schematic diagram of the conventional double-tail dynamic comparator

The operation of this comparator is given below. During reset phase (CLK=0, Mtai 1l *and* Mtail 2 turn off), transistors M3 − M4 pre-charge nodes fn and fp to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During the decision making phase (CLK=VDD, Mtai 1l *and* Mtail 2 are turn on), M3 − M4 are turn off and the voltages at the node fn and fp start to drop with the rate defined by IMtail /Cfn(p) and on top of this an input dependent differential voltage ΔVf n(p) will build up. The intermediate stage formed by MR1 and MR2 passes ΔVf n(p) to the cross coupled inverters and also provides a good shielding input and output.[6].Double tail comparator is clocked regenerative comparators. Clocked regenerative comparators have found many applications in many high-speed ADCs since they can make fast operations because of its strong positive feedback in the regenerative latch. For its best performance in low voltage application the various comparators are designed based on the double-tail structure. The designing of double tail comparator has dual input, dual output inverter stage that is suitable for high speed analog-to-digital converters. The double tail comparator also has low voltage and low power. In this technique, the voltage difference between the output nodes is increased for increasing the latch regeneration speed. For maintaining the high speed of proposed comparator, the main idea is to increase ΔVann/fp [8].

IV. CONCLUSION

The Low Power Double Tail Comparator having many advantages. The topology designed has less stacking, so it can operate at lower voltages compared to the single tail transistor. The double tail enables both a large current and smaller current in the latching stage for fast operation and input stage for lower offset respectively. Compared to other comparator it is found that shorter the propagation delay, higher the speed of circuit and vice versa.

V. REFERENCES

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