

# Review Paper on Serial Communication Inter-IC Protocol

Madhuri Daware, Prof. A. S. Patil

*Padmabhooshan Vasantdada Patil Institute of Technology, Pune, MS-India*

**Abstract** - In the world of multiple application based product it is very much a mandatory to have multiple devices connected to a system, this includes peripherals following different communication protocols as well. These requirements give rise to the need for an intermediate system which can act as a bridge between 2 devices following different communication protocols. This is where I<sup>2</sup>C master controller design is very useful. Today a system is connected to a number of devices and makes the communication smooth and fast, I<sup>2</sup>C protocol is considered as one of the very best. The EEPROM, ADC and RTC will require an interface for communication between them. So I<sup>2</sup>C bus is used as an interface between them. It is used to minimize system-level interconnect. Embedded system mainly uses serial communication to communicate with peripherals. Therefore serial communication plays vital role in embedded system design. Many serial communication protocols are used like Universal Asynchronous Receiver Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI) and Inter IC Protocol (I<sup>2</sup>C). Inter IC protocol satisfy the requirement of embedded system of less number of wires for interconnection. Implementation of inter IC protocol on FPGA gives flexibility to use it according to application. This paper provides reviews use of I<sup>2</sup>C protocol with FPGA implementation.

**Keywords** - Inter-IC (I<sup>2</sup>C), SCL, SDA, FPGA.

## I. INTRODUCTION

The I<sup>2</sup>C bus was developed in 1982; its original purpose was to provide an easy way to connect a CPU to peripheral chips in a TV set. Peripheral devices in embedded systems are often connected to the microcontroller as memory-mapped I/O devices. One common way to do this is connecting the peripherals to the microcontroller parallel address and data busses. This results in lots of wiring on the PCB (printed circuit board) and additional 'glue logic' to decode the address bus on which all the peripherals are connected. In order to spare microcontroller pins, additional logic and make the PCBs, invented the 'Inter-Integrated Circuit', I<sup>2</sup>C or I<sup>2</sup>C protocol that only requires 2 wires for connecting all the peripheral to a microcontroller.

## II. INTER-IC PROTOCOL

There are different types of serial communication protocols are present like Universal Asynchronous Receiver

Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I<sup>2</sup>C). Each protocol has certain advantage and disadvantage depends on application. SPI and UARTs can communicate from one point to another point only. USB use multiplexing technique to communicate multiple devices while CAN and I<sup>2</sup>C useful for software addressing of receiver. CAN and SPI protocol are beneficial protocol in communication but CAN is complex to design and have limited portfolio so it is not used in general communication. If we consider SPI protocol which has advantages of low cost small and easy to design but if peripheral increases the number of interconnects also increases. Hence not useful for communication purpose where peripherals are more.

I<sup>2</sup>C is protocol is two wire bus protocol SDA (serial data) and SCL (serial clock). Each device is recognized by a unique address, and can operate either as a transmitter or as a receiver. The I<sup>2</sup>C master is the device that initiates a transfer and generates the clock for the same. Any device addressed by the master is the slave. Each device can act as transmitter or receiver depending on its nature. The I<sup>2</sup>C bus is a multi-master bus. This means that more than one IC capable of initiating a data transfer on the bus is considered to it. I<sup>2</sup>C provides low cost and efficient link between ICs. It is synchronous protocol in which master initiate data communication and data get exchanged between master and slave. All communication is control by master using SCL line. All slave connected with SCL line. Slaves are controlled by same SCL line.

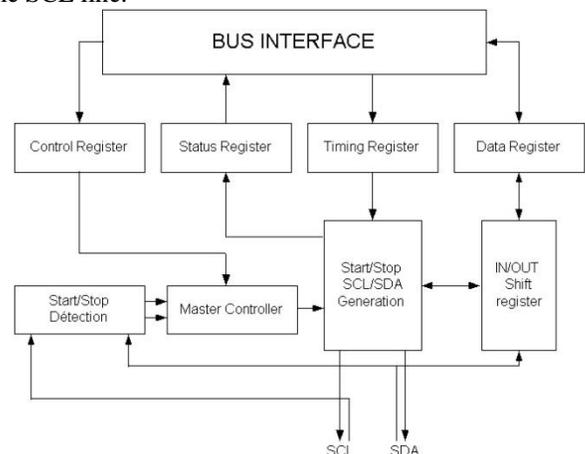


Fig.1: Block diagram of I<sup>2</sup>C Bus Interface

### Components of I2C

Figure 1 illustrates the block diagram of I2C bus interface. I<sup>2</sup>C master comprises of control register, timing register, status register, data register. Data comes initially into status register and depending upon it the command register issues the commands. Data register decide whether to transmit or receive the data and this data is transmitted parallel to data I/O register. I<sup>2</sup>C Master Byte Controller is the byte command controller and data I/O shift register. The byte command controller is the heart of I<sup>2</sup>C communication traffic at the byte level and is a state machine that generates different states of I<sup>2</sup>C byte operations based on the command register bits. The data I/O shift register is a component which contains and deals with the data associated with the present I<sup>2</sup>C write and read transactions. I<sup>2</sup>C Master bit controller involves clock generator and a bit command controller. During transmission data is shifted bit by bit into the command bit controller and from there it is transferred onto SDA. During reception data comes on SDA and then to bit controller.

### III. IMPLEMENTATION OF I2C

Many researchers proposed different model to implement inter IC protocol which helps to control various applications. Some of the models are summerised below:

Some researcher implemented serial data communication using I2C (Inter-Integrated Circuit) master bus controller using a field programmable gate array (FPGA). The I2C master bus controller was interfaced with MAXIM DS1307, which act as a slave. This module was designed in Verilog HDL and simulated in Modelsim 10.1c. The design was synthesized using Xilinx ISE Design Suite 14.2. [1]

Sahu *et al.* developed inter IC protocol for data surveillance purpose. Data surveillance is very important application to monitor people or sensors. I2C is used for data surveillance because it could make system efficient, accurate, flexibility, and low development cost. They designed a protocol in VHDL and interface with OV7620 single chip CMOS VGA color digital camera. Data surveillance includes monitoring people or collection of sensors information from various nodes. They developed system which will replace traditional cameras with LAN cameras with complex image processing and IP routing. Data compression takes place with H.263 algorithm due to its high compression efficiency and high data rate. For surveillance constant bit rate limit the real time communication of cameras so variable bit rate is used. Variable bit rate efficiently uses available bandwidth. H.263 encoding is very complex normal DSP processor cannot handle it so FPGA as programmable solution is used. All results were verified using Modelsim and FPGA can be used as interface in between camera and local monitor system. [5]

Some researchers developed Inter-IC protocol with volume controller application. WM 8731 sound driver was used in

MP3 audio or speech players. The designed interface was used to control features like volume control, mutes and power management. For designed purpose state machine model approach was used because it keeps track of operation from one state to another. A main tool used to design protocol was VHDL and Verilog. Assignment of pins can be done with assignment editor. Joint test action group (JTAG) programming was used and for simulation results validated using Modelsim- Altera 6.5b (Quartus II 9.1). [3]

Some researchers implemented serial communication protocol SPI (Serial Peripheral Interface) on FPGA. In the world of communication protocols, SPI is often considered as “little” communication protocol compared to Ethernet, USB, PCI-Express and others that present throughput in the ×100 Mb/s range, if not Gb/s. Ethernet, USB meant for “outside the box communications” and data exchanges between whole systems. While SPI, as well as others serial protocols such as I2C and 1-wire for instance, are well suited for communications between integrated circuits for low/medium data transfer speed with on-board peripherals. Here, sensor interfaced with the FPGA via ADC & result is displayed on LCD display. The temperature sensor LM 35 is used for sensing the temperature between -55 to 150oC. The MCP 3201 is used for analog to digital conversion of sensor output. MCP 3201 is 2.7v, 12 bit A/D converter with SPI serial interface. SPI protocol is used for data transfer from slave to master. Here sensor circuit is used as slave which transferring data to the SPI master. Both these slave & master is coded in VHDL. [6]

### IV. PROPOSED SYSTEM

In this paper implementing I2C bus protocol for interfacing low speed peripheral devices on FPGA. It is also the best bus for the control applications, where devices may have to be added or removed from the system. I2C protocol can also be used for communication between multiple circuit boards in equipments with or without using a shielded cable depending on the distance and speed of data transfer. I2C bus is a medium for communication where master controller is used to send and receive data to and from the slave devices. I2C master controller is designed using VHDL based on Finite State Machine (FSM). FSM is a sequential circuit that uses a finite number of states to keep track of its history of operations, and based on history of operation and current input, determines the next state. There are several states in obtaining the result. Figure 2 shows block diagram of proposed system interfacing low speed peripherals RTC (DS1302) and EEPROM with I2C master bus controller and implement on Cyclone IV FPGA with the help of Nios-II Softcore Processor.

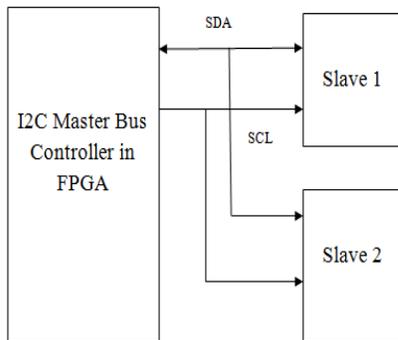


Fig.2: Block Diagram of Proposed System

#### V. ADVANTAGES OF I<sup>2</sup>C

- Used for security sensitive applications like sensor connections, RFID, biometric devices, etc
- Common communication standards between microcontrollers and sensors.
- Each device is recognized by its unique address and can operate as either a transmitter or receiver, depending upon the function of the device
- It Provides enhance security system
- Compatible with FPGA.

#### VI. CONCLUSION

This paper reviews about implementation of I2C protocol which reduces the requirement of wires in embedded system. It is useful in terms of number of pin count and with easier controlling. Implementation of I2C on FPGA is beneficial for data processing, minimal coding and faster operation. Implementation of protocol on FPGA helps in development of dedicated hardware for various applications. In proposed system going to implement I2C master bus controller on FPGA using VHDL and The low speed peripherals RTC (DS1302) and EEPROM are interfacing with I2C master bus through Nios-II Softcore Processor.

#### ACKNOWLEDGMENT

The authors would like to thank the researchers as well as publishers for making their resources available and teachers and guide for their guidance. We are thankful to the authorities of Savitribai Phule University, Pune. We also thank the college authorities for providing the required infrastructure and support. Finally, we would like to extend a heartfelt gratitude to friends and family members.

#### VII. REFERENCES

- [1] Bollam Eswari, N. Ponmagal, K. Preethi, S. G. Sreejeesh , “ Implementation of I<sup>2</sup>C Master Bus Controller on FPGA,”

- International Conference on Communication and Signal Processing, India, April 3-5, 2013, pp. 678-681.
- [2] Prof. Jai Karan Singh, “Design and Implementation of I2C master controller on FPGA using VHDL,” IJET, Vol. No. 4, Aug-Sep 2012.
- [3] Breckling A. Khan, A. Thakare, “FPGA Based Design & Implementation of Serial Data Transmission Controller” International Journal of Engineering Science and Technology 2010, pp 5526 – 5533.
- [4] Philips Semiconductor, “I2C Bus Specification” version 2.1, January 2000.
- [5] Arvind Sahu, Ravi Shankar Mishra, Puran Gour, “Design and Interfacing of High speed model of FPGA using I2C protocol,” Int. J. Comp. Tech. Appl., Vol 2 (3), 531-536.
- [6] Trupti D. Shingare, R. T. Patil, “SPI Implementation on FPGA,” International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-2, Issue-2, January 2013.
- [7] Pankaj Kumar Mehto, Pragya Mishra , Sonu Lal, “Design and Implementation for Interfacing Two Integrated Device Using I2C Bus, ” International Journal of Innovative Research in Computer and Communication Engineering, Vol. 2, Issue 3, March 2013.
- [8] J. J Patel, B. H. Soni, “Design and Implementation of I2c Bus Controller Using Verilog,” Journal of Information, Knowledge and Research in Electronics and Communication Engineering Nov 12 To Oct 13, Vol. 02, Issue – 02, page no. 520-522.
- [9] A.Sahu, R. Mishra, P.Gour, “An Implementation of I2C using VHDL for Data Surveillance”, International Journal on Computer Science and Engineering, pp-1857-1865, May 2011.